

of the mounting head 122 around the rotation axis Rb and the horizontal position of the stage 120 according to the needs.

[0021] The control part 130 controls the driving of each part and includes, for example, a CPU which performs various calculations and a memory part 138 which stores various data and programs. The control part 130 functions as a first lamination process part 132, a first permanent bonding process part 134, a second lamination process part 135, and a second permanent bonding process part 136 by reading programs from the memory part 138. The first lamination process part 132 forms a first chip laminate body by sequentially temporarily bonding one or more semiconductor chips 10 on the substrate 30 with the bonding part 106. The first permanent bonding process part 134 collectively permanently bonds the one or more semiconductor chips 10 which form the first chip laminate body with the bonding part 106. The second lamination process part 135 forms a second chip laminate body by sequentially laminating while temporarily bonding two or more semiconductor chips 10 on the permanently bonded semiconductor chips 10 with the bonding part 106. The second permanent bonding process part 136 collectively permanently bonds the two or more semiconductor chips 10 which form the second chip laminate body with the bonding part 106.

[0022] Note that the configuration of the mounting apparatus 100 described here is an example and is changed as appropriate. For example, in the embodiment, both the temporary bonding and the permanent bonding are performed by one mounting head 122, but a pressurizing head for the temporary bonding and a pressurizing head for the permanent bonding is provided. Further, in the embodiment, the stage 120 is configured to move horizontally, but the mounting head 122 is configured to move horizontally instead of or in addition to the stage 120. In addition, the configurations of the chip supplying part 102, the chip transporting part 104 and the like is changed as appropriate.

of a semiconductor device in which the plurality of semiconductor chips 10 are laminated and mounted on the substrate 30. The semiconductor device is configured by laminating and mounting a target lamination number of semiconductor chips 10 in each of the plurality of disposition regions 34. In the embodiment, the target lamination number is “8”, and eight semiconductor chips 10 are laminated and mounted in one disposition region 34. Hereinafter, a thing in which eight semiconductor chips 10 have been laminated and mounted is called a “finished laminate body ST0”.

[0030] In the embodiment, the finished laminate body ST0 is divided into and treated as a plurality of chip laminate bodies – specifically, a first chip laminate body ST1 and a second chip laminate body ST2. The first chip laminate body ST1 is a laminate body formed by four semiconductor chips 10 laminated on the substrate 30. Further, the second chip laminate body ST2 is a laminate body formed by four semiconductor chips 10 laminated on the first chip laminate body ST1. In the embodiment, after a first lamination step and a first permanent bonding step are performed to form the first chip laminate body ST1, a second lamination step and a second permanent step of forming the second chip laminate body ST2 are performed. In this way, one finished laminate body ST0 is divided into and treated as two or more laminate bodies ST1 and ST2, and this is for well mounting all the semiconductor chips 10, which will be described later.

[0031] Next, a flow of mounting the semiconductor chips 10 will be described with reference to FIGs. 5 to 7. FIGs. 5 to 7 are image diagrams showing a flow of mounting the semiconductor chips 10. Three disposition regions 34 are illustrated in FIGs. 5 to 7, and for convenience of description, these are referred to as a region A, a region B, and a region C in order from the left side. Further, the mounting procedure described below is performed under normal pressure or is performed in a vacuum to prevent inclusion of air bubbles and the like.

[0032] In the embodiment, as described above, first, after the first chip laminate body ST1 is mounted, the second chip laminate body ST2 is further mounted on the first chip laminate body ST1, and finally, the finished laminate body ST0 having eight layers is formed. Each of the chip laminate bodies ST1 and ST2 is mounted by performing a lamination step of sequentially laminating the four semiconductor chips 10 while temporarily bonding them to form the chip laminate bodies ST1 and ST2 in a temporarily bonded state and performing a permanent bonding step of collectively permanently bonding the four semiconductor chips 10 by heating at the second temperature T2 and pressurizing from the upper side of the chip laminate bodies ST1 and ST2.

[0033] Specifically speaking, first, at the beginning, as shown in (a) of FIG. 5, the mounting head 122 is used to dispose the semiconductor chip 10 in the region A on the substrate 30. At this time, the substrate 30 is positioned with respect to the semiconductor chip 10 so that the bumps 18 of the semiconductor chip 10 face electrode terminals 32 on the substrate 30. In addition, at this time, the mounting head 122 is heated to the first temperature T1 which is the temperature for temporary bonding. Next, as shown in (b) of FIG. 5, the semiconductor chip 10 is pressurized with the prescribed first load Ft1 by the mounting head 122, and the semiconductor chip 10 is temporarily bonded to the substrate 30. At this time, the NCF 20 is heated to the softening start temperature Ts or more by the heat transfer from the mounting head 122 and exhibits appropriate fluidity. In this way, the NCF 20 fills the gap between the semiconductor chip 10 and the substrate 30 without any gap. Note that the first load Ft1 is not particularly limited as long as the amount of the first load Ft1 allows the bumps 18 to contact the electrode terminals 32 of the substrate 30 by pushing away the softened NCF 20 without significantly deforming the bumps 18.

[0034] When the first-layer semiconductor chip 10 can be temporarily bonded, then the

second-layer semiconductor chip 10 is further temporarily bonded onto the temporarily bonded first-layer semiconductor chip 10. When the second-layer semiconductor chip 10 is being temporarily bonded, the same as the case in the first-layer semiconductor chip 10, the mounting head 122 is used to dispose the second-layer semiconductor chip 10 on the first-layer semiconductor chip 10 so that the bumps 18 of the second-layer semiconductor chip 10 face the electrode terminals 16 of the first-layer semiconductor chip 10. Then, in this state, the second-layer semiconductor chip 10 is heated at the first temperature T1 and pressurized with the first load Ft1 to be temporarily bonded to the first-layer semiconductor chip 10.

10 **[0035]** Thereafter, similarly, the third-layer semiconductor chip 10 is temporarily bonded onto the second-layer semiconductor chip 10, and the fourth-layer semiconductor chip 10 is temporarily bonded onto the third-layer semiconductor chip 10. (c) of FIG. 5 shows a mode in which four layers of the semiconductor chips 10 are laminated in the region A while being temporarily bonded. The step of laminating the four semiconductor chips 10 is the first lamination step, and the formed laminate body becomes the first chip laminate body ST1 in the temporarily bonded state.

[0036] When the first chip laminate body ST1 in the temporarily bonded state can be formed in the region A, the first chip laminate bodies ST1 in the temporarily bonded state are also formed in other disposition regions 34, such as the region B and the region C, in the same procedure. (a) of FIG. 6 shows a mode in which four semiconductor chips 10 are laminated while being temporarily bonded to form the first chip laminate bodies ST1 in the temporarily bonded state in all the disposition regions 34.

[0037] When the first chip laminate bodies ST1 in the temporarily bonded state can be formed in all the disposition regions 34, then the first permanent bonding step is performed for permanently bonding the first chip laminate bodies ST1. Specifically,

first, the mounting head 122 is heated to the second temperature T_2 which is the temperature for permanent bonding. Then, as shown in (b) of FIG. 6, the first chip laminate body ST1 in the temporarily bonded state is pressurized with the second load F_{t2} by the mounting head 122 heated to the second temperature T_2 , and the four semiconductor chips 10 are permanently bonded collectively. Note that the second load F_{t2} is not particularly limited as long as the pressing amount of the bumps 18 can be properly maintained.

[0038] By being pressed by the mounting head 122 heated to the second temperature T_2 , the four semiconductor chips 10 forming the first chip laminate body ST1 are also heated. However, the heating temperature decreases as the distance from the mounting head 122 increases. Specifically, the uppermost-layer (fourth-layer) semiconductor chip 10 is heated to substantially the same temperature as the second temperature T_2 , but the lowermost-layer (first-layer) semiconductor chip 10 is heated to a lower layer temperature $T_a = T_2 - \Delta T$, which is less than the second temperature T_2 by ΔT . The second temperature T_2 is set so that the lower layer temperature T_a becomes greater than the melting temperature T_m and the curing start temperature T_t . That is, at the time of permanent bonding, all the four semiconductor chips 10 forming the first chip laminate body ST1 are heated to a temperature greater than the melting temperature T_m and the curing start temperature T_t .

[0039] Each semiconductor chip 10 is heated to above the curing start temperature T_t , whereby the NCF 20 of the semiconductor chip 10 gradually cures. Then, by curing the NCF 20, the semiconductor chip 10 and the bonded body (the substrate 30 or the lower semiconductor chip 10) are firmly fixed mechanically. In addition, the bumps 18 can be melted and glued to the opposite electrode terminals 32 and 16 by being heated to above the melting temperature T_m . Then, in this way, the four semiconductor chips 10 and the

substrate 30 become to be in a mounting state in which they are electrically bonded to each other. Then, the step of collectively permanently bonding the four semiconductor chips 10 which form the first chip laminate body ST1 becomes the first permanent bonding step.

5 **[0040]** When one first chip laminate body ST1 can be permanently bonded, subsequently, other first chip laminate bodies ST1 are also permanently bonded. That is, the first permanent bonding step is performed in all of the two or more disposition regions 34 such as the region B, the region C and the like. (c) of FIG. 6 shows a mode in which the first permanent bonding step is performed in all the disposition regions 34.

10 **[0041]** When the first permanent bonding step is performed in all the disposition regions 34, subsequently, the second lamination step is performed for forming the second chip laminate bodies ST2 in the temporarily bonded state on the first chip laminate bodies ST1. Specifically, the temperature of the mounting head 122 is lowered to the first temperature T1 which is the temperature for temporary bonding. Thereafter, as
15 shown in (a) and (b) of FIG. 7, another four semiconductor chips 10 are sequentially laminated while being temporarily bonded on the permanently bonded first chip laminate bodies ST1. In this way, the formed laminate bodies are the second chip laminate bodies ST2, and the step of forming the second chip laminate bodies ST2 is the second lamination step. The second lamination step is also performed in all of the two or more
20 disposition regions 34. When the second chip laminate bodies ST2 in the temporarily bonded state are formed in all the disposition regions 34, finally, the second permanent bonding step is performed for permanently bonding all the second chip laminate bodies ST2. Then, when all the second chip laminate bodies ST2 are permanently bonded, the mounting step is completed.

25 **[0042]** As is clear from the above description, in the embodiment, one finished

body ST1 is formed, the next first chip laminate body ST1 is formed. Specifically speaking, in the embodiment, first, one semiconductor chip 10 is disposed in one disposition region 34 (the region A) by the mounting head 122 heated to the first temperature T1. Then, in this state, the first load Ft1 is applied to temporarily bond the semiconductor chip 10. Thereafter, the mounting head 122 is heated to the second temperature and then pressurizes the semiconductor chip 10 with the second load Ft2. That is, the first lamination step and the first permanent bonding step are continuously performed. In this step, one permanently bonded semiconductor chip 10 becomes the first chip laminate body ST1. When the first chip laminate body ST1 can be formed in the region A, subsequently, the first chip laminate bodies ST1 are also sequentially formed in the region B and the region C which are the remaining disposition regions 34. (a) of FIG. 8 shows a mode in which the first chip laminate bodies ST1 are formed in all the disposition regions 34.

[0048] Once in this state, subsequently, the second chip laminate bodies ST2 are formed. The formation procedure of the second chip laminate bodies ST2 is the same as that in the first embodiment. That is, a plurality of (three in the example shown in the drawings) semiconductor chips 10 are sequentially laminated while being temporarily bonded on the first chip laminate body ST1 by the mounting head 122 heated to the first temperature T1, and the second chip laminate body ST2 in the temporarily bonded state is formed. When one second chip laminate body ST2 can be formed, then other second chip laminate bodies ST2 are also formed in other disposition regions 34 in the same way. That is, the second lamination step is performed in all of the two or more disposition regions 34. (b) of FIG. 8 is a diagram showing a mode in which the second chip laminate bodies ST2 in the temporarily bonded state are formed. Subsequently, the mounting head 122 pressurizes the second chip laminate bodies ST2 in a state in which the

mounting head 122 is heated to the second temperature T2 for permanent bonding and collectively permanently bonds the four semiconductor chips 10. (c) of FIG. 8 is a diagram showing the mode of the second permanent bonding step. When the second permanent bonding step is completed in one disposition region 34, the second permanent bonding step is performed in the remaining disposition regions 34 in the same way. Thereafter, the second lamination step and the second permanent bonding step are repeated until the total lamination number of the semiconductor chips 10 reaches the target lamination number. For example, in the case where the target lamination number is “8”, once in the state shown of (c) of FIG. 8, subsequently, after four layers of the semiconductor chips 10 have been further laminated on each second chip laminate body ST2 while being temporarily bonded, the second lamination step and the second permanent bonding step is performed for the second time for permanent bonding. Further, in the case where the target lamination number is “10”, after the second lamination step and the second permanent bonding step have been performed for the second time as described above, two layers of the semiconductor chips 10 are further laminated while being temporarily bonded, and then the second lamination step and the second permanent bonding step is performed for the third time for permanent bonding.

[0049] By the way, as is clear from the above description, in the embodiment, the chip lamination number of the first chip lamination body ST1 is one. In other words, after the first-layer semiconductor chips 10 are permanently bonded in all of the two or more disposition regions 34, the second-layer and subsequent layers of the semiconductor chips are laminated. The reason for this configuration is as follows.

[0050] The substrate 30 in the embodiment is a semiconductor wafer made of silicon or the like. The semiconductor wafer has a high thermal conductivity compared with a normal resin substrate or the like. Therefore, the heat applied to the chip laminate body

in the region A by the permanent bonding is transferred to the chip laminate body in the adjacent region B. At this time, as shown in (b) of FIG. 6, it is assumed that the first-layer semiconductor chip 10 in the region B adjacent to the region A is in the temporarily bonded state when the chip laminate body in the region A is being permanently bonded. In this case, the heat transferred via the chip laminate body in the region A and the substrate 30 is also transferred to the first-layer semiconductor chip 10 in the region B. Then, the transferred heat causes the NCF 20 of the first-layer semiconductor chip 10 in the region B to start to cure. As described above, when the NCF 20 cures prior to the permanent bonding, the fixing of the semiconductor chip 10 to the substrate 30 becomes insufficient.

[0051] Therefore, in the embodiment, to prevent unintended curing of the NCF 20, the lamination of the second-layer and subsequent layers of the semiconductor chips 10 are performed after all of the first-layer semiconductor chips 10 are permanently bonded. In the case of this configuration, as shown in (c) of FIG. 8, the heat when the second-layer and subsequent layers of the semiconductor chips 10 are being permanently bonded in the region A is also transferred to the first-layer semiconductor chip 10 in the region B via the chip laminate body in the region A and the substrate 30. However, since the first-layer semiconductor chip 10 in the region B has already been permanently bonded, no problem occurs even if the heat is transferred thereto. Further, the heat is also transferred to the second-layer and subsequent layers of the semiconductor chips 10 in the region B via the first-layer semiconductor chip 10 in the region B. However, since the heat path from the heat source (the mounting head 122) is long for the second-layer and subsequent layers of the semiconductor chips 10 in the region B, the amount of heat transfer is small, and the curing of the NCFs 20 is unlikely to occur. Furthermore, the permanently bonded semiconductor chip 10 is interposed on the way of the heat path