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REDUCED MASK PROCESS FOR MANUFACTURE
OF MOS GATED DEVICES

BACKGROUND OF THE INVENTION

5 This invention relates to MOS gated devices,
and more specifically relates to a novel process which
exploits the different implantation ranges of certain N
and P impurities to produce a junction pattern with fewer
mask steps and only two critical mask alignments.

10 MOS gated devices, such as power MOSFETs,
Insulated Gate Bipolar Transistors (IGBTs) and MOS gated
thyristors are well known. The process used for the
manufacture of these devices employs a sequence of
masking steps in which many of the masks must be
carefully and critically aligned with respect to one
15 another. Each mask layer in a process increases
manufacturing expense, and each mask step introduces a
new possible source of defects. Moreover, the
requirement of aligning several masks with critical
accuracy relative to one another also adds manufacturing
20 costs and introduces the possibility of additional
manufacturing defects.

25 A process for manufacturing such devices which
employs a reduced number of masks, and a reduced number
of critical alignments between masks is desirable since
it reduces wafer handling, potential defects and the cost
of the individual chips in a wafer.

SUMMARY OF THE INVENTION

In accordance with the present invention, an
oxide layer, having adjacent thin and thick regions is

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formed in a first masking step. A critically aligned patterned polysilicon layer is formed in a second masking step to accurately deposit polysilicon layers in predefined regions of the thin oxide, which becomes the gate oxide of a MOS gated device. A first species is then implanted through both the thin and the thick oxide exposed by the patterned polysilicon so as to form spaced base regions. A second species is next implanted at an energy sufficient to penetrate only the thinner oxide regions exposed between the edges of the polysilicon and the edges of the thicker oxide, but not the exposed thicker oxide, to form source regions within the bases with critical alignment. After the base regions and source regions are formed as described above, a mask step which defines contact windows in a low temperature oxide which covers the wafer surface is carried out. This mask is critically aligned with the polysilicon mask.

Note that this process has only two critical alignment masking steps as described above. The first is the alignment of the polysilicon mask to the prior mask which defined the thin and thick oxide regions. The second is the alignment of the contact window mask to the prior polysilicon mask.

A plurality of series-connected PMOS devices can be formed during the process steps described above to form a termination surrounding the device active area.

More specifically, for fabricating semiconductor devices, masks are used to form each of the different layers necessary for the functioning of the semiconductor devices. In the present invention, in effect, a single mask defines two layers. Using a vertical N channel power MOSFET as an example, the vertical N channel power MOSFET consists of basically two



diffused regions: a shallow N^+ region and a deeper P body region. The range of boron (a P type dopant) in silicon dioxide is about five times that of arsenic (an N type dopant). An oxide thickness of 3000 Å can be
5 penetrated by boron implantation of greater than about 80 KeV while it would mask against arsenic implantation of less than about 120 KeV. In accordance with the invention, this property is used to define both the P body and N^+ regions using a single oxide layer and
10 polysilicon mask (eliminating the source mask). The device process then employs a further critical mask for defining all contact regions. This mask and the mask for defining the polysilicon pattern are the only two masks which require a critical, or high-accuracy alignment.
15 Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Figure 1 is a cross-sectional view of a small portion of a wafer after a first masking step and the definition of a pattern of thin and thick oxides.

Figure 2 shows the wafer portion of Figure 1, following a second mask used to pattern a polysilicon
25 layer with a critical alignment to the first mask.

Figure 3 shows the wafer portion of Figure 2 after an implant of a base region through exposed thick and thin oxide regions and the drive of the device base regions.

30 Figure 4 shows the wafer portion of Figure 3 following the implant of the source region through the



exposed thin oxide only, to form source regions and the anneal of those regions.

Figure 5 shows the wafer portion of Figure 5 following the deposition of an oxide interlayer and the formation of contact windows by a mask which is aligned with critical accuracy to the polysilicon mask.

Figure 6 shows the wafer portion of Figure 5, following the deposition of the source metal, and the patterning of the source metal by a non-critical mask step.

Figure 7 shows the use of series-connected PMOS devices as a termination for the device disclosed.

Figure 8 shows the use of floating-field rings with field plates as a termination for the device disclosed.

DETAILED DESCRIPTION OF THE INVENTION

Referring first to Figure 1, there is shown a small portion of a monocrystalline wafer 10 having a relatively thick substrate portion 11 and a relatively thin epitaxially deposited portion 12. Regions 11 and 12 are shown as N type for the manufacture of an N channel device, but the conductivity types can be reversed to form a P channel device.

The present invention can also be used in connection with any desired device topology, such as a cellular topology, as disclosed in Patent 5,008,725 or interdigitated topology, as shown in Patent 4,376,286. Further, the invention can be used for the manufacture of any desired type of MOS gated device, such as power MOSFETs, IGBTs, MOS gated thyristors, and the like.

In the embodiment disclosed, an N channel power MOSFET of interdigitated topology is disclosed. In



Figure 1, a thick oxide layer, of thickness of about 3000 Å, is first grown atop the epitaxial layer 12. This oxide is then coated with a photoresist, the resist is patterned with a first mask pattern (not shown) and the thick oxide is etched forming thick, spaced, parallel strips 14, 15 and 16. Any number of strips 14, 15 and 16 can be used and they may extend around predetermined parallel paths. These regions may also have the shapes of spaced closed polygons.

Thin oxide strips 18 and 19 are then regrown on the exposed silicon surface to a thickness, for example, of 500 Å. These regions 18 and 19 are between thick regions 14-15 and 15-16, respectively. Portions of regions 18 and 19 will ultimately define the gate oxide for the device. The thick and thin regions can have other thicknesses than 3000 Å and 500 Å respectively, and their thicknesses are selected based on the desired gate characteristics, the ion species to be implanted to form P and N regions and the implant energy to be used.

Thereafter, a layer of polysilicon is grown atop the surface of the device as shown in Figure 2 and a photoresist is deposited thereon and is patterned by a second mask which is critically, (very accurately) aligned to the first mask which defined the location of the thick and thin regions 14, 15, 16, 18 and 19. The polysilicon is then etched, leaving strips 20, 21, 22, 23, 24 and 25 in place. Strips 22 and 23 are gates for the MOS gated devices being made and are accurately located centrally atop thin gate oxide regions 18 and 19, defining gaps approximately 2 microns from the sides of each of the adjacent thick oxide regions and 5 microns wide.



Polysilicon strips 20-21 and 24-25 are spaced apart by a gap of about 3 microns. Strips 20, 21, 24 and 25 and other adjacent strips, not described will define guard rings and diffusions, as will be shown later.

5 Thereafter, as shown in Figure 3, a boron implant is carried out, using the polysilicon strips 20 to 25 as a mask, at an energy sufficient to penetrate both the thin and thick exposed oxide layers 14, 15, 16, 18 and 19. For example, boron implantation at an energy
10 of about 80 KeV or higher can be used at a dose of $7E13cm^2$. Species other than boron could alternately be selected. The energy used for the implant is determined, in part, by the thickness of the thick oxide. This implant is followed by a drive at 1175°C shown in Figure
15 3 for 30 minutes to form the P type regions 30 to 36. Note that regions 30, 31, 35 and 36 are sections through guard rings which terminate active base regions 32 and 34.

 Thereafter, and as shown in Figure 4, arsenic
20 is implanted into the silicon surface, using the same polysilicon strips 20 to 25 as masks. The energy selected for the arsenic implant (or any other species selected) is sufficient to penetrate the thin exposed gate oxide layers 18 and 19, but it is blocked by the
25 thicker exposed oxide regions. Arsenic, at an energy of 80 KeV and a dose of $1E16$, reaches the underlying silicon and forms N^+ source strips 40, 41, 42 and 43 in the bases 32, 33 and 34.

 As next shown in Figure 5, a layer of low
30 temperature oxide (LTO) 50 is deposited atop the wafer of Figure 4 to a thickness of about 7000 Å. The LTO is then patterned in a second critical masking step (relative to the polysilicon mask) to form contact windows 60 to 64.



Windows 60 and 64 expose the surfaces of rings 21 and 24,
windows 61 and 63 expose the surfaces of P regions 32 and
34, respectively, and sources 40 and 43, respectively,
and window 62 exposes the surfaces of base 33 and sources
5 41 and 42.

Note that if the topology of the device of
Figure 5 is chosen to be ring-shaped, base 33 may have a
polygonal shape, with sources 41 and 42 being sections
through a single annular source, and with bases 32 and 34
10 being sections through a single base which is concentric
with base 33, and with rings 31 and 35 being sections
through a single ring also concentric with base 33.

Thereafter, and as shown in Figure 6, a source
metal 50 is deposited atop the surface of Figure 5 to
15 make contact to rings 21 and 24 which terminate the
active area of the device and to base regions 32, 33 and
34 and their sources 40, 41-42 and 43, respectively.
Thereafter, a metal pattern is defined, using a fourth,
but non-critical mask step.

Figure 7 shows the use of a plurality of series
connected PMOS devices which can be used to terminate the
active area of the device of Figure 6. These rings are
formed during the same steps which are used to form the
active area of the devices.

Thus, in Figure 7, a polysilicon field plate 70
25 which may encircle the active area is formed during the
polysilicon etch step. A gate bus 71 is attached to
plate 70 which plate is continuous with the full
polysilicon gate area in the active device. Polysilicon
rings 80, 81 and 82 can be also formed during the
30 polysilicon etch step for the active device. P type
rings 90 to 93 are diffused during the step of Figure 3
and are defined by polysilicon patterns 70, 80, 81 and



82. Small contacts, schematically shown by dotted lines 95, 96 and 97 connect P regions 90, 91 and 92 to gates 80, 81 and 82 of the 3 PMOS devices shown, shorting the source and gate electrodes of each PMOS device. Thus, 5 the threshold voltages of the 3 PMOS devices are connected in series to terminate the device. Any desired number of PMOS devices can be used, as required by the voltage to be terminated.

The arrangement of Figure 7 shows a termination 10 structure in which the rings or strips 90, 91 and 92 are shorted to limit voltage to the device threshold voltages. Figure 8 shows another termination structure in which each of polysilicon rings 80, 81 and 82 is shorted to the next P ring 91, 92 and 93 respectively to 15 its right, limiting the voltage to the punch-through voltage between P rings and biasing the PMOS devices off. Small contacts, schematically shown in Figure 8 by dotted lines 195, 196 and 197, connect P regions 91, 92 and 93 to polysilicon field rings 80, 81 and 82. A combination 20 of the above two termination structures can also be used.

The shorting contacts used are preferably only sparsely spaced around the rings and the contact positions are defined during the contact opening mask step. Thus, small area contacts 95, 96 and 97 may be 25 located in a corner of a rectangular chip. The small area contacts 95, 96 and 97 may be separated from the source metal during the metal mask step.

Although the present invention has been described in relation to particular embodiments thereof, 30 many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be



limited not by the specific disclosure herein, but only
by the appended claims.

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WHAT IS CLAIMED IS:

1. A process for the manufacture of a MOS gated semiconductor device, characterized in comprising the steps of:

5 (a) forming an insulation layer atop a major surface of a silicon wafer;

(b) patterning said insulation layer in a first mask step to define at least a first area which is thicker than at least a thickened second area adjacent to said first area;

10 (c) depositing a layer of polysilicon atop said insulation layer and patterning said polysilicon layer in a second masking step to cover and mask a third area and to expose a fourth area of said second area;

15 (d) implanting first species atoms at an energy sufficient to penetrate both said first and second insulation areas and diffusing said implanted first species atom to form at least one base region in said silicon wafer in an area exposed by said patterned polysilicon;

20 (e) implanting second species atoms at an energy sufficient to penetrate said second insulation area but insufficient to penetrate said first insulation area, thereby to form at least one source region in said at least one base region;

25 (f) and thereafter forming a source contact which contacts said at least one source region and at least one base region.

2. The process of claim 1 which is further characterized in that said insulation layer is silicon dioxide.





3. The process of claims 1 and 2 which is further characterized in that a plurality of adjacent first and second areas are formed in said insulation layer, thereby to ultimately define a plurality of adjacent respective base regions and source regions.

4. The process of claims 2 and 3 which is further characterized in that said first area has a thickness of approximately 2500 Å and said second area has a thickness of less than about 1000 Å.

5. The process of claims 1 to 4 which is further characterized in that said first species is boron and said second species is arsenic.

6. The process of claim 5 which is further characterized in that the energy of implantation of said boron is greater than about 80 KeV and the energy of implantation of said arsenic is less than about 80 KeV.

7. The process of claims 1 to 6 which further includes the step of depositing and patterning a layer of low temperature oxide after step (e) in an alignment mask step to expose at least portions of said base and source regions prior to forming said source contact.

8. The process of claims 1 to 7 which is further characterized in that a portion of said polysilicon patterned layer overlies a portion of said first area to expose a further area of said first area to define at least one guard ring diffusion in said silicon surface during the formation of said base region.

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