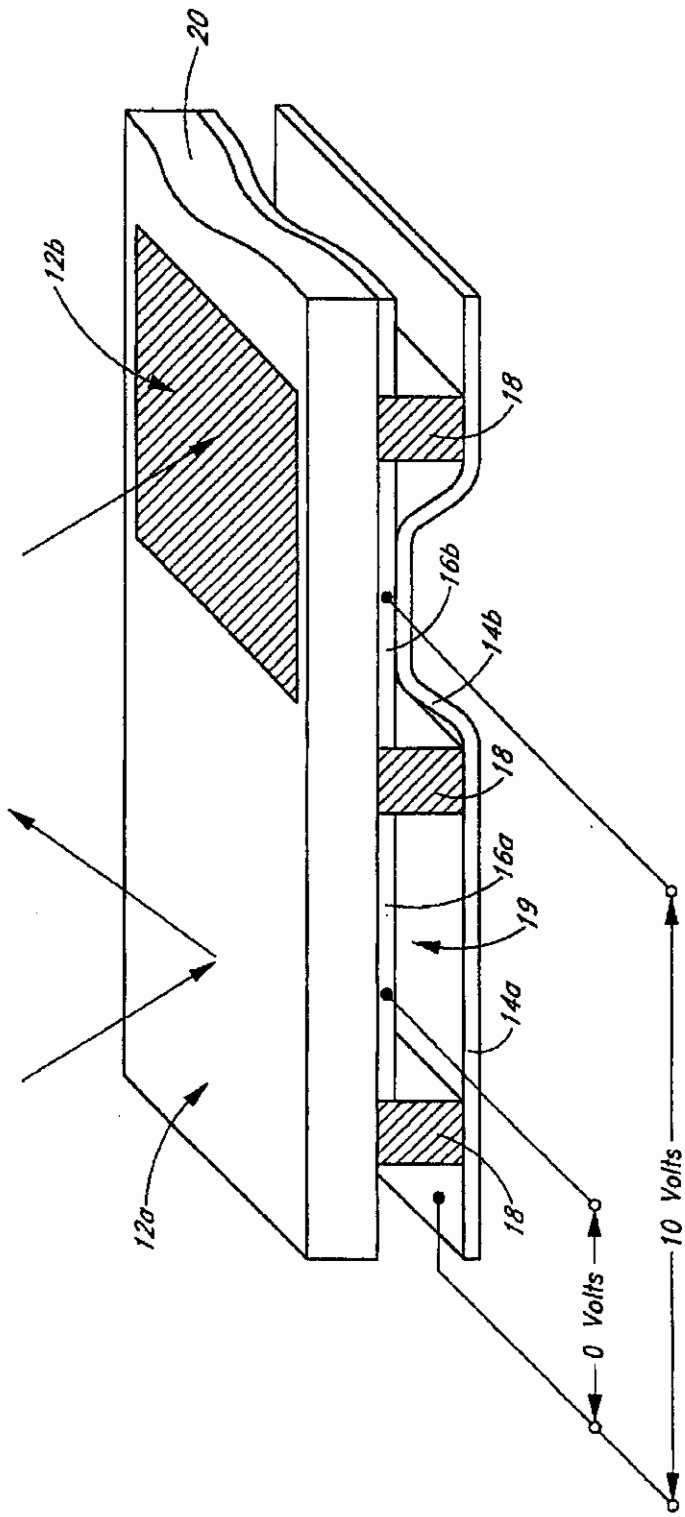


FIG. 1

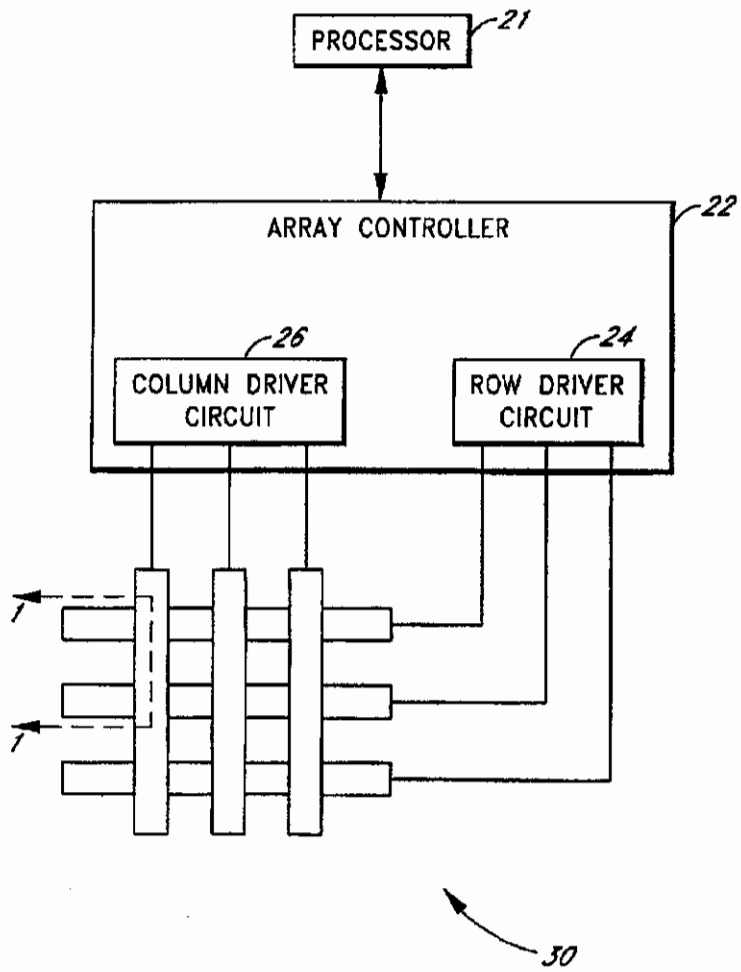

PROCESSOR
21
ARRAY CONTROLLER
22
26
COLUMN DRIVER CIRCUIT
24
ROW DRIVER CIRCUIT
1
1
30

FIG. 2

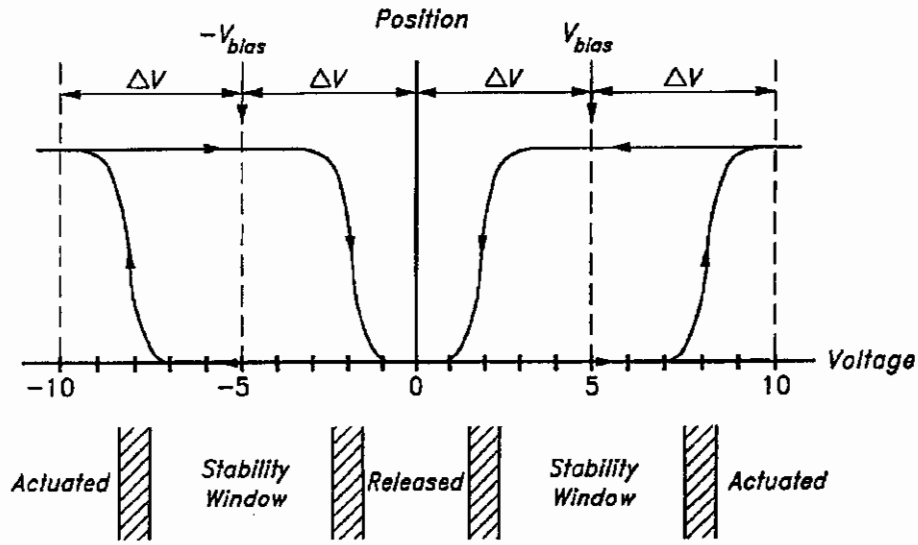


FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
+ ΔV	Relaxed	Actuate
− ΔV	Actuate	Relaxed

FIG. 4

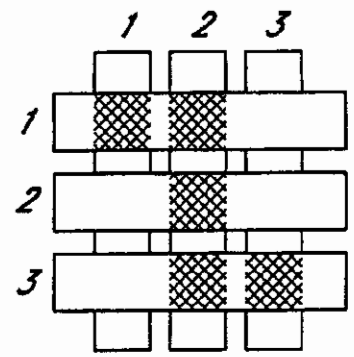

1
2
3
1
2
3
30

FIG. 5A

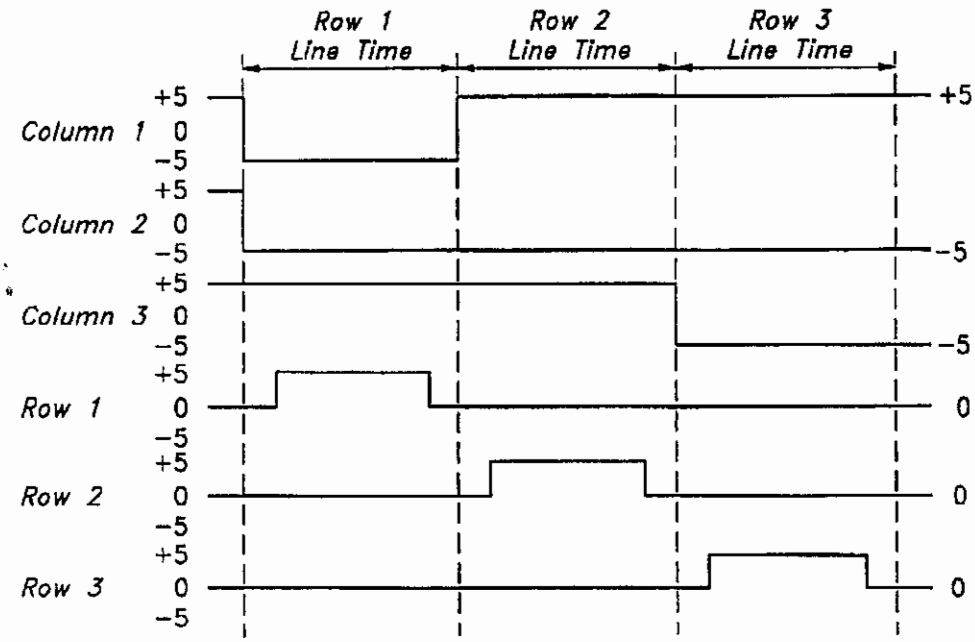

Row 1 Line Time
Row 2 Line Time
Row 3 Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
−5
+5
−5
−5
0
0
0

FIG. 5B

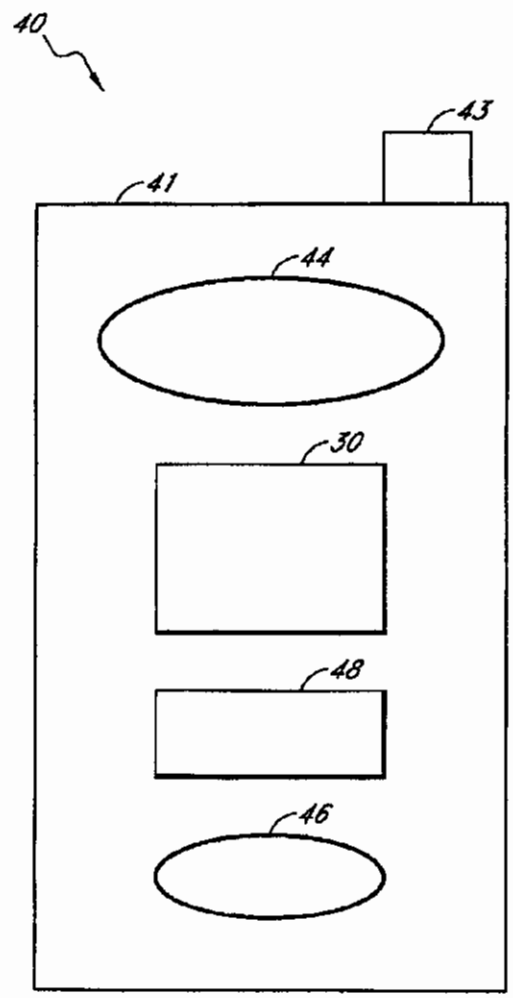


FIG. 6A

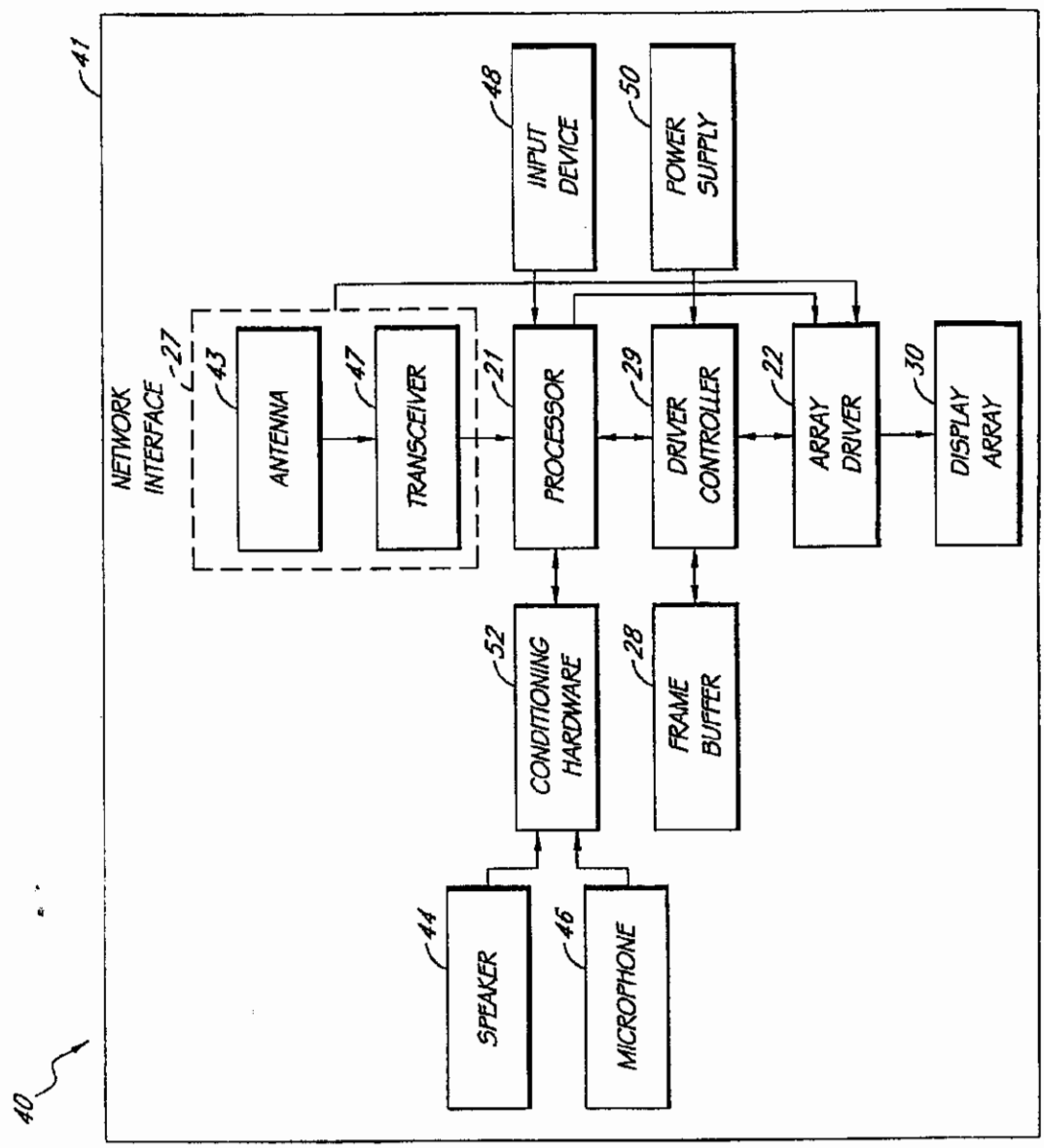

40
41
NETWORK INTERFACE
27
ANTENNA
43
TRANSCEIVER
47
21
PROCESSOR
INPUT DEVICE
48
POWER SUPPLY
50
DRIVER CONTROLLER
29
ARRAY DRIVER
22
DISPLAY ARRAY
30
CONDITIONING HARDWARE
52
FRAME BUFFER
28
SPEAKER
44
MICROPHONE
46

FIG. 6B

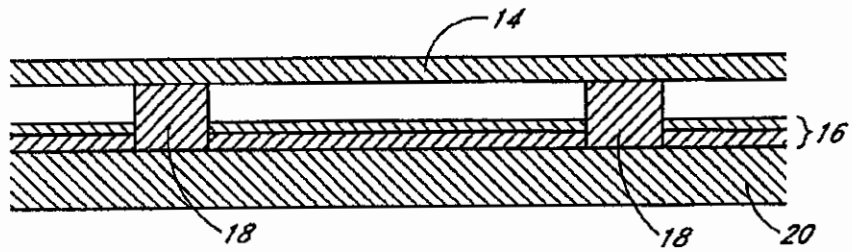


FIG. 7A

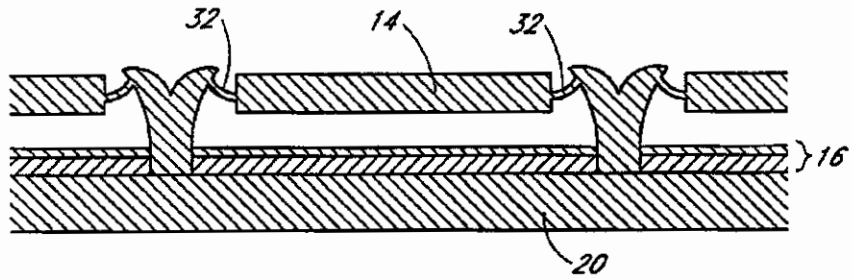


FIG. 7B

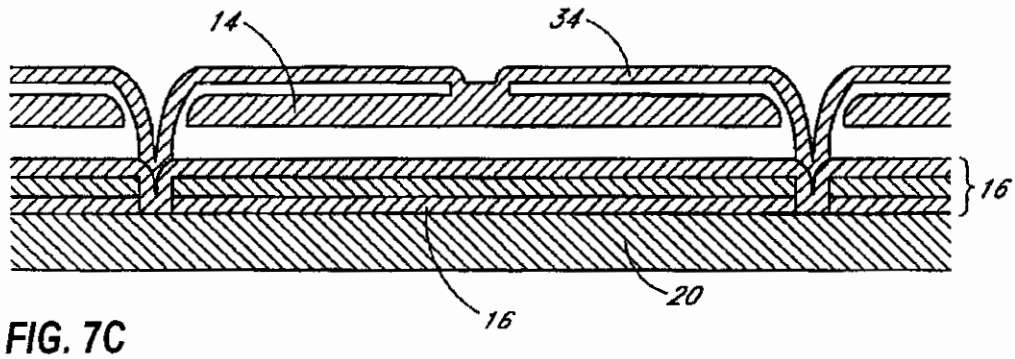


FIG. 7C

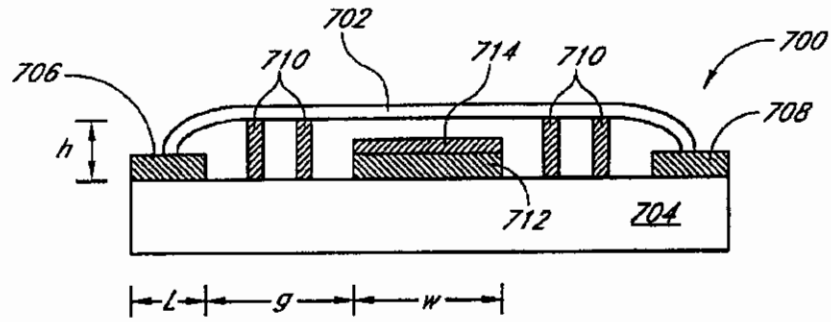

702
710
714
710
700
706
708
h
712
704
L
g
w

FIG. 7D

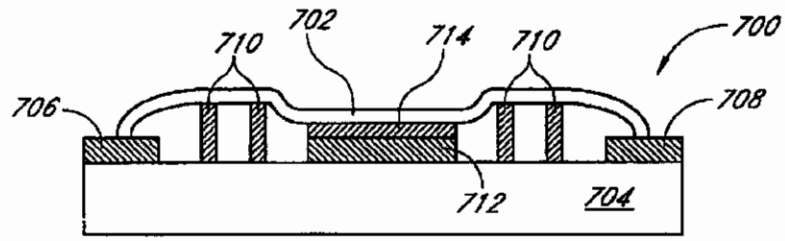

710
702
714
710
700
706
708
712
704

FIG. 7E

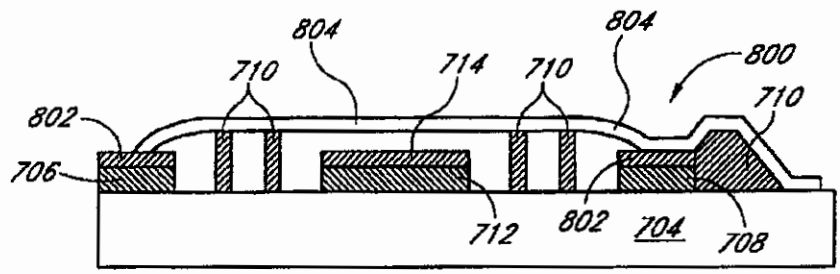

804
804
800
710
714
710
710
802
706
712
802
704
708

FIG. 8

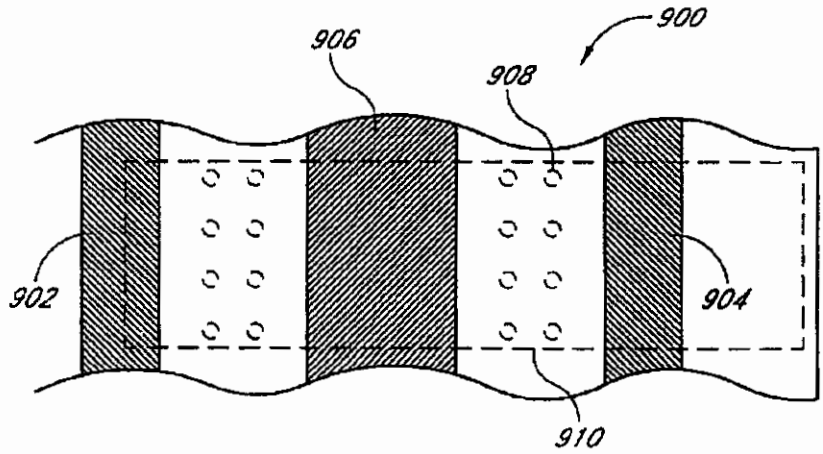

900
906
908
902
904
910

FIG. 9A

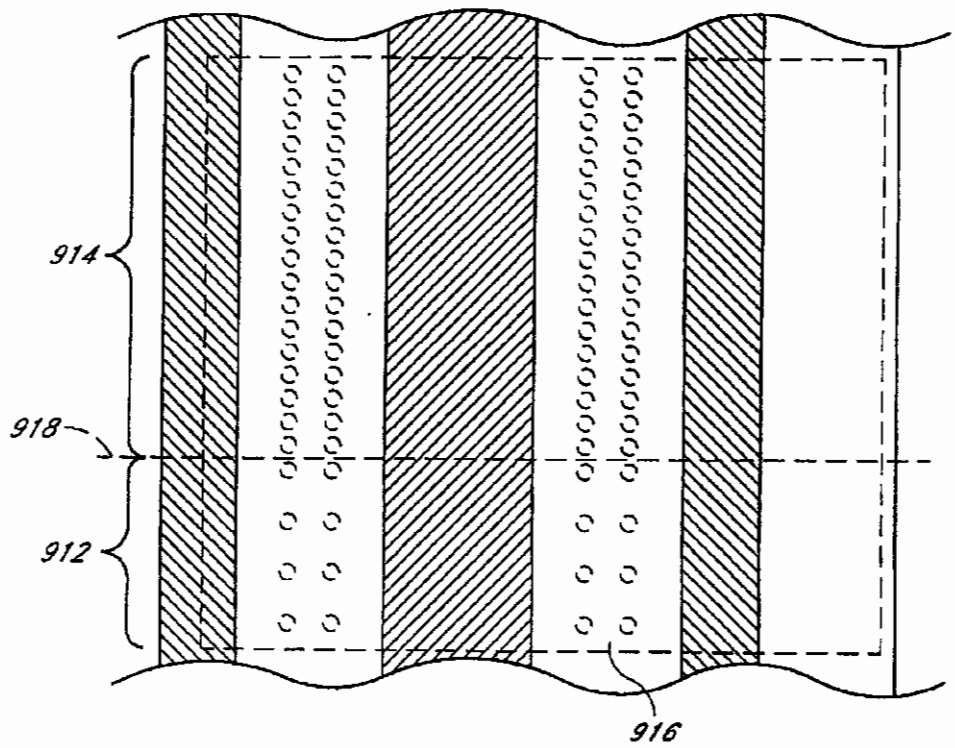


FIG. 9B1

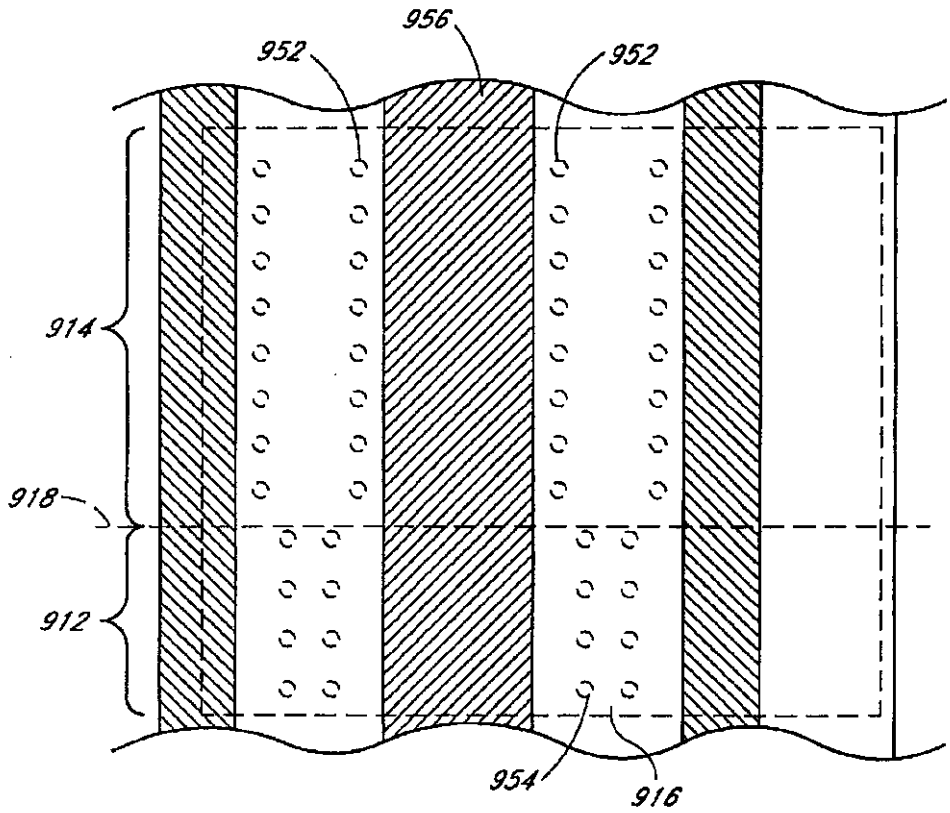


FIG. 9B2

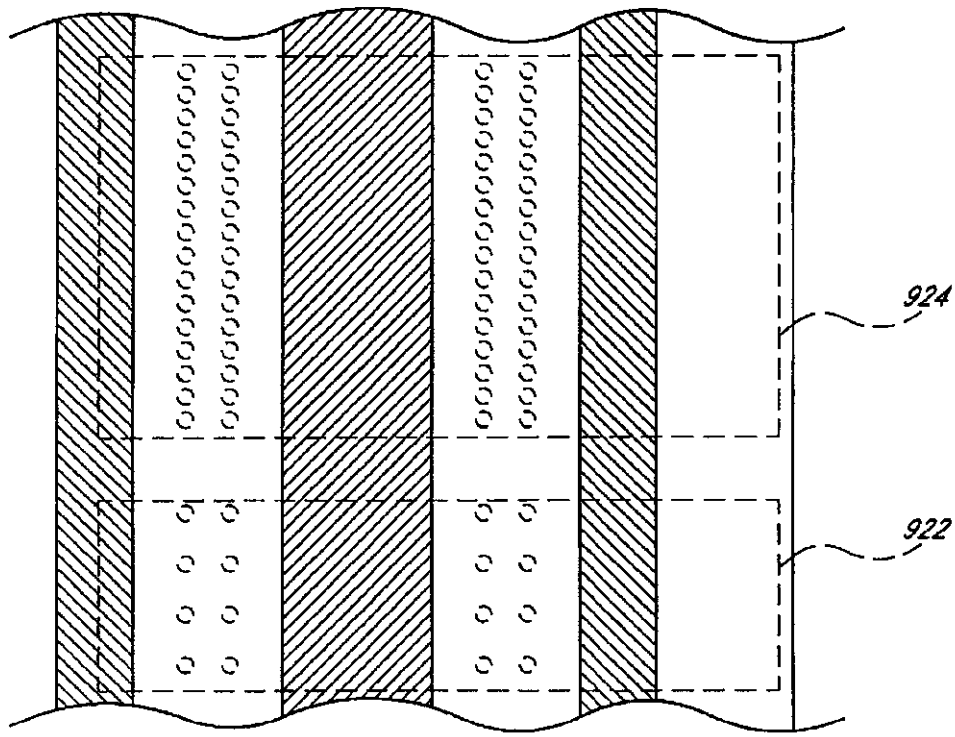


FIG. 9C1

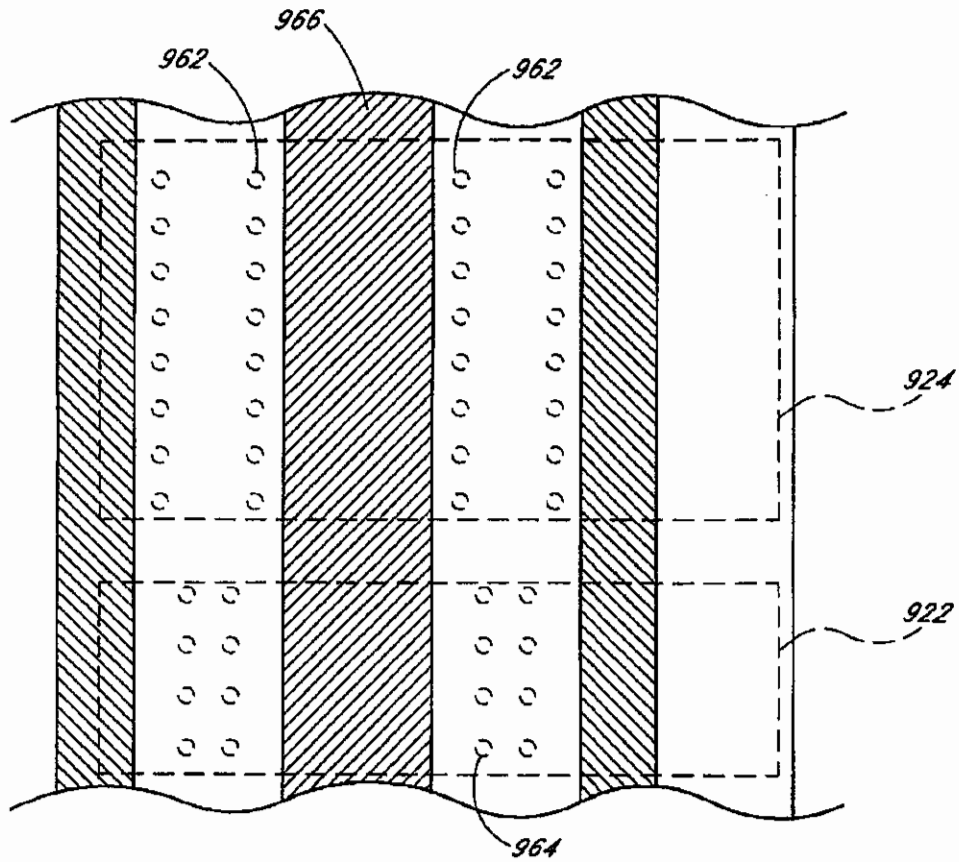


FIG. 9C2

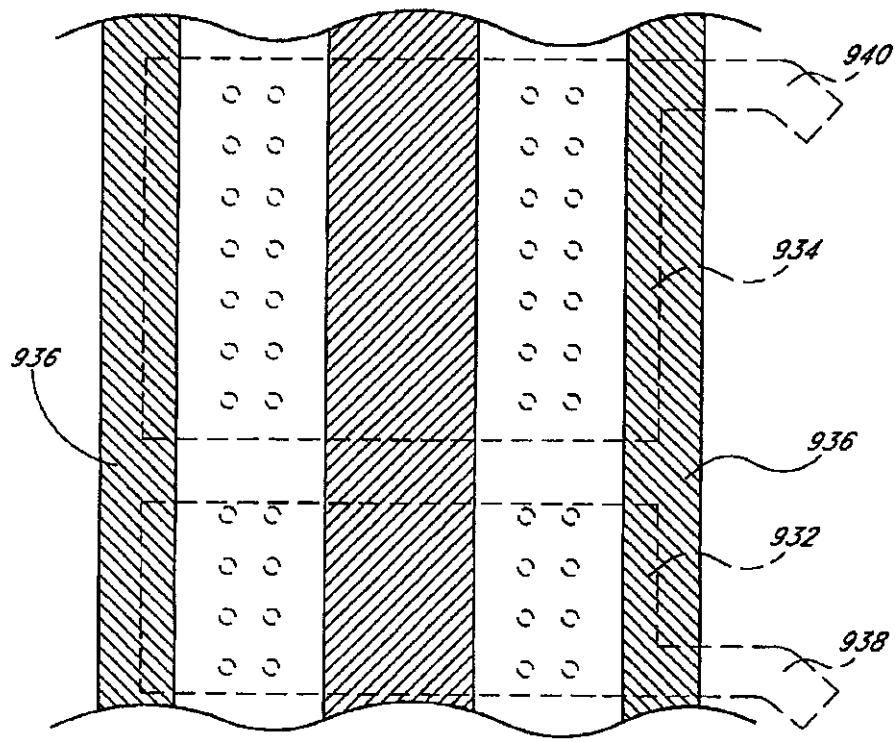


FIG. 9D

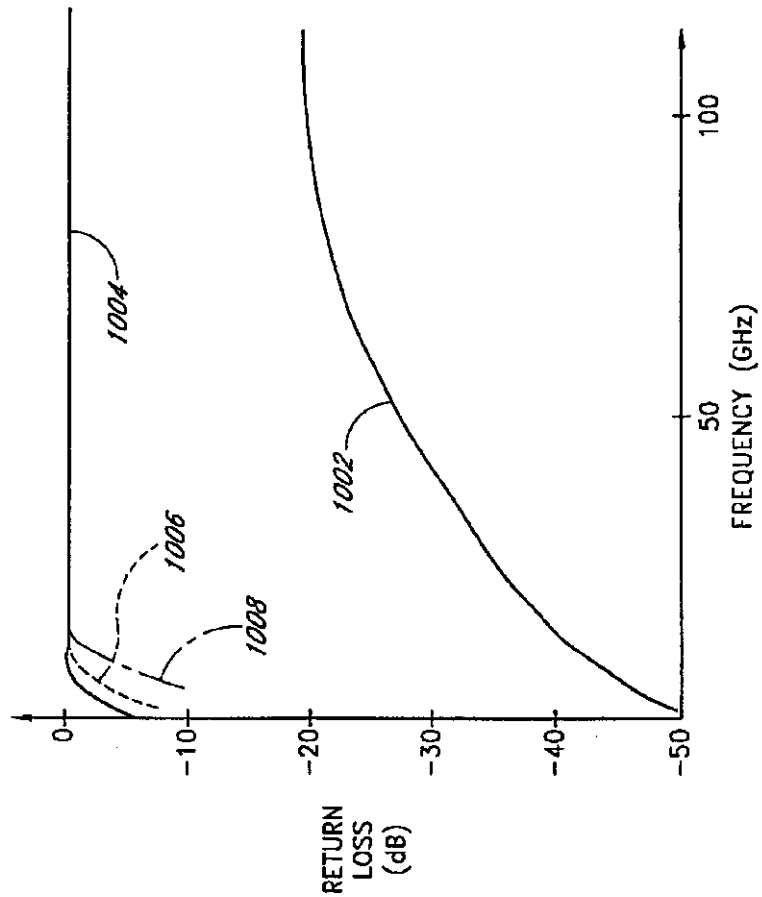

0
-10
-20
-30
-40
-50
RETURN LOSS (dB)
50
100
FREQUENCY (GHz)
1002
1004
1006
1008

FIG. 10A

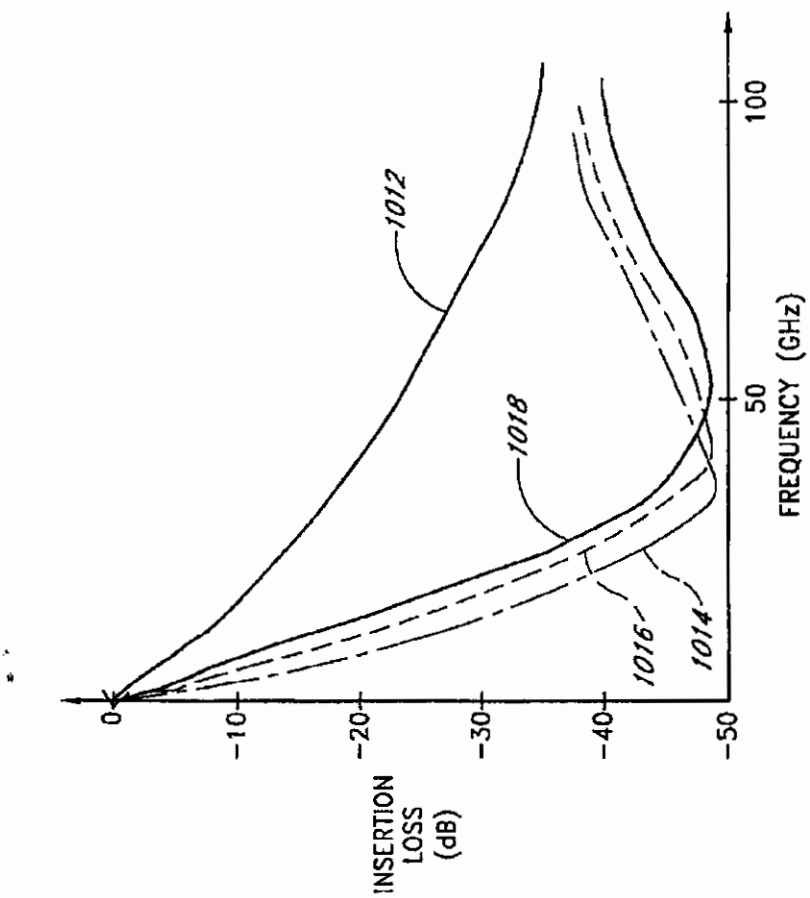

0
-10
-20
-30
-40
-50
INSERTION LOSS (dB)
50
100
FREQUENCY (GHz)
1012
1018
1016
1014

FIG. 10B

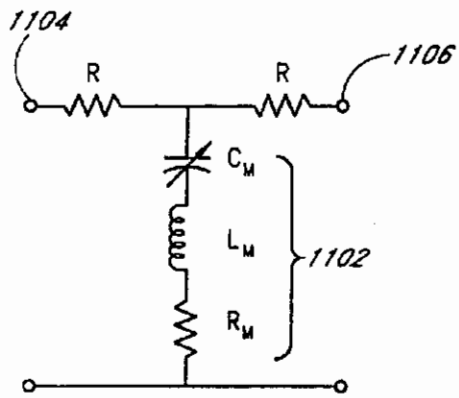


FIG. 11

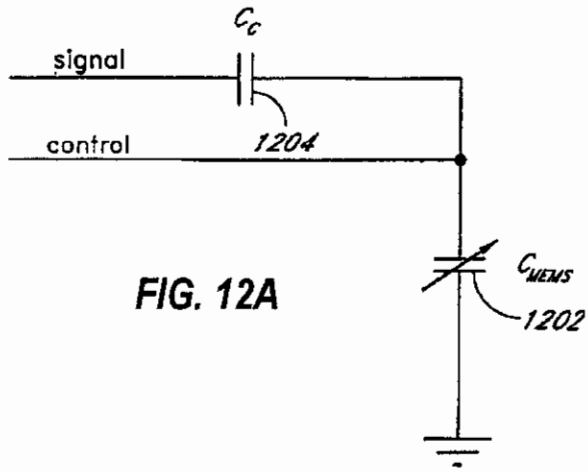


FIG. 12A

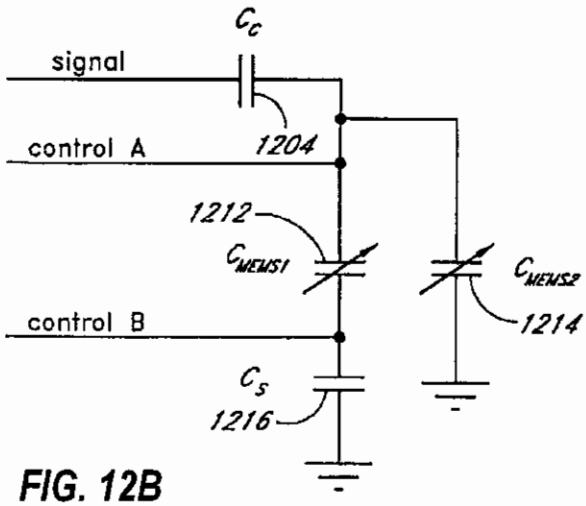


FIG. 12B

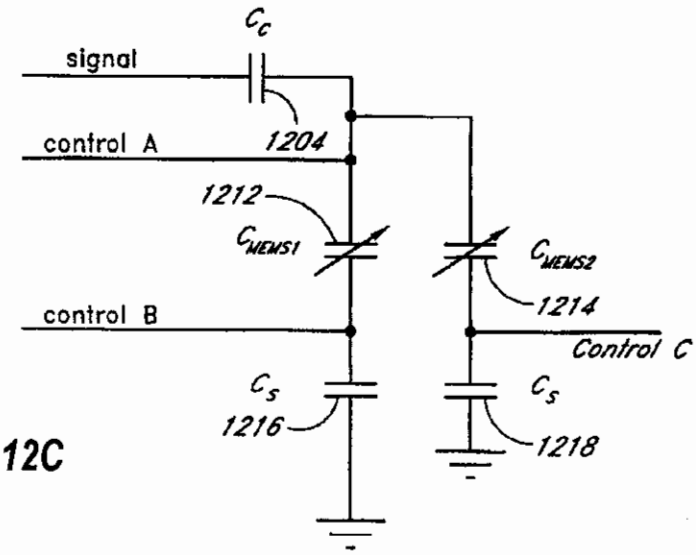


FIG. 12C

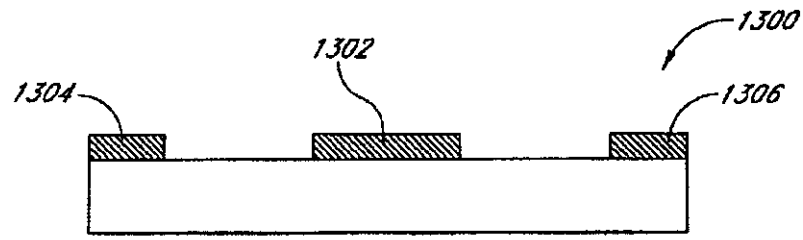


FIG. 13A

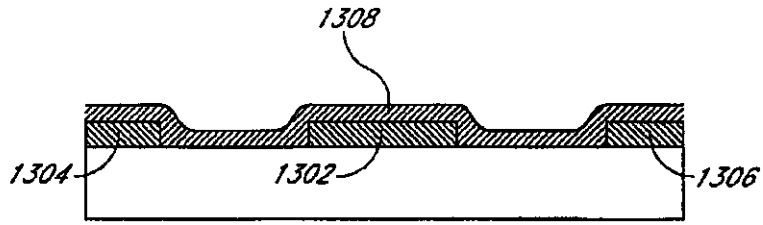


FIG. 13B

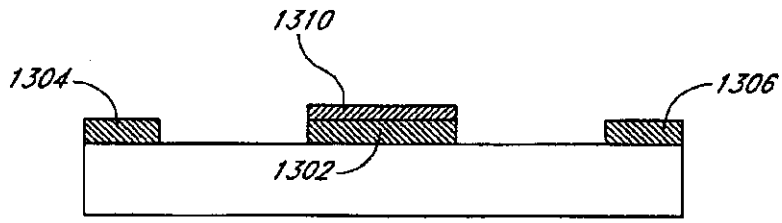


FIG. 13C

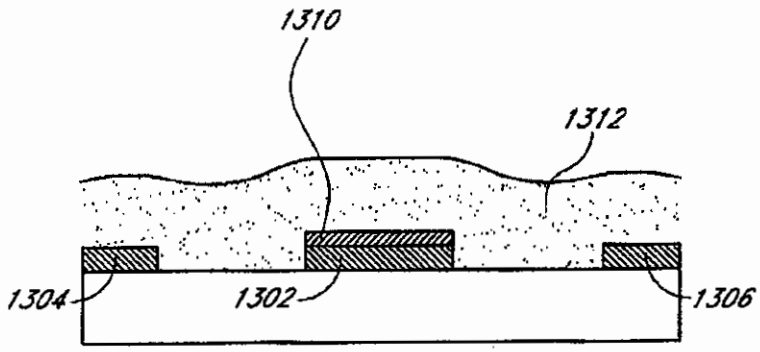


FIG. 13D

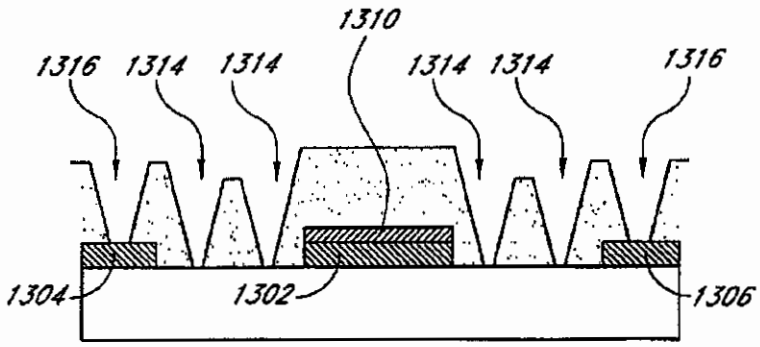


FIG. 13E

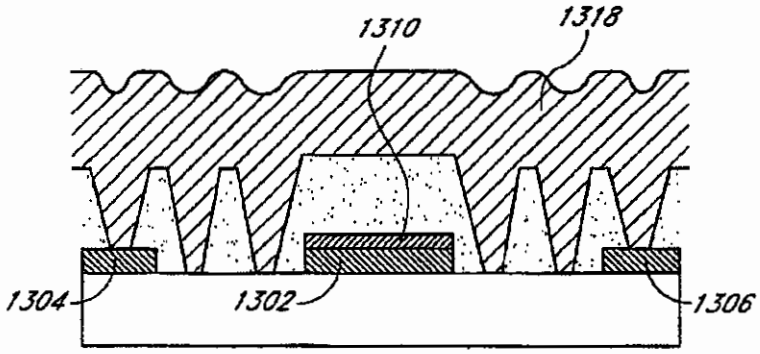


FIG. 13F

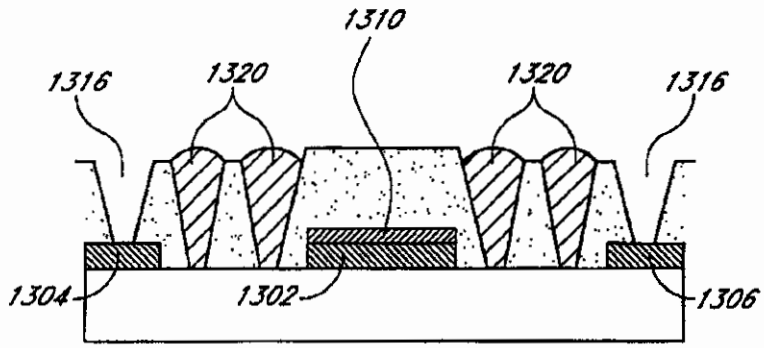


FIG. 13G

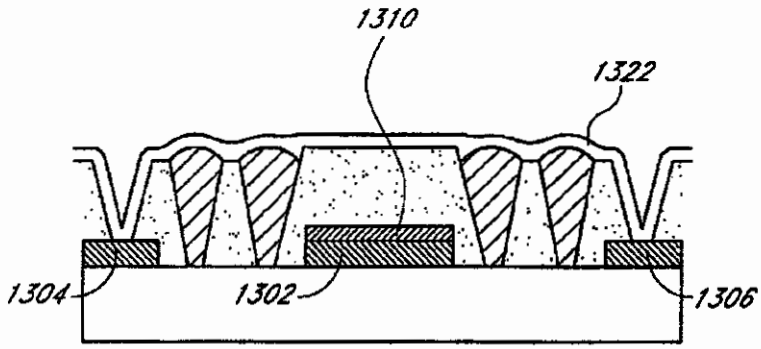


FIG. 13H

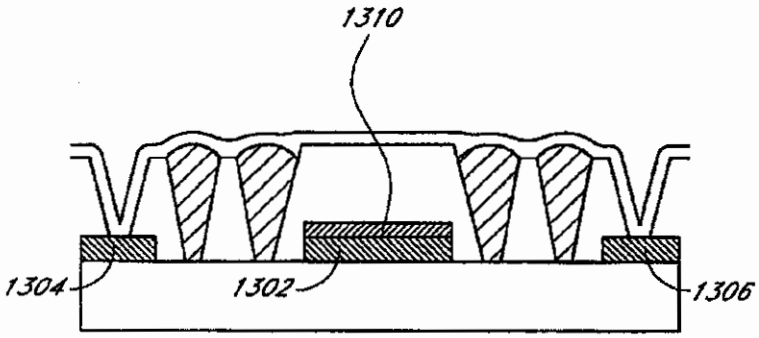


FIG. 13I