CLAIMS

1. A method of processing a semiconductor substrate, the method comprising:

providing a patterned semiconductor substrate;

depositing on the patterned semiconductor substrate a doped silicon oxide film, the film having a thickness of at least 5 μm; and

annealing the doped silicon oxide film to a temperature above the film glass transition temperature.

2. The method of claim 1, wherein the doped silicon oxide film on the substrate exhibits substantially zero as-deposited stress, substantially zero stress shift post-anneal, and substantially zero shrinkage post-anneal.

3. The method of claim 1, wherein the doped silicon oxide film is deposited by a chemical vapor deposition (CVD) process using precursors for silicon oxide and a dopant selected from the group consisting of B, P, Ge, and combinations thereof.

4. The method of claim 1, wherein the patterned semiconductor substrate is a 3D NAND structure having alternating oxide and nitride or polysilicon layers in a staircase pattern, and the doped silicon oxide film is deposited over the staircase pattern.

5. A method of conducting a large area gap fill in fabrication of a 3D NAND structure, the method comprising:

providing a patterned semiconductor substrate comprising a 3D NAND structure having alternating oxide and nitride or polysilicon layers in a staircase pattern;

depositing on the patterned semiconductor substrate over the staircase pattern a doped silicon oxide film, the film having a thickness of at least 5 μm; and

annealing the doped silicon oxide film to a temperature above the film glass transition temperature,

wherein the doped silicon oxide film is deposited by a chemical vapor deposition (CVD) process using precursors for silicon oxide and a dopant selected from the group consisting of B, P, Ge, and combinations thereof.

6. The method of claim 5, wherein the doped silicon oxide film on the substrate exhibits substantially zero as-deposited stress, substantially zero stress shift post-anneal, and substantially zero shrinkage post-anneal.

7. The method of claim 3 or 6, wherein the silicon oxide precursor is tetraethyl orthosilicate (TEOS).

8. The method of claim 3 or 7, wherein the dopant precursors are triethylborate (TEB), triethylphosphate (TEPO) and an organogermanium compound.

9. The method of claim 3 or 5, wherein the CVD is a plasma enhanced CVD (PECVD) process.

10. The method of claim 1 or 8, wherein the doped silicon oxide film has a dopant concentration in the range of up to about 10wt% of the film; or 0.5 to 10%; or 2-5%; or 2.5-3.5%.

11. The method of claim 10, wherein the doped silicon oxide film has a dopant concentration in the range of about 0 to 10wt% of the film B, 0 to 10% P, 0 to 10% Ge.

12. The method of claim 1 or 5, wherein the doped silicon oxide film has a thickness of at least 10 μm.

13. The method of claim 1 or 5, further comprising depositing an undoped silicon oxide capping layer on the doped silicon oxide film.

14. The method of claim 1, 5 or 9, wherein the doped silicon oxide film is deposited at a thickness up to 20 μm by a single-pass deposition.

15. The method of claim 1, 5 or 9, wherein the doped silicon oxide film is deposited at a rate of at least 1 μm per minute.

16. The method of claim 1, 5 or 9, wherein the annealing of the doped silicon oxide film causes reflow of the film to occur.

17. A semiconductor device, comprising:

a 3D NAND structure having alternating oxide and nitride or polysilicon layers in a staircase pattern;

a doped silicon oxide film disposed and annealed on the staircase pattern, the film having a thickness of at least 5 μm;

wherein the doped silicon oxide film is doped with a dopant selected from the group consisting of B, P, Ge, and combinations thereof; and

wherein the doped silicon oxide film disposed and annealed on the staircase pattern exhibits substantially zero as-deposited stress, substantially zero stress shift post-anneal, and substantially zero shrinkage post-anneal.

18. The device of claim 17, wherein the doped silicon oxide film has a dopant concentration in the range of up to about 10wt% of the film; or 0.5 to 10%; or 2-5%; or 2.5-3.5%.

19. The device of claim 18, wherein the doped silicon oxide film has a dopant concentration in the range of about 0 to 10wt% of the film B, 0 to 10% P, 0 to 10% Ge .

20. The device of claim 17, wherein the doped silicon oxide film has a thickness of at least 10 μm.

21. An apparatus for processing substrates, the apparatus comprising:

a process chamber having a chuck;

a gas source connected with the process chambers and associated flow-control hardware; and

substrate handling hardware;

a controller having a processor and a memory, wherein

the processor and the memory are communicatively connected with one another,

the processor is at least operatively connected with the flow-control and substrate handling hardware, and

the memory stores computer-executable instructions for controlling the processor to at least control the flow-control hardware and substrate handling hardware by:

causing a patterned semiconductor substrate to be provided;

causing deposition of a patterned semiconductor substrate disposed in the chamber a doped silicon oxide film having a thickness of at least 5 μm; and

causing annealing of the doped silicon oxide film to a temperature above the film glass transition temperature.

22. The apparatus of claim 21, wherein the process chamber is a PECVD process chamber.

23. The apparatus of claim 21 or 22, wherein the doped silicon oxide film is deposited at a thickness up to 20 μm by a single-pass deposition.

24. The apparatus of claim 21 or 22, wherein the doped silicon oxide film is deposited at a rate of at least 1 μm per minute.

25. The apparatus of claim 21 or 22, wherein the annealing of the doped silicon oxide film causes reflow of the film to occur.

26. An apparatus for processing substrates, the apparatus comprising:

a process chamber having a chuck;

a gas source connected with the process chambers and associated flow-control hardware; and

substrate handling hardware;

a controller having a processor and a memory, wherein

the processor and the memory are communicatively connected with one another,

the processor is at least operatively connected with the flow-control and substrate handling hardware, and

the memory stores computer-executable instructions for controlling the processor to at least control the flow-control hardware and substrate handling hardware by:

causing any of the method of claims 1 to 16 to be performed.