CLAIMS

What is claimed is:

1. A semiconductor structure for triggering asymmetric threshold voltage along a channel of a vertical transport field effect transistor (VTFET), the semiconductor structure comprising:

a first set of fins, each of the first set of fins including a low germanium content layer and a first material layer formed on the low germanium content layer, the low germanium content layer including SiGe with a Ge content of ≤20%, and the first material layer comprising Si or carbon-doped Si;

a second set of fins adjacent to the first set of fins, each of the second set of fins including the low germanium content layer and a high germanium content layer formed on the low germanium content layer, the high germanium content layer including SiGe with a Ge content of ≥40%;

a first high-κ metal gate disposed over the first set of fins; and

a second high-κ metal gate disposed over the second set of fins,

wherein an asymmetric threshold voltage is present along the channel of the VTFET in a region defined at a bottom of the first set of fins and the second set of fins.

2. The semiconductor structure of claim 1, wherein the low germanium content layer has a length in a vertical extending direction of the first set of fins that is 20-50% of a total channel length of the semiconductor structure in the vertical extending direction.

3. The semiconductor structure of claim 1, wherein the second high-κ metal gate is composed of different materials than the first high-κ metal gate.

4. The semiconductor structure of claim 1, wherein a shallow trench isolation (STI) region separates a bottom source region from a bottom drain region.

5. The semiconductor structure of claim 4, wherein top source/drain regions are disposed over exposed top portions of the first set of fins and the second set of fins.

6. The semiconductor structure of claim 5, wherein a metal fill is disposed over the top source/drain regions.

7. The semiconductor structure of claim 6, wherein a bottom spacer is disposed between the first high-κ metal gate and the bottom source/drain regions.

8. A method of fabricating a semiconductor structure for triggering asymmetric threshold voltage along a channel of a vertical transport field effect transistor (VTFET), the method comprising:

forming a first set of fins, each of the first set of fins including a low germanium content layer and a first material layer formed on the low germanium content layer, the low germanium content layer including SiGe with a Ge content of ≤20%, and the first material layer comprising Si or carbon-doped Si;

forming a second set of fins adjacent to the first set of fins, each of the second set of fins including the low germanium content layer and a high germanium content layer formed on the low germanium content layer, the high germanium content layer including SiGe with a Ge content of ≥40%;

forming a first high-κ metal gate over the first set of fins; and

forming a second high-κ metal gate over the second set of fins,

wherein an asymmetric threshold voltage is present along the channel of the VTFET in a region defined at a bottom of the first set of fins and the second set of fins.

9. The method of claim 8, wherein the low germanium content layer has a length in a vertical extending direction of the first set of fins that is 20-50% of a total channel length of the semiconductor structure in the vertical extending direction.

10. The method of claim 8, wherein the second high-κ metal gate is composed of different materials than the first high-κ metal gate.

11. The method of claim 8, wherein a shallow trench isolation (STI) region separates a bottom source region from a bottom drain region.

12. The method of claim 11, further comprising forming top source/drain regions over exposed top portions of the first set of fins and the second set of fins.

13. The method of claim 12, further comprising forming a metal fill over the top source/drain regions.

14. The method of claim 13, further comprising forming a bottom spacer between the first high-κ metal gate and the bottom source/drain regions.