TEST CIRCUIT, TEST APPARATUS AND TEST METHOD THEREOF

TECHNICAL FIELD

[0001] The embodiments of the present application relate to the technical field of memory, and in particular, to a test circuit, a test apparatus and a test method thereof.

BACKGROUND

[0002] A memory is a device used to store data. The memory usually includes multiple storage arrays, and each storage array includes multiple storage units. Each storage unit, as the basic unit structure of data storage, has the function of data storage.

[0003] When reading and writing the memory, it needs to be controlled by a pulse signal. Exemplarily, a pulse signal may be used to control the on and off of a transistor pair connected to the word line. Specifically, when the pulse signal is valid, the storage unit performs a read or write operation, and when the pulse signal becomes invalid, the storage unit maintains the original data. With the continuous increase in the requirements for the read and write speed of the memory, it is necessary to further increase the transmission frequency of the pulse signal and reduce the pulse width. In order to ensure the reliability of the pulse signal, it is necessary to test the pulse width through a test circuit to ensure that the generated pulse signal is the same as the designed signal. However, with the continuous narrowing of the pulse width, higher requirements are put forward for the test circuit and test device for a pulse width, and the present test circuit can no longer accurately test the narrowing pulse width.

SUMMARY

[0005] In an aspect of this application, a test circuit is provided, which includes a signal processing module and a sampling module.

[0006] The signal processing module is used to receive a pulse signal to be tested and output a processing signal under control of a control signal.

[0007] The sampling module is connected to an output terminal of the signal processing module, and is used to receive the processing signal and generate a sampling signal according to the processing signal.

[0008] The sampling signal includes a first sampling pulse and a second sampling pulse, the first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to a pulse width of the pulse signal.

[0009] In another aspect of this application, a testing apparatus is provided, which includes the test circuit as described above, and an analysis module.

[0010] The analysis module is connected to the sampling module and is used to obtain the pulse width of the pulse signal according to the first sampling pulse and the second sampling pulse.

[0011] In another aspect of the present application, a test method is provided, which is based on the above-mentioned test device and includes the following operations.

[0012] A pulse signal to be tested is received.

[0013] A processing signal is output under control of a control signal.

[0014] A sampling signal is generated according to the processing signal, the sampling signal including a first sampling pulse and a second sampling pulse.

[0015] The pulse width of the pulse signal is obtained according to the first sampling pulse and the second sampling pulse.

[0016] The first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to the pulse width of the pulse signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] In order to better describe and illustrate the embodiments of the application, one or more drawings may be referred to. However, the additional details or examples used to describe the drawings should not be considered as the limitation on the scope of any of the application, the currently described embodiments or the implementation modes of the present application.

[0018] FIG. 1 is a schematic structural diagram of a test circuit of a first embodiment;

[0019] FIG. 2 is an exemplary signal sequence diagram corresponding to the embodiment of FIG. 1;

[0020] FIG. 3 is another exemplary signal sequence diagram corresponding to the embodiment of FIG. 1;

[0021] FIG. 4 is yet another exemplary signal sequence diagram corresponding to the embodiment of FIG. 1;

[0022] FIG. 5 is a schematic structural diagram of a test circuit of a second embodiment;

[0023] FIG. 6 is an exemplary signal sequence diagram corresponding to the embodiment of FIG. 5;

[0024] FIG. 7 is a schematic structural diagram of a test circuit of a third embodiment;

[0025] FIG. 8 is a schematic structural diagram of a test circuit of a fourth embodiment;

[0026] FIG. 9 is an exemplary signal sequence diagram corresponding to the

embodiment of FIG. 8;

[0027] FIG. 10 is a schematic structural diagram of a test circuit of a fifth embodiment;

[0028] FIG. 11 is a schematic structural diagram of a test circuit of a sixth embodiment;

[0029] FIG. 12 is a schematic structural diagram of a test device according to an embodiment;

[0030] Fig. 13 is a flowchart of a test method according to an embodiment.

DETAILED DESCRIPTION

[0031] In order to facilitate understanding of the embodiments of the present application, the embodiments of the present application will be described in a more comprehensive manner with reference to related drawings. Some embodiments of the present application are shown in the accompanying drawings. However, the embodiments of the present application can be implemented in many different forms and are not limited to the embodiments described herein. On the contrary, these embodiments are provided to make the disclosure of the embodiments of the present application more thorough and comprehensive.

[0032] Unless otherwise defined, all technical and scientific terms used herein have the same meaning as commonly understood by those skilled in the technical field belonging to the embodiments of the present application. The terms used in the description of the embodiments of the present application herein are only for the purpose of describing specific embodiments, and are not intended to limit the embodiments of the present application. The term "and/or" as may be used herein includes any and all combinations of one or more related listed items.

[0033] In the description of the embodiments of the present application, it needs to be understood that the terms "upper", "lower", "vertical", "horizontal", "inner", "outer", etc., are based on the method or positional relationship shown in the

drawings, are only for convenience of describing the embodiments of the present application and simplifying the description, rather than indicating or implying that pointed device or element must have a specific orientation, be constructed and operated in a specific orientation, and therefore cannot be understood as the limitation to the embodiments of the present application.

[0034] FIG. 1 is schematic structural diagram of a test circuit 10 of a first embodiment. Referring to FIG. 1, in this embodiment, the test circuit 10 includes a signal processing module 100 and a sampling module 200.

[0035] A pulse signal to be tested is generated by a pulse generator 30 and is divided into at least two channels: one pulse signal is transmitted to the test circuit 10 for testing, and the other pulse signal is transmitted to the storage array to control data reading and writing of the storage array. In the embodiment of the present application, the pulse signal includes multiple pulses, and the pulse width refers to the duration of the high level of each pulse, that is, the time interval between the rising edge time and the falling edge time of a pulse is the pulse width.

[0036] The signal processing module 100 is configured to receive a pulse signal to be tested, and output a processing signal under control of the control signal, and the processing signal is the pulse signal or the inverted pulse signal in time division.

[0037] The processing signal is the pulse signal or the inverted pulse signal in time division means that the waveform of the processing signal coincides with the waveform of the pulse signal during part of the time period of the processing signal, and the waveform of the processing signal coincides with the waveform of the inverted pulse signal during the remaining time period of the processing signal. In this embodiment, the processing signal is transmitted to the clock driving terminal of the sampling module 200 to serve as the clock for the sampling of the signal input by the sampling module 200. Specifically, the signal input by the sampling module 200 is sampled according to edges of the processing signal.

[0038] It can be understood that one sampling module 200 usually only samples at one type of edge, that is, only rising edges or only falling edges. Therefore, if the sampling module 200 is required to sample at different edges, multiple flip-flops and other structures with complex structure need to be provided in the sampling module 200, which will result in more complex internal structure and control circuit of the sampling module 200. In this embodiment, by controlling the processing signal to be a pulse signal or an inverted pulse signal in time division, the sampling module 200 may only sample at one type of edges, that is, the pulse signal is inverted to achieve sampling at different edges. Exemplarily, if the sampling module 200 performs sampling at the rising edges, and part of the edges of the sampling signal is generated based on the falling edges of the pulse signal, a target falling edge of the pulse signal may be inverted to convert the falling edge of the pulse signal into the rising edge of the processing signal, simple and accurate sampling of the sampling module 200 can be implemented, thereby simplifying the internal structure of the sampling module 200. Moreover, compared with the sampling module 200 with a structure of multiple flip-flops, the control logic and circuit required for implementation of the time-divisional control of the inverting function are simpler. Therefore, the signal processing module 100 of this embodiment further simplifies the overall test circuit structure of the test circuit 10.

[0039] The sampling module 200 is connected to the output terminal of the signal processing module 100, and is configured to receive the processing signal and generate a sampling signal according to the processing signal. The sampling signal includes a first sampling pulse and a second sampling pulse. The first sampling pulse and the second sampling pulse have a pulse width difference. The pulse width difference is equal to the pulse width of the pulse signal. The pulse width difference refers to the difference between the pulse width of the first sampling pulse and the pulse width of the second sampling pulse, and the sampling module

200 generates a sampling signal in response to edges of the processing signal. Therefore, each rising edge in the sampling signal and each falling edge corresponds to an edge in the processing signal, that is, each rising edge and each falling edge in the sampling signal also corresponds to an edge in the pulse signal.

[0040] In this embodiment, the test circuit 10 includes a signal processing module 100 and a sampling module 200. The signal processing module is configured to receive a pulse signal to be tested and output the processing signal under control of a control signal, and the processing signal is the pulse signal or the inverted pulse signal in time division. The sampling module 200 is connected to the output terminal of the signal processing module 100, and is configured to receive the processing signal and generate a sampling signal according to the processing signal. The sampling signal includes a first sampling pulse and a second sampling pulse, the first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to the pulse width of the pulse signal. In this embodiment, the input pulse signal is processed by the signal processing module 100, and the sampling module 200 with a simpler structure may be used to sample at different edges of the pulse signal, thereby simplifying the hardware structure of the test circuit 10 and further samples the processing signal by means of the sampling module 200 to generate the first sampling pulse and the second sampling pulse, and the pulse width may be obtained through the first sampling pulse and the second sampling pulse, that is, a test circuit 10 with higher test accuracy is realized.

[0041] In some embodiments, the sampling module 200 may be used to generate the first sampling pulse in response to the same edge of the first two pulses at time sequence, and to generate the second sampling pulse in response to the different edges of the last two pulses at time sequence. FIG. 2 is an exemplary signal sequence diagram corresponding to the embodiment of FIG. 1. Referring to FIG. 1, in this embodiment, the pulse signal includes four pulses, and the sampling

module 200 generates a corresponding edge in responds to one of the rising edge and the falling edge of each pulse. Specifically, the first rising edge of the sampling signal is generated in response to the falling edge of the first pulse, the first falling edge of the sampling signal is generated in response to the rising edge of the second pulse, the second rising edge of the sampling signal is generated in response to the rising edge of the third pulse, and the second falling edge of the sampling signal is generated in response to the rising edge of the fourth pulse. The time interval between the first rising edge moment t1 and the first falling edge moment t2 is the width A of the first sampling pulse, and the time interval between the second rising edge moment t3 and the second falling edge moment t4 is the width B of the second sampling pulse. Therefore, based on the test circuit 10 of this embodiment, the pulse width of the input pulse signal can be obtained by only sampling one edge of each pulse, thereby reducing the sampling difficulty of the sampling module 200, and thus improving the test accuracy of the test circuit 10.

[0042] In other embodiments, as shown in FIG. 3, the second sampling pulse may be generated in response to the falling edge of the third pulse and the falling edge of the fourth pulse. Moreover, as shown in FIG. 4, the first sampling pulse may be generated in response to three or more pulses, and the second sampling pulse may be generated in response to other three or more pulses. It is also possible that the pulse signal includes five or more pulses, the first sampling pulse is generated in response to the first pulse and the second pulse, and the second sampling pulse is generated in response to the fourth pulse and the fifth pulse. It should be noted that the sampling signal generation methods in the embodiments of FIG. 2 to 4 are only used for exemplary description, and are not used to limit the protection scope of the present application, as long as the difference between pulse width of the first sampling pulse and the second sampling pulse is equal to the pulse width of the pulse signal to be tested, it belongs to the protection scope of the present application.

[0043] FIG. 5 is schematic structural diagram of a test circuit 10 of a second embodiment. Referring to FIG. 5, in this embodiment, the sampling module 200 includes a first temporary storage unit 210. The clock driving terminal of the first temporary storage unit 210 is connected to the signal processing module 100, and the first temporary storage unit 210 is used to sample the signal to be sampled in response to the processing signal to generate a first temporary storage signal, and the edge of the sampling signal corresponds to the edge of the first temporary storage signal. The input terminal of the first temporary storage unit 210 is connected to the signal source to be sampled, and the signal source to be sampled is used to output the signal to be sampled, exemplarily, the signal to be sampled may be a signal that is switched between a high level and a low level at a preset time interval.

[0044] FIG. 6 is an exemplary signal sequence diagram corresponding to the embodiment of FIG. 5. Referring to FIG. 5, in this embodiment, the pulse signal may include four pulses adjacent in timing sequence. The signal processing module 100 is configured to, in response to a control signal, invert the first pulse in the timing sequence in the pulse signal, without inverting the remaining pulses. The sampling module 200 is used to generate the first sampling pulse in response to the first two pulses in timing sequence, and to generate the second sampling pulse in response to the last two pulses in time sequence. Specifically, the period of the signal to be sampled is twice the period of the pulse signal, and the edge of the signal to be sampled is staggered from the edge of the pulse signal, so as to ensure the accuracy of sampling the signal to be sampled according to the edge of the processing signal. It can be understood that accurate sampling can be performed only when the signal to be sampled corresponding to the edge of the processing signal is in a stable state. Therefore, in this embodiment, the test circuit 10 requires a lower time sequence accuracy of the signal to be sampled, that is, the time sequence window is larger, and the time sequence reliability is higher.

[0045] Further, the first temporary storage unit 210 includes one or more of a flip-flop, a latch, and a register. In the embodiment shown in FIG. 5, the first temporary storage unit 210 includes a D flip-flop. The clock driving terminal of the D flip-flop is connected to the output terminal of the signal processing module 100. The input terminal of the D flip-flop is connected to the signal to be sampled, and the signal output from the output terminal of the D flip-flop may be used as a sampling signal. Furthermore, the set terminal or the reset terminal of the D flip-flop may also be connected to an external circuit, so that the initial state of the D flip-flop is determined by setting or resetting, thereby improving the reliability of the test circuit 10. In this embodiment, the first temporary storage unit 210 may sample and latch the edge of the processing signal, so as to accurately and stably output the sampled signal.

[0046] FIG. 7 is a schematic structural diagram of a test circuit 10 of a third embodiment. Referring to FIG. 7, in this embodiment, the sampling module 200 further includes a first inverter 220, which forms a feedback loop together with the first temporary storage unit 210. The feedback loop is configured to generate a feedback signal in response to the processing signal, and the edge of the feedback signal corresponds to the edge of the processing signal. It can be understood that, in the foregoing embodiments, the sampling signal may be output only through the signal source to be sampled from the external device. In this embodiment, by forming a feedback loop, the signal at the input terminal of the first temporary storage unit 210 can follow the feedback signal outputted by the first inverter 220, thereby simplifying the test circuit 10 and improving the flexibility and reliability of the test circuit 10.

[0047] Specifically, the input terminal of the first inverter 220 is connected to the output terminal of the first temporary storage unit 210, and the output terminal of the first inverter 220 is connected to the input terminal of the first temporary storage unit 210, and the first inverter 220 is configured to invert the first

temporary storage signal to generate a feedback signal. Exemplarily, after the rising edge of the current processing signal cycle arrives, the first temporary storage signal outputted by the first temporary storage unit 210 is in the 0 state, and the feedback signal outputted by the inverted output of the first inverter 220 is in the 1 state, then the signal at the input terminal of the first temporary storage unit 210 is also in the 1 state, after the rising edge of the next processing signal cycle arrives, the first temporary storage signal will switch to the 1 state, thereby automatically updating the feedback signal inputted from the input terminal of the first temporary storage unit 210, that is, the test circuit 10 having a simpler structure and capable of automatic sampling is realized.

[0048] With continued reference to FIG. 7, in an embodiment, the sampling module 200 further includes a second inverter 230. An input terminal of the second inverter 230 is connected to an output terminal of the first inverter 220. The second inverter 230 is configured to receive the feedback signal and generate the sampling signal according to the feedback signal. By setting the second inverter 230, the signal output by the sampling module 200 can coincide with the signal output by the first temporary storage unit 210.

[0049] FIG. 8 is a schematic structural diagram of a test circuit 10 of a fourth embodiment. Referring to FIG. 8, in this embodiment, the test circuit 10 further includes a control module 300, which is connected to the sampling module 200 and the signal processing module 100 respectively, and is configured to generate the control signal in response to the sampling signal. The edge of the control signal corresponds to the edge of the sampling signal.

[0050] Specifically, the control module 300 may generate a responsive control signal according to the signal outputted by the sampling module 200, so as to control the output signal of the signal processing module 100, that is, control the processing signal outputted by the signal processing module 100 according to the electrical

level state of the control signal. For example, FIG. 9 is an exemplary signal sequence diagram corresponding to the embodiment of FIG. 8. Referring to FIG. 9, in this embodiment, when the electrical level state of the control signal is high, the signal processing module 100 outputs a pulse signal; when the electrical level state of the control signal is low, the signal processing module 100 outputs an inverted pulse signal.

[0051] With continued reference to FIG. 8, the control module 300 may include a second temporary storage unit 310. The clock driving terminal of the second temporary storage unit 310 is connected to the output terminal of the sampling module 200, and the input terminal of the second temporary storage unit 310 is connected to a preset level signal generator to obtain a preset level signal, and the output terminal of the second temporary storage unit 310 is connected to the signal processing module 100, and the second temporary storage unit 310 is configured to, in response to the sampling signal, sample the preset level signal to generate a second temporary storage signal. The edge of the control signal corresponds to the edge of the second temporary storage signal. That is, the preset level signal generator outputs a signal in a constant level state, for example, a high level signal. Before the sampling module 200 runs, the second temporary storage unit 310 may be reset to make the second temporary storage unit 310 outputs in the 0 state, the enable signal of the reset terminal is disconnected at the target time, and the high level signal output by the preset level signal generator is sampled according to the sampling signal, so that the state of the control signal Q output by the second temporary storage unit 310 is switched to the 1 state, thereby realizing the purpose of inverting part of the pulse signal and keeping the state of the remaining pulse signal. The target moment may be controlled through the number of inverters connected to the output terminal of the first temporary storage unit 210.

[0052] FIG. 10 is a schematic structural diagram of a test circuit 10 of a fifth embodiment. Referring to FIG. 10, in this embodiment, the control module 300

further includes a third inverter 320. The input terminal of the third inverter 320 is connected to the output terminal of the second temporary storage unit 310. The third inverter 320 is used to receive the second temporary storage signal and generate the control signal according to the second temporary storage signal. In this embodiment, a control signal Q and a control signal QN may be generated by the third inverter 320, that is, the signal processing module 100 may be controlled based on the two control signals, thereby improving the control reliability of the signal processing module 100.

[0053] FIG. 11 is a schematic structural diagram of a test circuit 10 of a sixth embodiment. Referring to FIG. 11, in this embodiment, the signal processing module 100 includes a fourth inverter 110 and a multiplexer 120. The first input terminal of the multiplexer 120 is connected to the output terminal of the fourth inverter 110. The second input terminal of the multiplexer 120 is connected to the pulse signal. The multiplexer 120 is configured to receive the control signal, and under the control of the control signal, select to turn on the path between the first input terminal and the output terminal or the path between the second input terminal and the output terminals. It should be noted that the structure of the multiplexer 120 is not limited to the structure in the embodiment shown in the figure, and other multiplexers 120 that can realize the multiplexing function also belong to the protection scope of the present application.

[0054] Fig. 12 is a schematic structural diagram of a test device according to an embodiment. Referring to Fig. 12, in this embodiment, the test device includes: the above-mentioned test circuit 10; an analysis module 20, which is connected to the sampling module 200 and is used to obtain the pulse width of the pulse signal according to the first sampling pulse and the second sampling pulse. The specific limitation of the test circuit 10 may refer to the above limitation, which will not be repeated here. In this embodiment, a test device with accurate pulse width test is realized by the test circuit 10 and the analysis module 20.

[0055] FIG. 13 is a flowchart of a test method of an embodiment. The test method of this embodiment is based on the above-mentioned test device. Referring to FIG. 13, in this embodiment, the method includes S100 to S400.

[0056] At S100, a pulse signal to be tested is received.

[0057] At S200, a processing signal is output under control of a control signal.

[0058] At S300, a sampling signal is generated according to the processing signal, the sampling signal including a first sampling pulse and a second sampling pulse.

[0059] At S400, the pulse width of the pulse signal is obtained according to the first sampling pulse and the second sampling pulse.

[0060] It should be noted that the specific limitation on the test method may refer to the above limitation on the test device, which will not be repeated here. It should be understood that although the various steps in the flowchart of FIG. 13 are displayed in an order as indicated by the arrows, these steps are not necessarily performed in turn according to the order as indicated by the arrows. Unless specifically stated herein, the execution order of these steps is not strictly limited, and these steps can be executed in other orders. Moreover, at least part of the steps in FIG. 13 may include multiple sub-steps or multiple stages, these sub-steps or stages are not necessarily executed at the same moment, but can be executed at different moments, the execution of these sub-steps or stages is not necessarily performed sequentially, but may be performed in turn or alternatingly with at least part of other steps or sub-steps or stages of other steps.

[0061] The technical features of the above-mentioned embodiments can be combined arbitrarily, in order to make the description concise, all possible combinations of the various technical features in the above-mentioned embodiments are not described, however, as long as there is no contradiction in the combination of these technical features, it should be considered as the scope of this specification.

[0062] The above mentioned embodiments only express several implementation manners of the embodiments of the present application, and the description is relatively specific and detailed, but it should not be understood as a limitation on the scope of the application. It should be noted that for those of ordinary skill in this art, without departing from the concept of the embodiments of the present application, several modifications and improvements can be made, and these all fall within the protection scope of the embodiments of the present application. Therefore, the scope of protection of the patent for the embodiments of this application shall be subject to the appended claims.

CLAIMS:

1. A test circuit, comprising:

a signal processing module, which is configured to receive a pulse signal to be tested and output a processing signal under control of a control signal;

a sampling module, which is connected to an output terminal of the signal processing module and is configured to receive the processing signal and generate a sampling signal according to the processing signal;

wherein the sampling signal comprises a first sampling pulse and a second sampling pulse, the first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to a pulse width of the pulse signal.

2. The test circuit of claim 1, wherein the sampling module comprises:

a first temporary storage unit, wherein a clock driving terminal of the first temporary storage unit is connected to the signal processing module, and the first temporary storage unit is configured to sample the signal to be sampled in response to the processing signal, to generate a first temporary storage signal, and an edge of the sampling signal corresponds to an edge of the first temporary storage signal.

3. The test circuit of claim 2, wherein the first temporary storage unit comprises one or more of a flip-flop, a latch and a register.

4. The test circuit of claim 2, wherein the sampling module further comprises:

a first inverter, wherein the first inverter and the first temporary storage unit jointly forms a feedback loop, the feedback loop is configured to generate a feedback signal in response to the processing signal, and an edge of the feedback signal corresponds to an edge of the processing signal.

5. The test circuit of claim 4, wherein an input terminal of the first inverter is connected to an output terminal of the first temporary storage unit, an output terminal

of the first inverter is connected to an input terminal of the first temporary storage unit, and the first inverter is configured to invert the first temporary storage signal to generate the feedback signal.

6. The test circuit of claim 5, wherein the sampling module further comprises:

a second inverter, wherein an input terminal of the second inverter is connected to the output terminal of the first inverter, the second inverter is configured to receive the feedback signal and generate the sampling signal according to the feedback signal.

7. The test circuit of claim 1, wherein the pulse signal comprises four pulses adjacent at time sequence, and the signal processing module is configured to, in response to the control signal, invert a first pulse at time sequence in the pulse signal without inverting remaining pulses;

wherein the sampling module is configured to generate the first sampling pulse in response to first two pulses at timing sequence, and generate the second sampling pulse in response to last two pulses at timing sequence.

8. The test circuit of claim 7, wherein the sampling module is configured to generate the first sampling pulse in response to a same edge of the first two pulses at timing sequence, and generate the second sampling pulse in response to different edges of the last two pulses at timing sequence.

9. The test circuit of claim 1, further comprising:

a control module, which is connected to the sampling module and the signal processing module respectively, and is configured to generate the control signal in response to the sampling signal, wherein an edge of the control signal corresponds to an edge of the sampling signal.

10. The test circuit of claim 9, wherein the control module comprising:

a second temporary storage unit, wherein a clock driving terminal of the second temporary storage unit is connected to an output terminal of the sampling module, an

input terminal of the second temporary storage unit is connected to a preset level signal, and an output terminal of the second temporary storage unit is connected to the signal processing module, the second temporary storage unit is configured to sample the preset level signal in response to the sampling signal, to generate a second temporary storage signal, and an edge of the control signal corresponds to an edge of the second temporary storage signal.

11. The test circuit of claim 10, wherein the control module further comprises:

a third inverter, wherein an input terminal of the third inverter is connected to the output terminal of the second temporary storage unit, the third inverter is configured to receive the second temporary storage signal and generate the control signal according to the second temporary storage signal.

12. A test apparatus, comprising:

a test circuit according to any one of claims 1 to 11;

an analysis module, which is connected to the sampling module and is configured to obtain a pulse width of the pulse signal according to the first sampling pulse and the second sampling pulse.

13. A test method, based on the test device according to claim 12, wherein the method comprising:

receiving a pulse signal to be tested;

outputting a processing signal under a control signal;

generating a sampling signal according to the processing signal, wherein the sampling signal comprises a first sampling pulse and a second sampling pulse;

obtaining a pulse width of the pulse signal according to the first sampling pulse and the second sampling pulse;

wherein the first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to the pulse width of the pulse signal.