

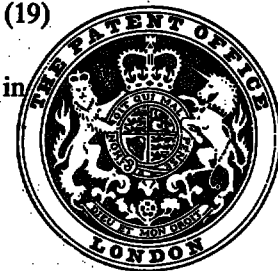
PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO VOLTAGE BOOSTERS

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates to voltage boosters and has for its object to provide improved boosters which may be made of relatively very small size and which are such as to lend themselves to integrated circuit construction better than do known comparable boosters. These objects are achieved by providing boosters the circuit elements of which consist almost entirely of MOS-FET's, the only elements which are not MOS-FETs being condensers.

In conventional voltage boosters as at present commonly employed, the boosting circuits comprise diodes and condensers. Such circuits are very difficult to embody in integrated circuit structures. Such conventional boosters therefore require, for their accommodation, an amount of space which makes them unsuitable for use in the circuitry of electronic watches, pocket calculators and other electronic devices in which there is very little space available. Moreover the cost of the transformers and diodes used in such conventional boosters is a serious disadvantage in an electronic watch or calculator.

As will be seen later the invention provides improved voltage boosters which avoid the defects and disadvantages of the conventional voltage boosters above referred to. A further advantage of the invention - again as will be seen later - is that it employs booster circuits which can be connected in effective cascade to enable a required high value of voltage boosting ratio to be obtained over all and that such cascaded circuits can readily be accommo-

dated on the same chip in an integrated circuit structure.

According to this invention there is provided a voltage booster including as its first boosting stage a circuit comprising two series connected complementary MOS-FETs at least one of which has its gate connected to one of two pulse input terminals of the booster and which are together in series with a condenser between said pulse input terminals, said complementary MOS-FETs having a common drain connection connected to the gate of an N-type MOS-FET, the connection point of the series-connected complementary MOS-FETs with said condenser constituting an output terminal of said first voltage boosting stage and being connected to the source of said N type MOS-FET the drain of which is connected to a point of anchored potential. There may be a plurality of similar voltage booster stages, each as just broadly described, each of which, except the first, has pulse input terminals connected to receive output from the preceding stage as its pulse input.

In one form of embodiment of the invention the first (or only) stage comprises a P type MOS-FET having its source connected to a point of relatively high fixed potential and its gate connected to one of two pulse input terminals; a first N type MOS-FET having its drain connected to a point of relatively low fixed potential and its gate connected to the drain of said P type MOS-FET; a second N type MOS-FET having its source connected to the source of said first N type MOS-FET, its drain connected to the drain of said P type MOS-FET, and its gate connected to the gate of said P type MOS-FET; and a condenser one side of which is connected to the other of the pulse input terminals and the other side of which is connected to the common connection point of the sources of said first and second N type MOS-FETs.

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In another form of embodiment of the invention the first (or only) stage comprises a P-type MOS-FET having its source connected to a point of relatively high fixed potential and its gate connected to a pulse input terminal; a first N type MOS-FET having its drain connected to a point of relatively low fixed potential and its gate connected to the drain of said P type MOS-FET; a second N type MOS-FET having its source connected to the source of said first N type MOS-FET, its drain connected to the drain of said P type MOS-FET, and its gate connected to said point of relatively low fixed potential; and a condenser one side of which is connected to said pulse input terminal through an inverter and the other side of which is connected to the common connection point of the sources of said first and second N type MOS-FETS. This first stage circuit may be followed by a second stage also including a P type MOS-FET and first and second N type MOS-FETS interconnected similarly to the corresponding circuit elements in the first stage and wherein there is a connection between the output terminal of the first stage and the gate of the P type MOS-FET in the second stage, a connection between the drain of the first N type MOS-FET in said second stage and the source of the first N type MOS-FET in the first stage, a connection between the source of the P type MOS-FET in said second stage and said point of relatively high fixed potential; and a condenser connected between said point of relatively high fixed potential and the common source connection of the first and second N type MOS-FETS in the second stage.

In the preferred embodiments of the invention every circuit element which is not a MOS-FET is a condenser.

Preferably also circuits in accordance with the invention are embodied in integrated circuit structures.

The invention is illustrated in the accompanying drawings in which

Figures 1, 3, 4 and 6 show diagrammatically different embodiments of the invention, and

Figures 2, 5 and 7 are graphical wave form figures explanatory of the operation of the embodiments shown in Figures 1, 4 and 6 respectively.

Figure 8 is a simplified block diagram of an electronic timepiece incorporating a voltage booster in accordance with the invention in its circuitry.

The embodiment of the invention shown in Figure 1 is a booster consisting of two boosting circuits or units in the blocks indicated by the references 1 and 2.

Referring to Figure 1 there is shown a voltage booster having a first stage 1 which includes a P-type MOS-FET 3 and an

N-type MOS-FET 4 having their gate electrodes connected together and their drain electrodes also connected together. Their common gate connection is connected to a terminal 13 and their common drain connection is connected to the gate electrode of a further N type MOS-FET 5 the drain electrode of which is connected to a terminal 14.

The source electrode of the MOS-FET 3 is connected to a terminal 16, and the source electrodes of the MOS-FETS 4 and 5 are connected together and to one side 18 of a first condenser 6 the other side of which is connected to a terminal 15.

There is a second stage 2 including a P type MOS-FET 8 and an N type MOS-FET 9 having their gate-electrodes connected together and their drain electrodes connected together. Their common gate connection is connected to the connecting point 7 of the drain electrodes of the MOS-FETS 3 and 4 in the boosting unit 1. The common drain connection of the MOS-FETS 8 and 9 is connected to the gate electrode of another N type MOS-FET 10.

The source electrode of the MOS-FET 8 is connected like the source electrode of the MOS-FET 3 in stage 1, to the terminal 16, and the source electrodes of the MOS-FETS 9 and 10 are connected together and to a terminal 17 and to one side of a second condenser 11 the other side of which is connected to a terminal 19.

The terminals 16 and 19 are connected to the high voltage point of a power supply source, and the terminal 14 is connected to a low voltage point of said source. The terminal 13 is the terminal to which an input signal for driving the boosting circuit arrangement is applied. This input signal may be, for example, a signal taken from a frequency divider dividing the oscillating output from a quartz or other time standard oscillator in an electronic timepiece.

The terminal 15 is a terminal to which is applied a signal in phase opposition to the signal applied to terminal 13.

Terminal 17 is the output terminal of the whole boosting circuit arrangement and the required boosted output appears at said output terminal 17.

To quote practical voltage figures, by way of example only, the power supply source might be a 1 volt source and the various applied terminal voltages might be 0 volts at terminals 16 and 19 and -1 volt at terminal 14. The voltage at terminal 17 is caused to be about -IV by reason of the charge in the condenser 11 and, by reason of the MOS-FETS 5 and 10 acting as N type parasitic diodes, the voltage at point 18 is also caused to be about -1 volt.

If the voltage at the input terminal 13 is -1 volt and that at the input terminal 15

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becomes 0 volt, the MOS-FET 3 will become ON, its threshold voltage VTP is less than 1 volt, and the MOS-FET 4 becomes OFF when its source voltage is equal to its gate voltage. Therefore, in these circumstances, the voltage at the connecting point 7 becomes 0 volt, the MOS-FET 5 will become ON if its threshold voltage VTN is lower than 1 volt, the MOS-FET 8 becomes OFF and the MOS-FET 9 becomes ON. The source and gate voltages of the MOS-FET 10 are equal and this MOS-FET becomes OFF.

The voltage at terminal 15 being 0 volt, the condenser 6 charges through the MOS-FET 5 and the voltage at connecting point 18 becomes 1 volt so that said condenser 6 receives 1 volt charge.

If now the input signal inverts, the voltage at terminal 15 becoming -1 volt, the MOS-FET 3 changes to OFF, and the MOS-FET 4 changes to ON, the source and gate voltages of MOS-FET 5 become equal and the MOS-FET 5 becomes OFF.

However, because the first condenser 6 does not suddenly lose its charge, the voltage at terminal 18 falls to -2 volts when the voltage at terminal 15 changes to -1 volt. Therefore, the voltage at terminal 7 becomes -2 volts, MOS-FET 8 changes to ON, and MOS-FET 9 changes to OFF. Therefore the voltage at the common drain connection 12 of the MOS-FETs 8 and 9 becomes 0 volt, and MOS-FET 10 becomes ON.

Accordingly the second condenser 11 charges through the MOS-FET 10 and the voltage at terminal 17 becomes lower than -1 volt. At this time the first condenser 6 discharges.

When the voltage at terminal 13 is -1 volt and that at terminal 15 is 0 volt, the first condenser 6 charges. When the input signal inverts, its stored charge is transferred to the second condenser 11. With repetition of these operations, the condenser 11 is slowly charged until it is charged to twice the power source and this voltage appears at terminal 17. When a load is connected between the terminals 16 and 17, the said second condenser 11 remains charged by the repeated switching operations described so that the output voltage is maintained at a substantially constant level.

Figure 2 shows in conventional waveform manner the voltages appearing at various points in the arrangement of Figure 1, the voltages appearing at said various points being indicated by the references used in Figure 1 for the respective points. In view of the description already given it is thought that no further explanation of Figure 2 is necessary.

The arrangement of Figure 1 has the great advantage that the MOS-FETs are easily

incorporated in an integrated circuit construction enabling a very small and compact construction to be achieved, for the only circuit elements which are not FETS are the condensers. Accordingly the invention is highly advantageous for use as a boosting arrangement in apparatus in which the attainment of a high degree of compactness, as well as low cost, are of great importance - notably in electronic watches and small (pocket) calculators. Figure 2 shows a two unit arrangement giving a boost ratio of two, but, by increasing the number of boosting stages, higher boost ratios can be achieved. Figure 3, which is almost self-explanatory and needs but little further description shows an arrangement comprising three boosting stage units referenced 1, 2 and 19. Units 1 and 2 are identical with the units 1 and 2 of Figure 1. The third unit 19 is identical with unit 2 and is connected to it in the same way as that in which unit 2 is connected to unit 1.

Figure 4 shows another embodiment of the invention and, like Figure 1 has two stage units though, again like Figure 1, it could be extended to include more than two stage units.

Referring to Figure 4, block 40 in the first boosting unit and block 41 is the second. The first boosting unit 40 includes a P type MOS-FET 42 which acts as a switching element and has its source electrode connected at 50 to the high voltage terminal of a voltage supply source. Input pulses ϕ_1 fed into the point so marked, are applied to the gate of said MOS-FET 42. The drain electrode of MOS-FET 42 is connected to the drain-electrode of an N type MOS-FET 43 and to the gate electrode of an N type MOS-FET 44 the drain electrode of which is connected to a low voltage terminal 45 of said voltage supply source. The gate electrode of the MOS-FET 43 is also connected to terminal 45. The source electrodes of the MOS-FETs 43 and 44 are connected together and to one side of a condenser 47 at point 46. The input pulses ϕ_1 are inverted by an inverter 48 and applied to the other side of said condenser 47. The second boosting unit 2 includes a P type MOS-FET 49 the source electrode of which is connected to the same high voltage terminal 50 as the source electrode of the MOS-FET 42 in the first boosting unit. The inverted input pulse ϕ_1 appearing at the output of the inverter 48 is applied to the gate electrode of the MOS-FET 49. The drain electrode of the MOS-FET 49 is connected to the drain electrode of an N type MOS-FET 52 and the common drain connection is connected to the gate electrode of an N type MOS-FET 51 the drain electrode of which is connected to point 46 in the first unit. The source electrodes of the MOS-FETs 51 and 52 are

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connected together and to an output terminal 53 and also to one side of a condenser 54, the other side of which is connected to the source electrode of the MOS-FET 49. The boosted output voltage appears between the output terminal 53 and the high voltage point 50.

The operation of Figure 4 will now be described with the aid of Figure 5 which bears the same relation to Figure 4 as Figure 2 does to Figure 1.

Referring to Figure 5 this shows the input pulses ϕ_1 which are applied to the gate electrode of the MOS-FET 42 in the first boosting unit 40; and the pulses ϕ_1 inverted by the inverter 48, which are applied to the gate electrode of the MOS-FET 49 in the second boosting unit 41 and to one side of the condenser 47. If the voltage at the high voltage point 50 of the power supply is 0 volt, and the voltage at the low voltage point 45 of said supply is -1 volt, the MOS-FET 42 will become ON when the voltage of the pulse ϕ_1 is -1 volt, and the MOS-FET 44 will also become ON so that the voltage at point 46 will become 1 volt. At this time the voltage on that electrode of the condenser 47 connected to the output side of the inverter 48 will be 0 volt. When the voltage of the input pulse ϕ changes to 0 volt, MOS-FET 42 becomes OFF, and the voltage at point 46 becomes lower than -2 volt because of the -1 volt change of voltage at the side of the condenser 47 connected to the inverter 48. The MOS-FET 44 becomes OFF and the MOS-FET 43 becomes ON. When the voltage of input pulse ϕ_1 is changed to -1 volt, MOS-FETs 42 and 44 become ON and the voltage at point 46 changes to -1 volt, the MOS-FET 43 being OFF. Figure 5 shows the waveform of voltage at point 46 by the waveform so referenced.

In the second boosting unit 41, if the voltage of the inverted pulse ϕ_1 applied to the gate electrode of MOS-FET 49 is -1 volt, this MOS-FET 49 becomes ON, and also MOS-FET 51 becomes ON. Therefore, the voltage at the output terminal 53 becomes -2 volts (at this time the voltage at point 46 is -2 volts). After this, the voltage of the inverted input pulse ϕ_1 became 0 volt, MOS-FETs 49 and 51 become OFF and MOS-FET 52 becomes ON. In this condition the output terminal 53 is maintained at -2 volts by the charged condenser 54. Figure 5 shows the voltage waveform at terminal 53 by the waveform so referenced.

Figure 6 shows a further embodiment of the invention. In the example shown in Figure 6, there are three boosting units namely those in the blocks 50 (the first boosting unit), 51 (the second boosting unit) and 52 (the third boosting unit). The first boosting unit 50 includes a P type MOS-

FET 53 used as a switching element and having its source electrode connected to a high voltage point 54 of a voltage power supply. An input pulse ϕ_2 is applied to the gate electrode of the MOS-FET 53 and the drain electrode thereof is connected to the drain electrode of an N type MOS-FET 56, the common drain connection being connected to the gate electrode of an N type MOS-FET 55 the drain electrode of which is connected to a low voltage point 56 of the voltage supply as also is the gate electrode of the MOS-FET 87. The source electrode of the MOS-FET 55 is connected at point 57 to the source electrode of the MOS-FET 87 and also to one side of a condenser 59 to the other side of which the input pulses, inverted by an inverter 58 are applied.

Second boosting unit 51 includes a P type MOS-FET 60, which is used as a switching element and which has its source electrode connected to the high voltage point 54 of the voltage supply. The inverted input pulses ϕ_2 from the inverter 58 are applied to the gate electrode of the MOS-FET 60 the drain of which is connected to the drain electrode of an N-type MOS-FET 62 and the common drain connection is connected to the gate electrode of an N type MOS-FET 61. The drain electrode of MOS-FET 61 is connected to the point 57 in unit 50 as also is the gate electrode of MOS-FET 62. The source electrode of MOS-FET 61 is connected at point 63 to the source electrode of the MOS-FET 62 and to one side of a condenser 66. The input pulses ϕ_2 are applied to the other side of the condenser through two inverters 64 and 65 in series.

The third boosting unit 52 is similar to the second one, 51 and has a P type MOS-FET 67 which serves as a switching element and the source electrode of which is connected to the high voltage point 54. Output pulses from the inverter 65 are applied to the gate electrode of said MOS-FET 67, the drain electrode of which is connected to the drain electrode of an N-type MOS-FET 69. The common drain connection is connected to the gate electrode of an N type MOS-FET 68 the drain electrode of which is connected to the point 63 in the second boosting unit 51 as also is the gate electrode of the MOS-FET 69. The source electrodes of the MOS-FETs 68 and 69 are connected together and to the output terminal 70 and a condenser 71 is connected between said output terminal on the one hand, and the source electrode of the MOS-FET 67 and the high voltage point 54 on the other. Boosted output voltage appears between said output terminal 70 and said high voltage point 54.

The operation of the embodiment in Figure 6 is illustrated graphically in Figure 7.

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Figure 7 shows the input pulse wave ϕ_2 which is applied to the gate electrode of the MOS-FET 53 in the first boosting unit 50, a pulsed wave of the same phase being applied to the gate electrode of the MOS-FET 67 in the third boosting unit 52 and to the condenser 66 in the second unit 51. An inverted input pulse ϕ_2 , as also shown in Figure 7 is applied from the inverter 58 to the MOS-FET 60 in the second unit 51 and to the condenser 59 in the first unit 50.

If the voltage at the high voltage point 54 of the voltage supply is 0 volt, and that at the low voltage point 56 is -1 volt, a signal as indicated by waveform 57 appears at point 57 due to the input pulsed wave ϕ_2 which alternates between 0 volt and -1 volt. This signal is applied to the drain electrode of MOS-FET 61, and the gate electrode of the MOS-FET 62 in the second boosting unit 51. When the voltage of the inverted pulsed wave ϕ_2 is -1 volt, the MOS-FET 60 becomes ON, and the MOS-FET 61 also becomes ON. At this time, the voltage at terminal 57 is -2 volts and the voltage at terminal 63 is also -2 volts.

When the voltage of the inverted pulsed wave ϕ_2 changes to 0 volt, the MOS-FETs 60 and 61 become OFF, and the MOS-FET 62 becomes ON. At this time the voltage at the output side of the inverter 65 changes from 0 volt to -1 volt and the voltage at the point 63 is changed via the condenser 66 from -2 volts to -3 volts. The voltage changes at the point 63 are indicated by the waveform 63 in Figure 7. The changed voltage at point 63 is applied to the drain electrode of the MOS-FET 68 and to the gate electrode of the MOS-FET 69 in the third boosting unit 52. If the voltage of the input pulsed wave ϕ_2 applied to the gate electrode of the MOS-FET 67 is -1 volt, MOS-FET 67 becomes ON, as does the MOS-FET 68, and a voltage of -3 volts appears at the point 63 and at the output terminal 70. This voltage is maintained by the condenser 71. When the input pulsed voltage applied to the MOS-FET 67 changes to 0 volt, MOS-FETs 67 and 68 become OFF, and the voltage at the output terminal 70 is maintained at -3 volts as indicated at 70 in Figure 7.

In this way a boosting voltage ratio of three is obtained by means of the three boosting units 50, 51 and 52.

Figure 8 is a simplified block diagram of an electronic watch having a boosting circuit arrangement in accordance with the invention. As shown in Figure 8 the watch has a quartz or other time standard oscillator 80 which feeds into a frequency divider 81 which provides, from the oscillator output, a 1HZ time standard pulse. This is applied to a level shifter 82. A frequency divided signal, preferably derived from an interme-

diated stage of the divider 81 is applied as input to a boosting circuit arrangement 86 which is an arrangement in accordance with this invention. If the arrangement 86 has a boosting ratio of three, e.g. it is as described with reference to Figure 6 it will boost the input voltage to three times its original voltage. This boosted voltage is applied to the level shifter 82; to time measuring (counting) apparatus at 83, which provides time signals (e.g. hour, minute and second signals) at the outputs; to a driving circuit 84 which receives said time signals; and to a time display device 85 driven by said driving circuit. The level shifter 82 shifts the level of the standard 1HZ pulses from the divider 81 and applies them to the time measuring apparatus at 83, which, as already stated consists of counting circuits which produce time signals and applies them, amplified, to the driving circuit 84. The driving circuit 84 is of known form adapted to provide output suitable for operating the display device 85 which may, for example, be a numeric or digital display device comprising time displaying numerals each comprising seven display electrode segments as well known per se.

The invention has the great practical advantage that because boosting arrangements in accordance herewith are composed almost entirely of MOS-FETs (in the illustrated embodiments the condensers are the only circuit elements which are not MOS-FETs) they can be made substantially smaller and more compact than conventional boosters using diodes and lend themselves admirably to integrated circuit construction. Indeed the boosting units may be on the same chip with one another and, in many cases, with other circuitry in a watch or in a pocket calculator. Almost any overall voltage boosting ratio can be obtained by connecting a suitably chosen number of boosting units to one another, each providing an output voltage which is used as the input voltage to the next.

WHAT WE CLAIM IS:

1. A voltage booster including as its first voltage boosting stage a circuit comprising two series connected complementary MOS-FETs at least one of which has its gate connected to one of two pulse input terminals of the booster and which are together in series with a condenser between said pulse input terminals, said complementary MOS-FETs having a common drain connection connected to the gate of an N-type MOS-FET, the connection point of the series-connected complementary MOS-FETs with said condenser constituting an output terminal of said first voltage boosting stage and being connected to the source of said N-type MOS-FET the drain of which is connected to a point of anchored potential.



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Figure 7 shows the input pulse wave ϕ_2 which is applied to the gate electrode of the MOS-FET 53 in the first boosting unit 50, a pulsed wave of the same phase being applied to the gate electrode of the MOS-FET 67 in the third boosting unit 52 and to the condenser 66 in the second unit 51. An inverted input pulse ϕ_2 , as also shown in Figure 7 is applied from the inverter 58 to the MOS-FET 60 in the second unit 51 and to the condenser 59 in the first unit 50.

If the voltage at the high voltage point 54 of the voltage supply is 0 volt, and that at the low voltage point 56 is -1 volt, a signal as indicated by waveform 57 appears at point 57 due to the input pulsed wave ϕ_2 which alternates between 0 volt and -1 volt. This signal is applied to the drain electrode of MOS-FET 61, and the gate electrode of the MOS-FET 62 in the second boosting unit 51. When the voltage of the inverted pulsed wave ϕ_2 is -1 volt, the MOS-FET 60 becomes ON, and the MOS-FET 61 also becomes ON. At this time, the voltage at terminal 57 is -2 volts and the voltage at terminal 63 is also -2 volts.

When the voltage of the inverted pulsed wave ϕ_2 changes to 0 volt, the MOS-FETs 60 and 61 become OFF, and the MOS-FET 62 becomes ON. At this time the voltage at the output side of the inverter 65 changes from 0 volt to -1 volt and the voltage at the point 63 is changed via the condenser 66 from -2 volts to -3 volts. The voltage changes at the point 63 are indicated by the waveform 63 in Figure 7. The changed voltage at point 63 is applied to the drain electrode of the MOS-FET 68 and to the gate electrode of the MOS-FET 69 in the third boosting unit 52. If the voltage of the input pulsed wave ϕ_2 applied to the gate electrode of the MOS-FET 67 is -1 volt, MOS-FET 67 becomes ON, as does the MOS-FET 68, and a voltage of -3 volts appears at the point 63 and at the output terminal 70. This voltage is maintained by the condenser 71. When the input pulsed voltage applied to the MOS-FET 67 changes to 0 volt, MOS-FETs 67 and 68 become OFF, and the voltage at the output terminal 70 is maintained at -3 volts as indicated at 70 in Figure 7.

In this way a boosting voltage ratio of three is obtained by means of the three boosting units 50, 51 and 52.

Figure 8 is a simplified block diagram of an electronic watch having a boosting circuit arrangement in accordance with the invention. As shown in Figure 8 the watch has a quartz or other time standard oscillator 80 which feeds into a frequency divider 81 which provides, from the oscillator output, a 1HZ time standard pulse. This is applied to a level shifter 82. A frequency divided signal, preferably derived from an interme-

diated stage of the divider 81 is applied as input to a boosting circuit arrangement 86 which is an arrangement in accordance with this invention. If the arrangement 86 has a boosting ratio of three, e.g. it is as described with reference to Figure 6 it will boost the input voltage to three times its original voltage. This boosted voltage is applied to the level shifter 82; to time measuring (counting) apparatus at 83, which provides time signals (e.g. hour, minute and second signals) at the outputs; to a driving circuit 84 which receives said time signals; and to a time display device 85 driven by said driving circuit. The level shifter 82 shifts the level of the standard 1HZ pulses from the divider 81 and applies them to the time measuring apparatus at 83, which, as already stated consists of counting circuits which produce time signals and applies them, amplified, to the driving circuit 84. The driving circuit 84 is of known form adapted to provide output suitable for operating the display device 85 which may, for example, be a numeric or digital display device comprising time displaying numerals each comprising seven display electrode segments as well known per se.

The invention has the great practical advantage that because boosting arrangements in accordance herewith are composed almost entirely of MOS-FETs (in the illustrated embodiments the condensers are the only circuit elements which are not MOS-FETs) they can be made substantially smaller and more compact than conventional boosters using diodes and lend themselves admirably to integrated circuit construction. Indeed the boosting units may be on the same chip with one another and, in many cases, with other circuitry in a watch or in a pocket calculator. Almost any overall voltage boosting ratio can be obtained by connecting a suitably chosen number of boosting units to one another, each providing an output voltage which is used as the input voltage to the next.

WHAT WE CLAIM IS:

1. A voltage booster including as its first voltage boosting stage a circuit comprising two series connected complementary MOS-FETs at least one of which has its gate connected to one of two pulse input terminals of the booster and which are together in series with a condenser between said pulse input terminals, said complementary MOS-FETs having a common drain connection connected to the gate of an N-type MOS-FET, the connection point of the series-connected complementary MOS-FETs with said condenser constituting an output terminal of said first voltage boosting stage and being connected to the source of said N-type MOS-FET the drain of which is connected to a point of anchored potential.

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2. A voltage booster as claimed in claim 1 wherein the gates of both the series connected complementary MOS-FETs are connected to said one pulse input terminal.
3. A voltage booster as claimed in claim 1 or 2 wherein there is a plurality of similar voltage boosting stages each of which, except the first, has pulse input terminals connected to receive output from the preceding stage as its pulse input.
4. A voltage booster wherein the first (or only) stage comprises a P-type MOS-FET having its source connected to a point of relatively high fixed potential and its gate connected to one of two pulse input terminals; a first N-type MOS-FET having its drain connected to a point of relatively low fixed potential and its gate connected to the drain of said P-type MOS-FET; a second N-type MOS-FET having its source connected to the source of said first N-type MOS-FET, its drain connected to the drain of said P-type MOS-FET, and its gate connected to the gate of said P-type MOS-FET, and a condenser one side of which is connected to the other of the pulse input terminals and the other side of which is connected to the common connection point of the sources of said first and second N-type MOS-FETs.
5. A voltage booster wherein the first (or only) stage comprises a P type MOS-FET having its source connected to a point of relatively high fixed potential and its gate connected to a pulse input terminal; a first N type MOS-FET having its drain connected to a point of relatively low fixed potential and its gate connected to the drain of said P type MOS-FET; a second N type MOS-FET having its source connected to the source of said first N type MOS-FET, its drain connected to the drain of said P type MOS-FET, and its gate connected to said point of relatively low fixed potential; and a condenser one side of which is connected to said pulse input terminal through an inverter and the other side of which is connected to the common connection point of the sources of said first and second N type MOS-FETs.
6. A booster as claimed in claim 5 wherein the first stage is followed by a second stage also including a P type MOS-FET and first and second N type MOS-FETs interconnected similarly to the corresponding circuit elements in the first stage and wherein there is a connection between the output terminal of the inverter of the first stage and the gate of the P type MOS-FET in the second stage; a connection between the drain of the first N type MOS-FET in said second stage and the source of the first N type MOS-FET in the first stage; a connection between the source of the P type MOS-FET in said second stage and said point of relatively high fixed potential; and a condenser connected between said point of relatively high fixed potential and the common source connection of the first and second N type MOS-FETs in the second stage.
7. A voltage booster as claimed in any of the preceding claims wherein every circuit element which is not a MOS-FET is a condenser.
8. A voltage booster substantially as herein described with reference to Figure 1 of the accompanying drawings.
9. A voltage booster substantially as herein described with reference to Figure 3 of the accompanying drawings.
10. A voltage booster substantially as herein described with reference to Figure 4 of the accompanying drawings.
11. A voltage booster substantially as herein described with reference to Figure 6 of the accompanying drawings.
12. An electronic timepiece or electronic calculator including in its circuitry a voltage booster as claimed in any of the preceding claims.
13. An electronic timepiece in accordance with claim 12 and substantially as herein described with reference to Figure 8 of the accompanying drawings.
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