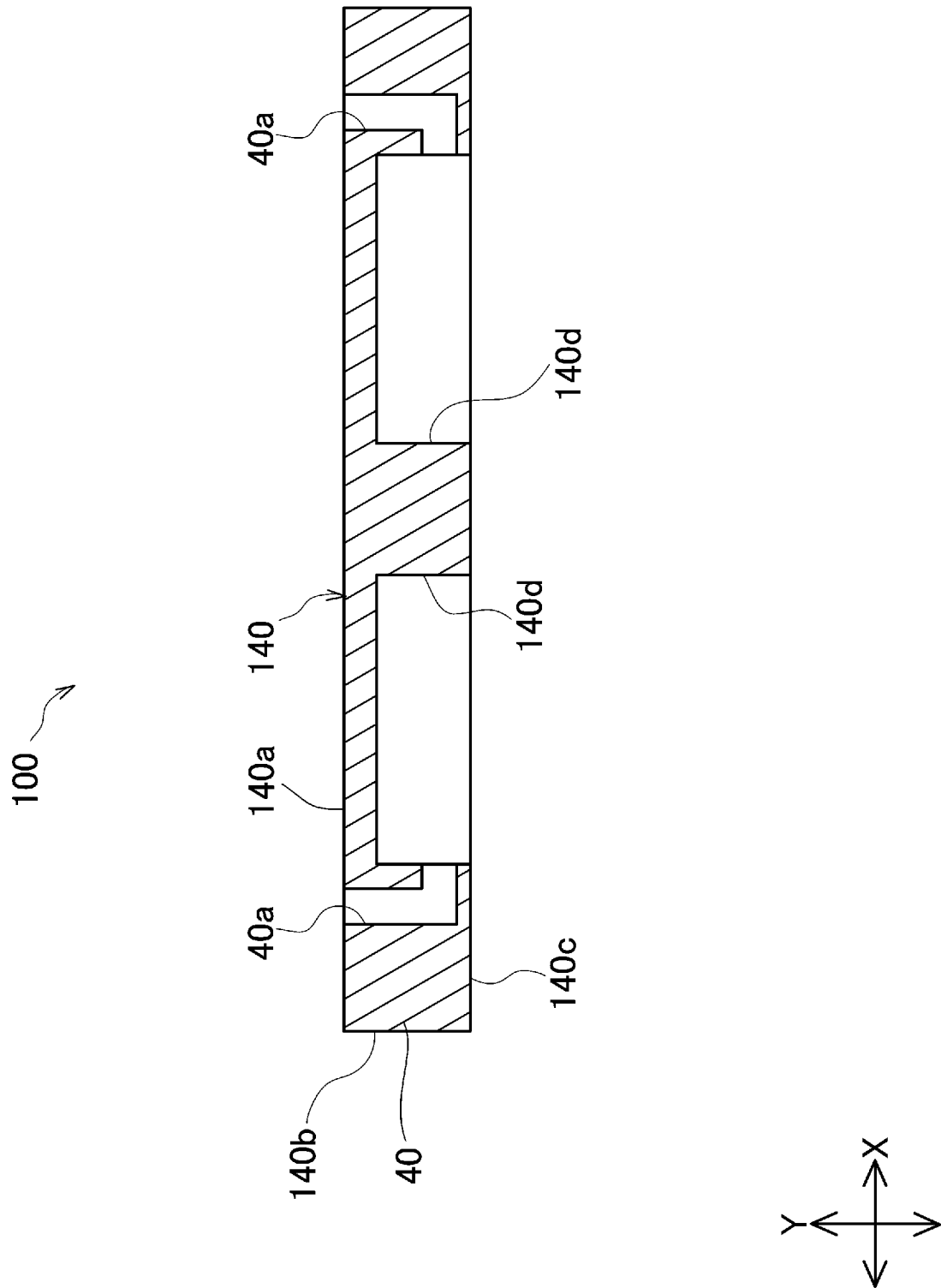
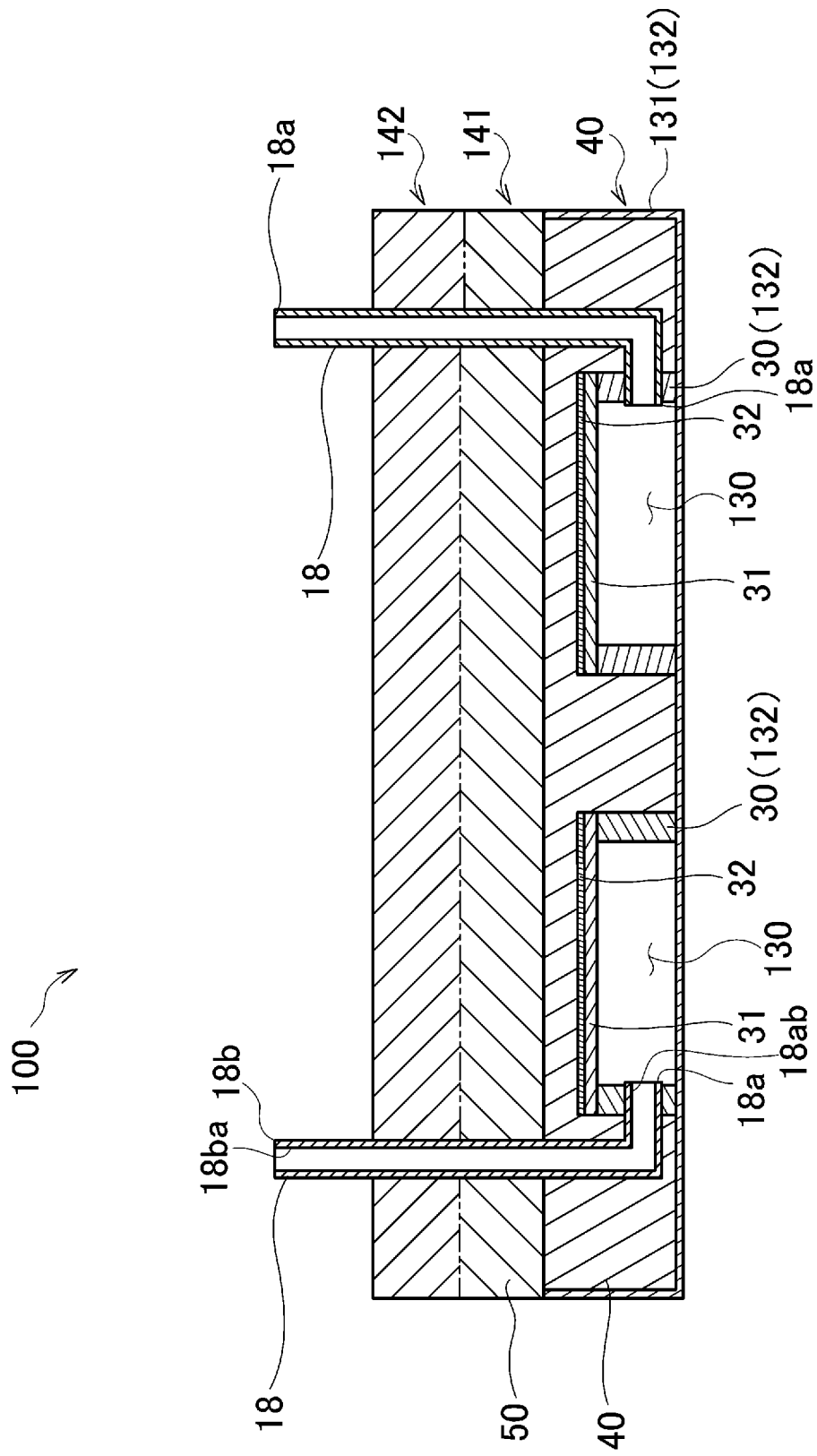


[図1]



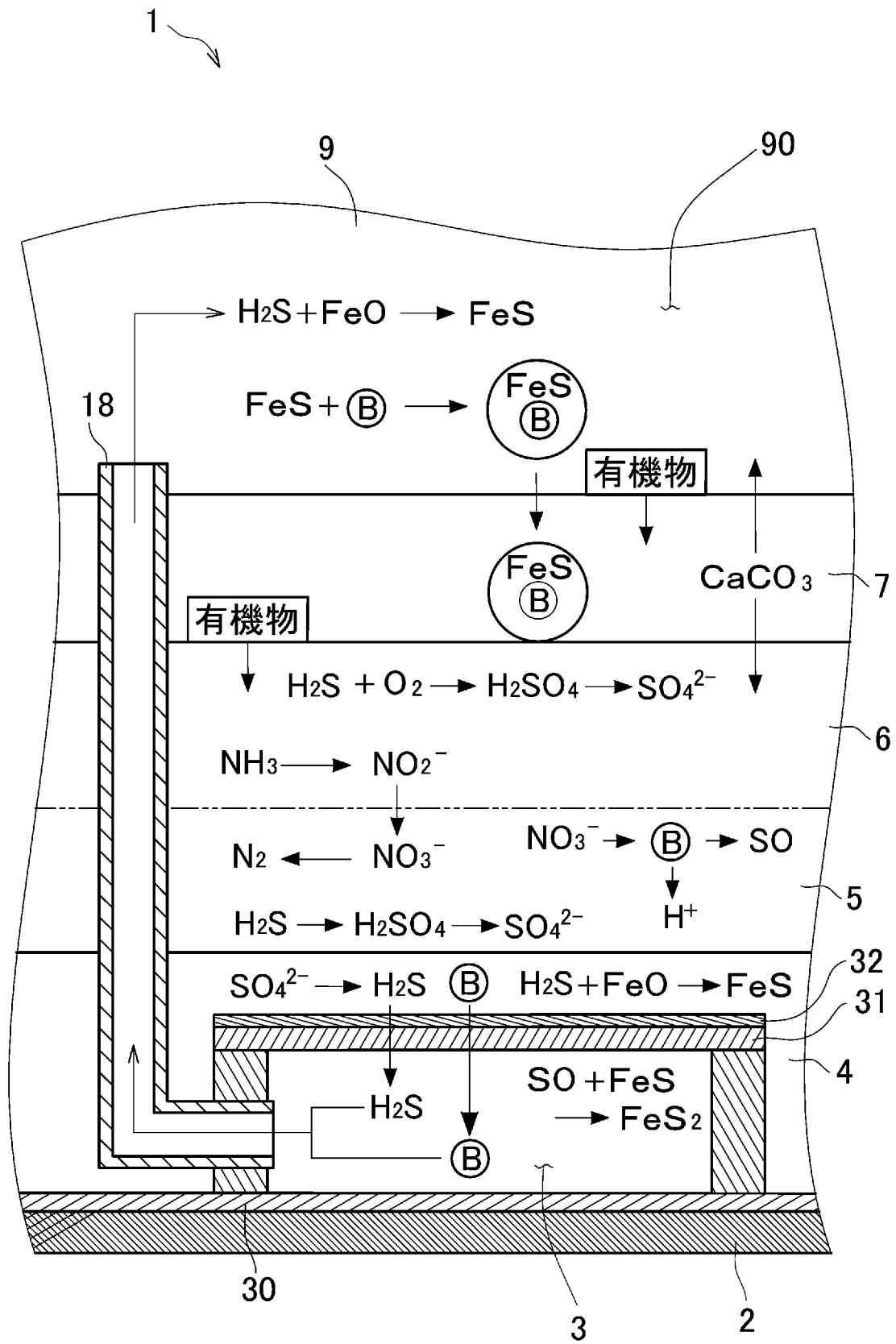
This cross-sectional diagram illustrates a semiconductor device 100. It features a substrate 40 with a top surface 40a and bottom surface 40b. Two transistors are formed on the top surface: transistor 8 on the left and transistor 140(132) on the right. Each transistor includes a gate stack (30, 130) with a gate insulating layer (31, 131) and a gate electrode (32, 132). Source/drain regions (30a, 130a) are located beneath the gate electrodes. A channel stopper (18, 140c) is positioned between the two transistors. The channel stopper has a top surface 18ab and side surfaces 18ba, 18b. Dimensions L1 and L2 indicate specific lengths related to the channel stopper and the distance between the transistors. A coordinate system with X and Y axes is shown at the bottom.

[図3]

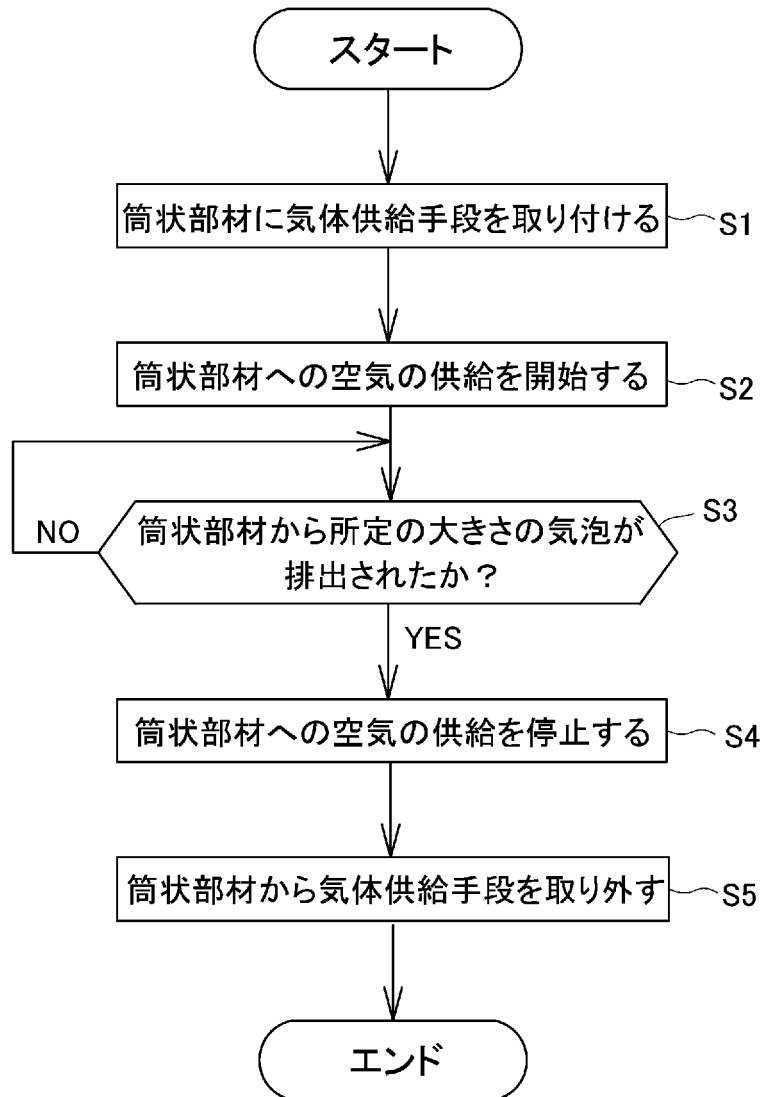




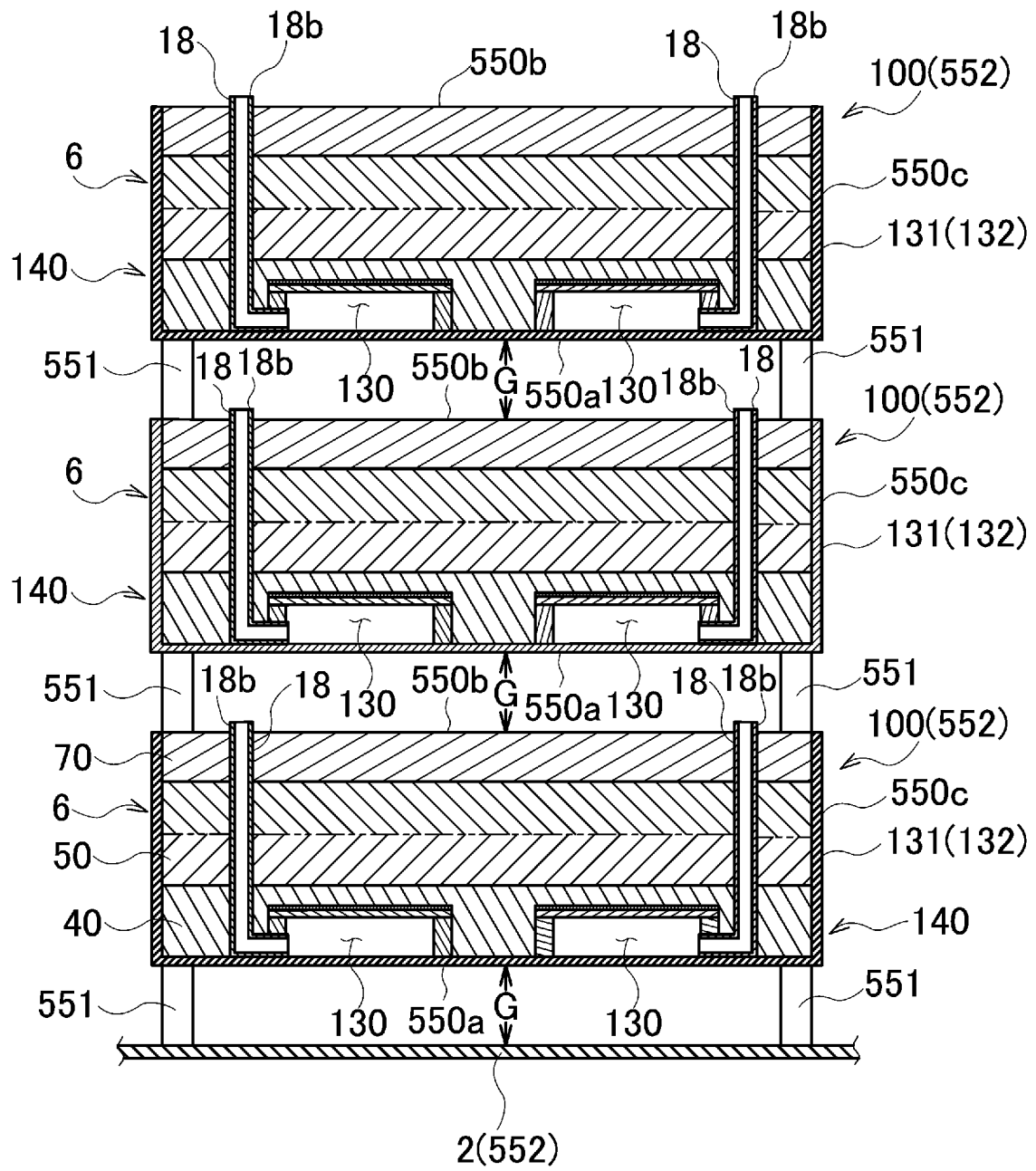
[図5]



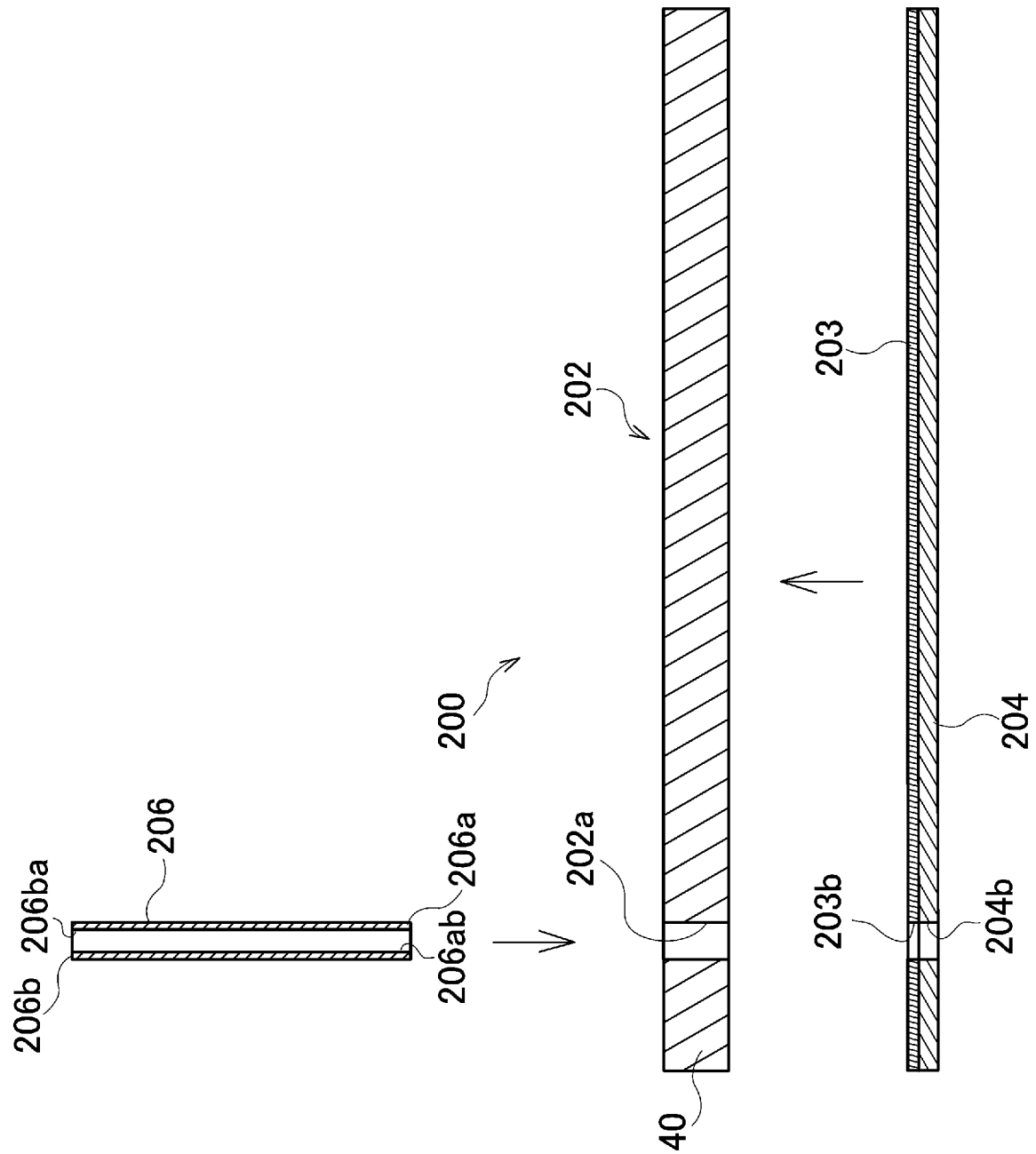
[図6]



[図7]

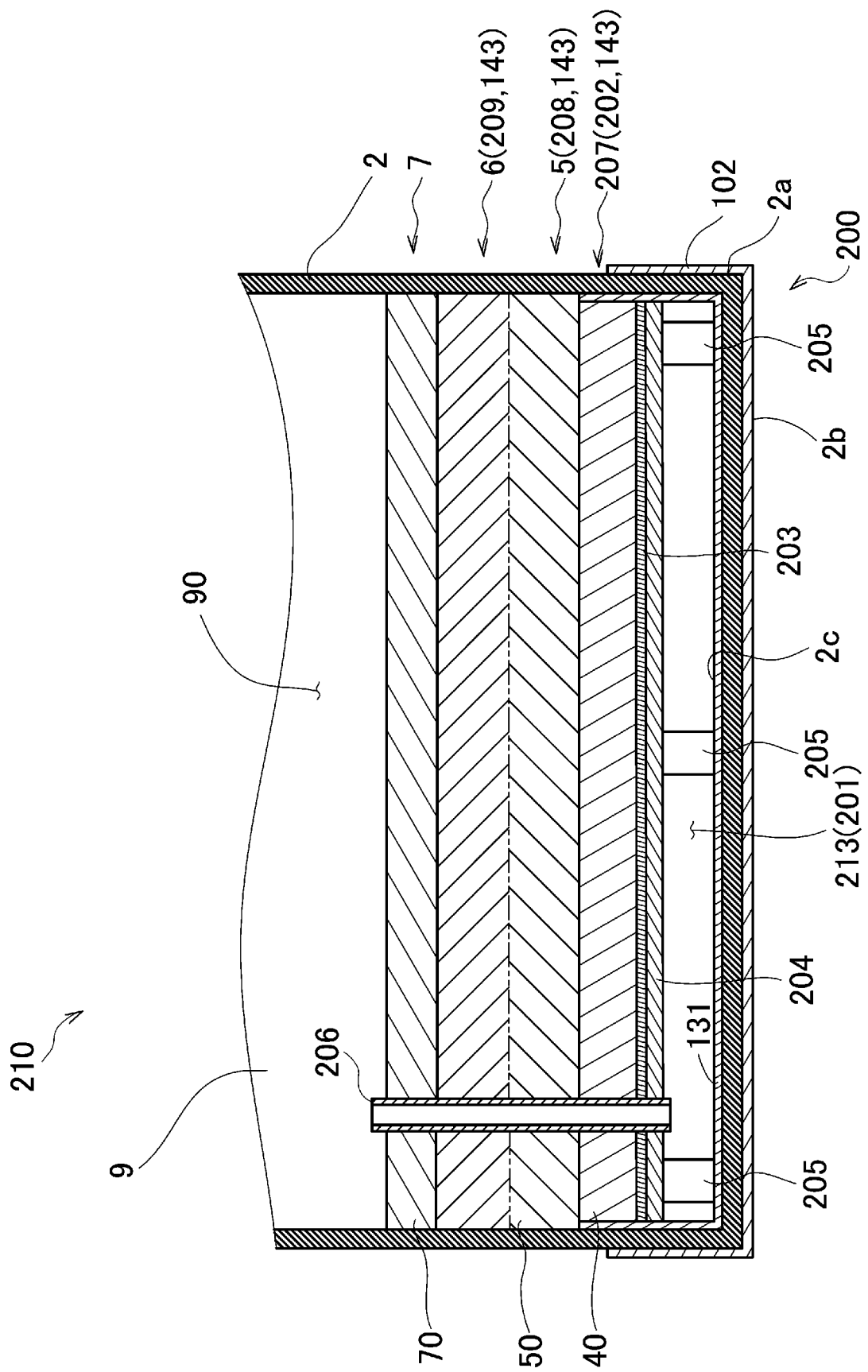


[図8]





[図10]





750 ↗

