

Description

Background of the invention

Field of the invention

This invention relates, in general, to counters and more particularly to ripple counters having a reduced propagation delay.

Background art

Ripple counters having "D" type flip-flops of which a first flip-flop has a clock input responsive to a clock pulse, and a D input responsive to a $\bar{Q}$ output are known from, for example, SMPTE Journal, Vol. 87, No. 1, January 1978 pages 28-35 and Japanese Patent Abstract No. JP-A-5344165. In such ripple counters a clock input of a second flip-flop is responsive to a Q output of the first flip-flop, and a D input of the second flip-flop is responsive to a $\bar{Q}$ output of the second flip-flop. A Q output of the second flip-flop may clock a third flip-flop in a similar manner, with the number of flip-flops so connected determined by the desired count length, or divider ratio. Each flip-flop serially connected in this manner introduces a propagation delay between the first clock input and the last Q output. This propagation delay can be reduced by operating the flip-flops at higher bias currents.

Circuitry requiring low currents, such as the Electronic Telephone Chip (ETC) which includes a Dual Tone Multifrequency (DTMF) Generator For Touch Tone Dialing, may require that the current for each gate be limited. I²L technology used in such circuitry has speed limitations, such that more current is needed for lower propagation delays. When a ripple counter as described above is used to implement a programmable counter, the propagation delay of the flip-flops becomes the limiting factor in determining the highest clock frequency.

Therefore, what is needed is a flip-flop circuit having reduced propagation delay and a reduced total current requirement.

Summary of the invention

Accordingly, the present invention provides a ripple counter circuit having reduced propagation delay including at least four D-type flip-flops, each flip-flop having a clock input, an output, and an inverted output which is coupled to a D-input wherein said clock input of a first flip-flop is responsive to a clock signal, said clock input of a second flip-flop is coupled to said output of said first flip-flop, each subsequent flip-flop having its clock input coupled to the output of the preceding flip-flop, said ripple counter circuit characterized in that said second flip-flop has its clock input also responsive to said clock signal and each flip-flop subsequent to the first flip-flop has its output also coupled to an output of the preceding flip-flop.

The present invention will be better understood from the following detailed description taken in conjunction with the accompanying drawings.

Brief description of the drawings

Figure 1 is a block diagram of a known ripple counter circuit using D-type flip-flops.

Figure 2 is a timing diagram illustrating the operation of the counter circuit of Figure 1.

Figure 3 is a block diagram of the ripple counter circuit of the present invention.

Figure 4 is a timing diagram illustrating the operation of the ripple counter circuit of the present invention.

Detailed description of the invention

Referring to Figure 1, a typical ripple counter circuit 10 includes a first flip-flop 12 having a clock input $\overline{\text{CLK}}$ connected to terminal 14 and responsive to a clock signal. Flip-flop 16 has a clock input $\overline{\text{CLK}}$ connected to an output Q of flip-flop 12. Both flip-flops 12, 16 each have an output $\bar{Q}$ connected to their respective input D. It is obvious to those skilled in the art that a "D" type flip-flop so connected functions as a toggle flip-flop. Therefore, the ripple counter circuit 10 may comprise toggle flip-flops in place of "D" type flip-flops. Output Q of flip-flop 16 may be connected to additional flip-flops (not shown) as required.

Referring to Figure 2, waveform 18 illustrates a typical clock signal applied to input terminal 14. Waveforms 20, 22 illustrate the output Q of flip-flops 12, 16, respectively. When a downward transition occurs on waveform 18 and flip-flop 12 is "clocked", the output Q of flip-flop 12, waveform 20, will transition upward after propagation delay t_{PD1} . On the next downward transition of waveform 18, waveform 20 will transition downward after the propagation delay t_{PD1} , thereby clocking flip-flop 16, causing waveform 22 to transition upward after another propagation delay t_{PD2} associated with flip-flop 16. Therefore, output Q of flip-flop 16 of the known circuit, includes a total propagation delay t_{PD} equal to $t_{PD1} + t_{PD2}$.

Referring now to Figure 3, ripple counter circuit 24 is shown which is suitable to be fabricated in monolithic integrated circuit form as well as with discrete components. Circuit 24 includes NAND gate 25 having an input connected to terminal 28 and responsive to a clock signal. Flip-flop 26 has a clock input $\overline{\text{CLK}}$ connected to one output of NAND gate 25. Flip-flop 30 has a clock input $\overline{\text{CLK}}$ wired ANDed to output Q₁ of flip-flop 26 and another output of NAND gate 25. Flip-flop 32 has a clock input $\overline{\text{CLK}}$ wired ANDed to output Q₁ of flip-flop 30 and output Q₂ of flip-flop 26. Additional flip-flops may be connected in a similar manner as shown in the drawing by N flip-flop 34. Each additional serially connected flip-flop has its clock input $\overline{\text{CLK}}$ responsive to the wire ANDed signals from the output Q₁ of the preceding flip-flop and the output Q₂ of the twice preceding flip-flop. Flip-flops 26, 30, 32, 34 each have an output $\bar{Q}$ connected to its respective input D.

Referring to Figure 4, waveform 36 illustrates the signal at the output of the NAND gate 25. Waveform 40 illustrates the signal applied to clock input $\overline{\text{CLK}}$ of flip-flop 30. This signal is the

wired AND of the signal from NAND gate 25 and the output Q_1 from flip-flop 26. Therefore, waveform 40 will transition downward when waveform 36 transitions downward, regardless of the propagation delay of flip-flop 26.

Waveform 44 illustrates the clock input $\overline{CLK}$ to flip-flop 32 and is the result of the wired AND of output Q_1 of flip-flop 30 and Q_2 of flip-flop 26. Therefore waveform 44 transitions downward with a propagation delay of T_{PD1} . Comparing this result with the circuit and waveforms of Figure 1 and 2 respectively, it may be seen that the propagation delay T_{PD2} has been avoided. Waveform 48 illustrates the clock input $\overline{CLK}$ signal to flip-flop 34 and is the result of the wired AND of output Q_1 of flip-flop 32 and output Q_2 of flip-flop 30. Waveform 48 has a propagation delay of only T_{PD2} . Therefore, for example, the output of flip-flop circuit 24 will have only two propagation delays for four flip-flops and four propagation delays for eight flip-flops, wherein the prior art circuit 10 of Figure 1 had delays of four and eight, respectively.

By now it should be appreciated that there has been provided an improved ripple counter circuit that may be used in programmable counters. This ripple counter circuit reduces the propagation delays inherently induced by the flip-flops, therefore reducing the amount of current required to drive the circuit at a required speed.

Claim

A ripple counter circuit (24) having reduced propagation delay including at least four D-type flip-flops (26, 30, 32, 34), each flip-flop having a clock input (CLK), an output (Q_1 , Q_2) and an inverted output ($\overline{Q}$) which is coupled to a D-input wherein said clock input of a first flip-flop (26) is responsive to a clock signal, said clock input of a second flip-flop (30) is coupled to said output of said first flip-flop, each subsequent flip-flop having its clock input coupled to the output of the preceding flip-flop, said ripple counter circuit characterized in that said second flip-flop has its clock input also responsive to said clock signal

and each flip-flop subsequent to the first flip-flop has its output also coupled to an output of the preceding flip-flop.

Patentanspruch

Asynchrone Zählerschaltung (24) mit reduzierter Laufzeit, enthaltend wenigstens vier D-Flipflops (26, 30, 32, 34), von denen jedes einen Takteingang (CLK), einen Ausgang (Q_1 , Q_2) und einen invertierten Ausgang ($\overline{Q}$) aufweist, der mit einem D-Eingang verbunden ist, wobei der Takteingang eines ersten Flipflops (26) auf ein Taktsignal anspricht, der Takteingang eines zweiten Flipflops (30) mit dem Ausgang des ersten Flipflops verbunden ist, jedes nachfolgende Flipflop mit seinem Takteingang mit dem Ausgang des vorangehenden Flipflops verbunden ist, dadurch gekennzeichnet, daß der Takteingang des zweiten Flipflops ebenfalls auf das Taktsignal anspricht und daß jedes sich an das erste Flipflop anschließende Flipflop mit seinem Ausgang ebenfalls mit einem Ausgang des vorangehenden Flipflops verbunden ist.

Revendication

Circuit de compteur en anneau (24) ayant un délai de propagation réduit, comportant au moins quatre circuits bistables de type D (26, 30, 32, 34), chaque circuit bistable comportant une entrée d'horloge (CLK), une sortie (Q_1 , Q_2) et une sortie inversée ($\overline{Q}$) qui est couplée avec une entrée (d), dans lequel ladite entrée d'horloge d'un premier circuit bistable (26) réagit à un signal d'horloge, ladite entrée d'horloge d'un second circuit bistable (30) est couplée avec ladite sortie dudit premier circuit bistable, chaque circuit bistable suivant ayant son entrée d'horloge couplée avec la sortie du circuit bistable précédent, ledit circuit de compteur en anneau étant caractérisé en ce que l'entrée d'horloge dudit second circuit bistable, réagit également audit signal d'horloge et la sortie de chaque circuit bistable suivant le premier circuit bistable est également couplée avec une sortie du circuit bistable précédent.

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