What is claimed is:

1. A memory cell, comprising:

a vertical channel coupled at a first end of the vertical channel to a capacitor, the vertical channel configured to increase a native band gap energy of material forming the channel;

a dielectric substantially surrounding the vertical channel; and

a field electrode coupled to the vertical channel using the dielectric.

2. The memory cell of claim 1, wherein the capacitor is a double-sided capacitor associated with a dynamic random access memory.

3. The memory cell of one of claims 1 and 2, wherein the vertical channel is coupled to the capacitor using at least one shared doped region.

4. The memory cell of claim 3, wherein the at least one doped region is formed from a silicon substrate.

5. The memory cell of one of claims 1-4, wherein the vertical channel includes a channel portion with a substantially circular cross-section.

6. The memory cell of claim 5, wherein the substantially circular cross-section has a diameter of between about 0.5 nm to about 15 nm.

7. The memory cell of one of claims 1-6, wherein the field electrode is configured to regulate a discharge current associated with the capacitor.

8. The memory cell of one of claims 1-7, wherein a length of the vertical channel is less than 250 nm.

9. The memory cell of one of claims 1-8, wherein the dielectric is configured to support an electric field along the vertical channel to couple a charge at the first end with a shared doped region.

10. The memory cell of one of claims 1-9, wherein the dielectric is configured to cooperate with at least one of a channel dimension and the channel material to increase the native band gap energy.

11. A system comprising:

a plurality of capacitive cells coupled to an input/output circuit, wherein some of the plurality of capacitive cells include a capacitor coupled to an access transistor comprising a vertical channel region configured to transfer charge between the capacitor and a conductive region based on a signal associated with a processor, and wherein the vertical channel region comprises at least one nanorod configured to reduce a leakage current between the capacitor and the conductive region using a band gap energy difference.

12. The system of claim 11, wherein the at least one nanorod shares a gate region channel material.

13. The system of one of claims 11 or 12, wherein the gate region channel material includes at least one of a dielectric and a gate conductor.

14. The system of one of claims 11-13, wherein the dielectric includes a gate dielectric configured to support an inversion field in the vertical channel region.

15. The system of one of claims 11-14, wherein the at least one nanorod is formed from at least one of a silicon substrate and a silicon wafer.

16. The system of one of claims 11-15, wherein the capacitor includes a double-sided capacitor.

17. The system of one of claims 11-16, wherein the plurality of capacitive cells are configured to form a portion of a memory module.

18. The system of one of claims 11-17, wherein the memory module comprises a DRAM module.

19. The system of one of claims 11-18, wherein the at least one nanorod includes a region with a band gap energy greater than 1.12 eV.

20. A memory unit, comprising:

a channel region comprising at least one nanorod, wherein the at least one nanorod includes a vertical transport region of semiconductor material;

a gate region encompassing at least a portion of the at least one nanorod in the vertical transport region; and

a first drain/source region coupled to the at least one nanorod at an end supporting a capacitor cell.

21. The memory unit of claim 20, wherein the channel region is configured to use a shifted band gap energy.

22. The memory unit of one of claims 20-21, wherein the at least one nanorod is configured to provide a shifted band gap energy.

23. The memory unit of one of claims 20-22, wherein the channel region is configured to reduce an off-state leakage current associated with the capacitor cell.

24. The memory unit of one of claims 20-23, wherein the gate region includes a shared gate material comprising at least one of a gate dielectric and a gate conductor.

25. The memory unit of one of claims 20-24, wherein the gate region is configured to use a common gate electrode.

26. The memory unit of one of claims 20-25, wherein a diameter of the at least one nanorod is between about 0.5 nm and about 20 nm.

27. The memory unit of one of claims 20-26, wherein the vertical transport region includes a portion with a quantization energy that is greater than a bulk band gap energy.

28. The memory unit of one of claims 20-27, wherein the channel region is coupled to a second drain/source region.

29. The memory unit of one of claims 20-27, wherein at least one of a second drain/source region and the least one nanorod is formed from a single crystal semiconductor substrate.

30. The memory unit of one of claims 20-29, wherein the vertical transport region includes at least one of a silicon, silicon germanium, and a silicon carbide.

31. The memory unit of one of claims 20-30, wherein the gate region includes a material comprising at least one of a metal and a polysilicon.

32. The memory unit of one of claims 20-31, wherein the capacitor cell is coupled to at least one of a row access circuit and a column access circuit.

33. A method comprising:

propagating charge through a predefined vertical region in a semiconductor material according to a specified signal, the vertical region coupled to an electrode associated with a capacitor; and

blocking charge flow using the predefined vertical region, wherein the semiconductor material has an electronic energy band gap greater than its native band gap energy.

34. The method of claim 33, wherein propagating includes propagating through at least one nanorod.

35. The method of one of claims 33-34, wherein propagating includes propagating charge to discharge the capacitor.

36. The method of one of claims 33-35, wherein blocking includes blocking charge associated with a leakage current.

37. The method of one of claims 33-36, wherein blocking includes selectively blocking using the electronic energy band gap in combination with a bias field associated with a gate potential.

38. A method comprising:

forming a vertical channel transistor using a first semiconductor material and a second semiconductor material, the first semiconductor material incorporating a nanorod geometry to increase an electronic energy gap of the first semiconductor material, and the second semiconductor material having a native electronic band gap energy less than the electronic band gap energy of the first semiconductor material; and

forming a gate region enclosing a portion of first semiconductor material.

39. The method of claim 38, wherein forming a vertical channel transistor includes forming with a material that includes silicon.

40. The method of one of claims 38-39, wherein forming a vertical channel transistor using the first semiconductor material includes using a first semiconductor material with the same lattice constant as silicon.

41. The method of one of claims 38-40, wherein forming a vertical transistor channel includes forming using a self assembled layer.

42. A method comprising:

forming an access transistor comprising at least one vertical nanorod;

forming a capacitor cell supported by the access transistor; and

connecting the access transistor to the capacitor cell using a plurality of electrodes.

43. The method of claim 42, wherein forming an access transistor includes forming an annular gate structure.

44. The method of claim 43, wherein forming an annular gate structure includes forming an annular gate dielectric and an annular gate electrode.

45. The method of one of claims 42-44, wherein forming an access transistor includes forming a shared drain/source region.

46. The method of one of claims 42-45, wherein forming an access transistor includes removing material using a spacer layer.

47. The method of claim 46, wherein removing includes removing material supported by a substrate.

48. The method of one of claims 46-47, wherein removing includes removing at least one of a substrate material and a portion of a semiconductor wafer.

49. The method of one of claims 42-48, wherein forming an access transistor includes first forming the at least one vertical nanorod.

50. The method of one of claims 42-49, wherein connecting the access transistor includes coupling the at least one nanorod to the capacitor cell using a capacitor plate.

51. The method of one of claims 42-49, wherein connecting the access transistor includes connecting the access transistor to the capacitor cell using a gate electrode.

52. A memory cell comprising:

an access transistor adjacent to a substrate layer, the access transistor comprising at least one vertical channel shaped as a rod, the at least one vertical channel sharing a gate electrode and at least one drain/source region with another vertical channel; and

a capacitor coupled to one end of the access transistor.

53. The memory cell of claim 52, wherein the gate electrode encloses a region including a quantized band gap energy.

54. The memory cell of one of claims 52-53, wherein the at least one vertical channel is formed from the substrate layer.

55. The memory cell of one of claims 52-54, wherein the substrate layer is a silicon wafer.

56. The memory cell of one of claims 52-55, wherein the at least one vertical channel, the substrate layer, and the at least one drain/source region are formed with materials having the same lattice constant.

57. The memory cell of one of claims 52-56, wherein the at least one vertical channel, the substrate layer, and the at least one drain/source region are a formed of a single material.

58. A method comprising:

establishing a first electric field in a vertical electron channel;

establishing a second electric field in the vertical electron channel to discharge a capacitor, wherein the vertical electron channel includes a semiconductor material with a first band gap energy greater than silicon, and wherein the vertical electron channel is coupled to a region of material with a second band gap energy lower than the first band gap energy, and wherein at least one of the vertical electron channel and the region of material have a lattice constant equal to silicon.

59. The method of claim 58, wherein establishing a first electric field includes establishing a charge on a capacitor plate.

60. The method of claim 59, wherein establishing a charge includes establishing a charge on the capacitor plate associated with a double sided capacitor.

61. The method of one of claims 58-60, wherein establishing a first electric field includes establishing a charge on a capacitor plate.

62. The method of one of claims 58-61, wherein establishing a first electric field includes establishing a first electric field with a vertical potential gradient.

63. The method of one of claims 58-62, wherein establishing a second electric field includes discharging a capacitor associated with a dynamic read only memory cell.

64. The method of one of claims 58-63, wherein establishing a second electric field includes establishing a second electric field with a radial potential gradient.

65. A system comprising:

a user interface coupled to a memory, the memory comprising a plurality of capacitor cells, at least a portion of the capacitor cells including at least one access transistor, the access transistor comprising at least one vertical channel shaped as a rod, wherein the rod includes a first band gap energy region and a second band gap energy region, the second band gap energy being lower than the first band gap energy, and wherein the first band gap energy region and the second band gap energy region cooperate to reduce a channel leakage current.

66. The system of claim 65, wherein the user interface is coupled to at least one of a personal digital assistant, a cell phone, a television, a computer and a network server.

67. The system of one of claims 65-66, wherein the user interface is configured to receive a signal associated with at least one of a processor and a modem.

68. The system of one of claims 65-67, wherein the user interface is configured to transmit a signal to at least one of a processor, a display and a storage device.

What is claimed is:

1. A memory cell, comprising:

a vertical channel comprising at least one nanorod that includes a vertical transport region of a semiconductor material, the vertical channel coupled at a first end of the vertical channel to a capacitor, the vertical channel configured to increase a native band gap energy of the semiconductor material forming the channel, wherein the semiconductor material consists of a SiGeC layer contacting and extending vertically from a SiC layer;

a dielectric substantially surrounding the vertical channel; and

a field electrode coupled to the vertical channel using the dielectric.

2. The memory cell of claim 1, wherein the capacitor is a double-sided capacitor associated with a dynamic random access memory.

3. The memory cell of claim 1, wherein the vertical channel is coupled to the capacitor using at least one shared doped region.

4. The memory cell of claim 3, wherein the at least one doped region is formed from a silicon substrate.

5. The memory cell of claim 1, wherein the vertical channel includes a channel portion with a substantially circular cross-section.

6. The memory cell of claim 5, wherein the substantially circular cross-section has a diameter of between about 0.5 nm to about 15 nm.

7. The memory cell of claim 1, wherein the field electrode is configured to regulate a discharge current associated with the capacitor.

8. The memory cell of claim 1, wherein a length of the vertical channel is less than 250 nm.

9. The memory cell of claim 1, wherein the dielectric is configured to support an electric field along the vertical channel to couple a charge at the first end with a shared doped region.

10. A memory unit, comprising:

a channel region comprising at least one nanorod, wherein the at least one nanorod includes a vertical transport region of semiconductor material, the semiconductor material of the vertical transport region having a band gap energy increased from its native band gap energy in bulk form, wherein the semiconductor material consists essentially of a SiGeC layer contacting and extending vertically from a SiC layer;

a gate region encompassing at least a portion of the at least one nanorod in the vertical transport region;

a dielectric contacting the channel region, the dielectric including one or more oxynitrides of Mo, W, Ta, Hf, or Al; and

a first drain/source region coupled to the at least one nanorod at an end supporting a capacitor cell.

11. The memory unit of claim 10, wherein the first drain/source region has a size sufficiently large such that the first drain/source region is without quantum size effects.

12. The memory unit of claim 10, wherein the channel region is on and contacting a second drain/source region, the second drain/source region coupled to a ground plane by a via through a substrate on which components of the memory unit are disposed.

13. The memory unit of claim 10, wherein the channel region is configured to reduce an off-state leakage current associated with the capacitor cell.

14. The memory unit of claim 10, wherein the gate region includes a shared gate material comprising at least one of a gate dielectric and a gate conductor.

15. The memory unit of claim 10, wherein the gate region is configured to use a common gate electrode.

16. The memory unit of claim 10, wherein a diameter of the at least one nanorod is between about 0.5 nm and about 20 nm.

17. The memory unit of claim 10, wherein the channel region, the gate region, the

dielectric, and the first drain/source region are disposed on a single crystal silicon substrate.

18. The memory unit of claim 10, wherein the channel region is coupled to a second drain/source region.

19. The memory unit of claim 18, wherein at least one of the second drain/source region or the at least one nanorod is formed from a single crystal semiconductor substrate.

20. The memory unit of claim 10, wherein the vertical transport region includes at least one of a silicon, silicon germanium, or a silicon carbide.

21. The memory unit of claim 10, wherein the gate region includes a material comprising at least one of a metal and a polysilicon.

22. The memory unit of claim 10, wherein the capacitor cell is coupled to at least one of a row access circuit and a column access circuit.

23. A memory cell comprising:

an access transistor adjacent to a substrate layer, the access transistor comprising at least one vertical channel shaped as a nanorod that includes a vertical transport region of semiconductor material, the at least one vertical channel configured to increase a native band gap energy of the semiconductor material forming the vertical channel, the at least one vertical channel sharing a gate electrode and at least one drain/source region with another vertical channel, the at least one vertical channel substantially surrounded by a dielectric, wherein the semiconductor material consists of a SiGeC layer contacting and extending vertically from a SiC layer; and

a capacitor coupled to one end of the access transistor.

24. The memory cell of claim 23, wherein the gate electrode encloses a region including a quantized band gap energy.

25. The memory cell of claim 23, wherein the at least one vertical channel is formed from the substrate layer.

26. The memory cell of claim 23, wherein the substrate layer is a silicon wafer.

27. The memory cell of claim 23, wherein the at least one vertical channel, the substrate layer, and the at least one drain/source region are formed with materials having the same lattice constant.

28. The memory cell of claim 23, wherein the at least one vertical channel, the substrate layer, and the at least one drain/source region are formed of a single material.