CLAIMS

What is claimed is:

1. A memory system, comprising:

a memory device comprising memory cells,

a memory controller coupled to the memory device,

a power loss protection (PLP) circuit, and

a discharge circuit coupled to an output of the PLP circuit, wherein the discharge circuit comprises one or more discharge paths configured to discharge at least one of the PLP circuit, the memory device, or the memory controller.

2. The memory system of claim 1, wherein a first discharge path of the one or more discharge paths comprises:

a first resistor coupled to the output of the PLP circuit, and

a first transistor coupled to a first switch transistor, wherein a gate of the first switch transistor is coupled to a first voltage dividing circuit, wherein the first voltage dividing circuit is configured to generate a divided voltage of the output of the PLP circuit, and wherein a terminal of the first switch transistor is coupled to the output of the PLP circuit.

3. The memory system of claim 2, wherein the first voltage dividing circuit comprises two resistors connected in series, wherein a first end of the first voltage dividing circuit is coupled to the output of the PLP circuit, and a second end of the first voltage dividing circuit is coupled to ground.

4. The memory system of claim 2, wherein a second discharge path of the one or more discharge paths comprises:

a second resistor coupled to an enable pin of a voltage converter configured to activate the voltage converter, wherein the voltage converter is configured to generate a voltage for the memory controller based on the output of the PLP circuit, and

a second transistor coupled to the first switch transistor.

5. The memory system of claim 2, wherein a third discharge path of the one or more discharge paths comprises:

a third resistor coupled to the memory device, and

a third transistor coupled to the first switch transistor.

6. The memory system of claim 2, wherein the PLP circuit comprises a capacitor, wherein the PLP circuit is configured to:

charge the capacitor when an external power source is turned on, and

discharge the capacitor to provide power for the memory system when the external power source is turned off.

7. The memory system of claim 6, wherein a fourth discharge path of the one or more discharge paths comprises:

a fourth resistor coupled to the output of the PLP circuit, and

a fourth transistor coupled to a second switch transistor, wherein a gate of the second switch transistor is coupled to the first voltage dividing circuit, and wherein a terminal of the second switch transistor is coupled to a second voltage dividing circuit configured to generate a divided voltage of a voltage of the capacitor.

8. The memory system of claim 7, wherein a fifth discharge path of the one or more discharge paths comprises:

a fifth resistor coupled to the capacitor, and

a fifth transistor coupled to the second switch transistor.

9. The memory system of claim 1, wherein the memory device, the memory controller, the PLP circuit and the discharge circuit are placed on a printed circuit board, wherein the discharge circuit is distanced from the PLP circuit on the printed circuit board.

10. The memory system of claim 8, wherein the discharge circuit is coupled to at least one of:

a capacitor of the PLP circuit,

an enable pin of a voltage converter, and

the memory device.

11. A memory system, comprising:

a memory device comprising memory cells,

a memory controller coupled to the memory device,

a power loss protection (PLP) circuit configured to provide power for the memory system when an external power source is turned off, and

a discharge circuit configured to:

in response to determining that an output voltage of the PLP circuit is lower than a first threshold, discharge at least one of the PLP circuit, the memory device or the memory controller.

12. The memory system of claim 11, wherein the discharge circuit comprises one or more discharge paths each comprising a transistor and a resistor.

13. The memory system of claim 12, wherein discharging at least one of the PLP circuit, the memory device or the memory controller comprises:

discharging the PLP circuit through a first discharge path of the discharge circuit,

discharging a first voltage line through a second discharge path of the discharge circuit, wherein the first voltage line is configured to activate a voltage converter configured to generate a voltage for the memory controller based on the output voltage of the PLP circuit, and

discharging a second voltage line through a third discharge path of the discharge circuit, wherein the second voltage line is configured to provide power for the memory device.

14. The memory system of claim 13, wherein the PLP circuit comprises a capacitor, and wherein the discharge circuit is configured to:

in response to determining that the output voltage of the PLP circuit is lower than a second threshold and that a voltage of the capacitor is higher than a third threshold:

discharge the PLP circuit through a fourth discharge path of the discharge circuit, and

discharge the capacitor through a fifth discharge path of the discharge circuit.

15. The memory system of claim 13, wherein the discharge circuit is configured to:

in response to determining that the output voltage of the PLP circuit is higher than a fourth threshold and lower than the first threshold, discharge the PLP circuit through the first discharge path.

16. The memory system of claim 14, wherein the first discharge path, the second discharge path and the third discharge path are coupled to a first switch transistor,

wherein a gate of the first switch transistor is coupled to a first voltage dividing circuit configured to generate a divided voltage of the output voltage of the PLP circuit, and wherein a terminal of the first switch transistor is coupled to an output of the PLP circuit.

17. The memory system of claim 16, wherein the fourth discharge path and the fifth discharge path are coupled to a second switch transistor,

wherein a gate of the second switch transistor is coupled to the first voltage dividing circuit, wherein a terminal of the second switch transistor is coupled to a second voltage dividing circuit configured to generate a divided voltage of a voltage of the capacitor.

18. A method of discharging a memory system, comprising:

in response to determining that an output voltage of a power loss protection (PLP) circuit of the memory system is lower than a first threshold, discharging, by a discharge circuit, at least one of the PLP circuit, a memory device of the memory system, or a memory controller of the memory system,

wherein the discharge circuit is distanced from the PLP circuit.

19. The method of claim 18, wherein discharging at least one of the PLP circuit, the memory device or the memory controller comprises:

in response to determining that the output voltage of the PLP circuit is lower than the first threshold, discharging the PLP circuit through a first discharge path of the discharge circuit, and

in response to determining that the output voltage of the PLP circuit is lower than a second threshold and that a voltage of a capacitor of the PLP circuit is higher than a third threshold, discharging the PLP circuit through a fourth discharge path of the discharge circuit.

20. The method of claim 19, comprising:

in response to determining that the output voltage of the PLP circuit is higher than a fourth threshold and lower than the first threshold, discharging the PLP circuit through the first discharge path.