A METHOD FOR MAKING LOW-LEAKAGE DRAM STRUCTURES USING SELECTIVE SILICON EPITAXIAL GROWTH (SEG) ON AN INSULATING LAYER

ABSTRACT

Low current leakage DRAM structures are achieved using a selective silicon epitaxial growth over an insulating layer on memory cell (device) areas. An insulating layer, that also serves as a stress-release layer, and a Si_3N_4 hard mask are patterned to leave portions over the memory cell areas. Shallow trenches are etched in the substrate and filled with a CVD oxide which is polished back to the hard mask to form shallow trench isolation (STI) around the memory cell areas. The hard mask is selectively removed to form recesses in the STI aligned over the memory cell areas exposing the underlying insulating layer. Openings are etched in the insulating layer to provide a silicon-seed surface from which is grown a selective epitaxial layer extending over the insulating layer within the recesses. After growing a gate oxide on the epitaxial layer, FETs and DRAM capacitors can be formed on the epitaxial layer. The insulating layer under the epitaxial layer drastically reduces the capacitor leakage current and improves DRAM device performance. This self-aligning method also increases memory cell density, and is integratable into current DRAM processes to reduce cost.

Figure 2