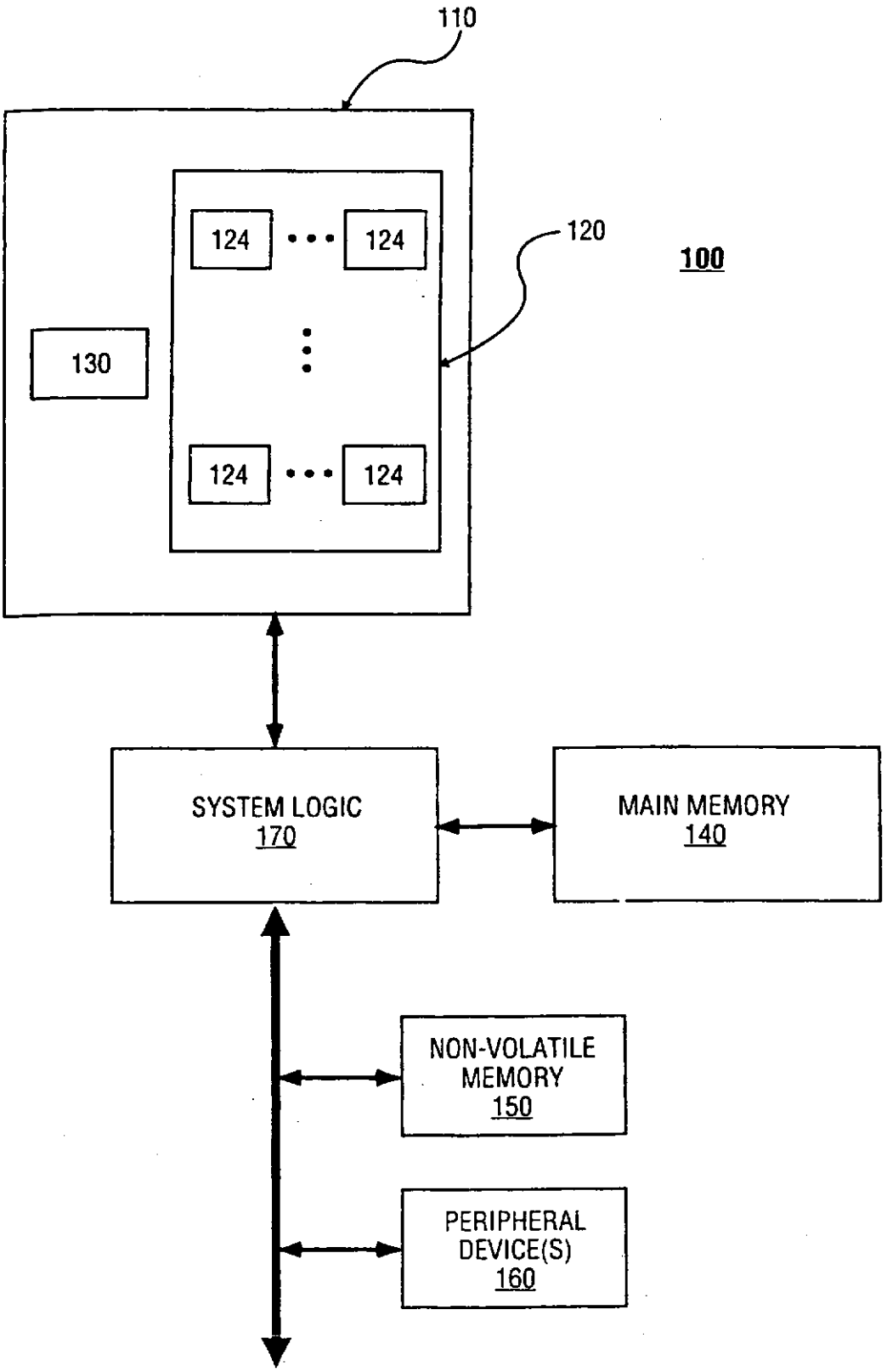

110
120
100
124
124
130
124
124
SYSTEM LOGIC
170
MAIN MEMORY
140
NON-VOLATILE
MEMORY
150
PERIPHERAL
DEVICE(S)
160

FIG. 1

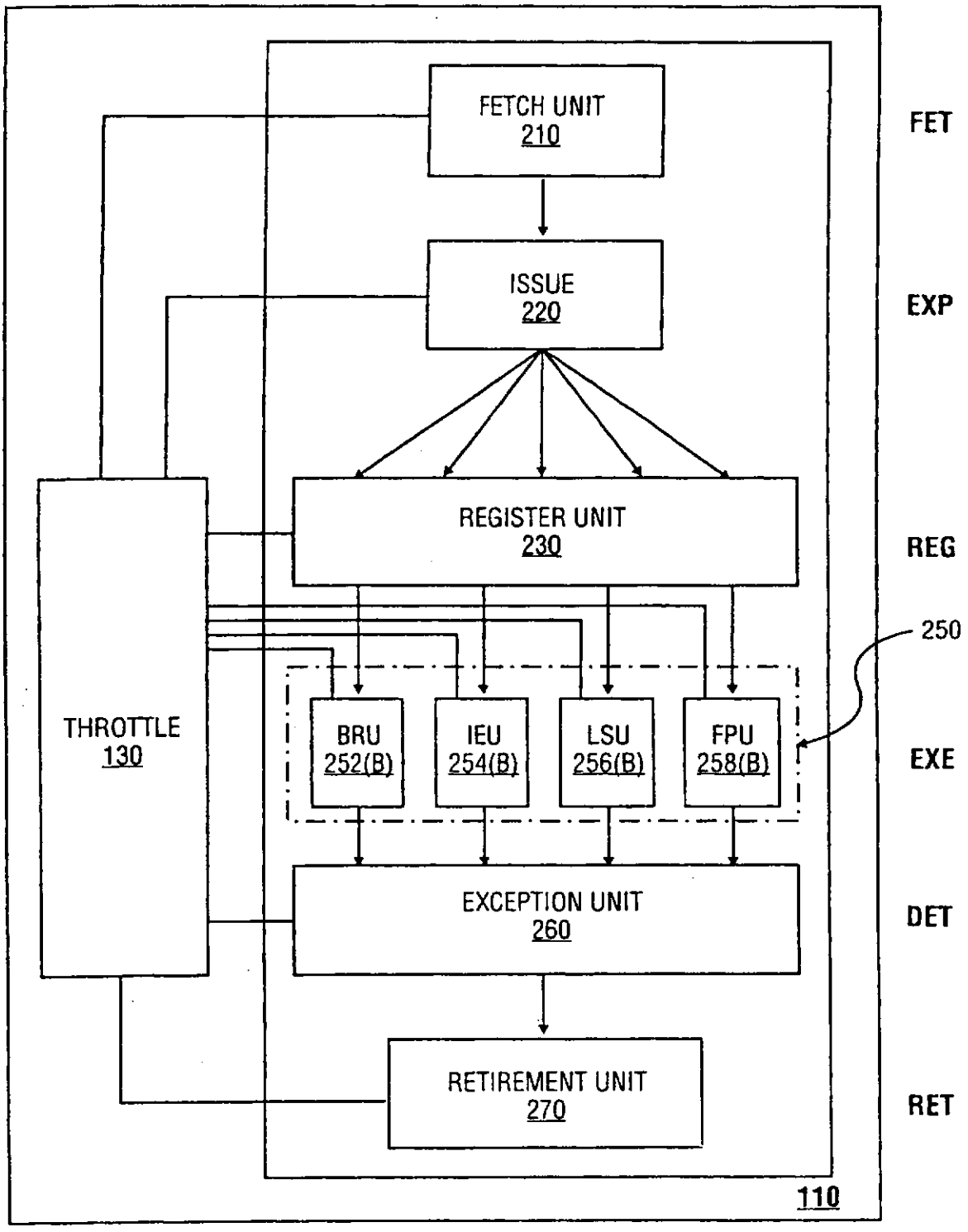

FETCH UNIT
210
ISSUE
220
REGISTER UNIT
230
THROTTLE
130
BRU
252(B)
IEU
254(B)
LSU
256(B)
FPU
258(B)
EXCEPTION UNIT
260
RETIREMENT UNIT
270
110
FET
EXP
REG
250
EXE
DET
RET

FIG. 2

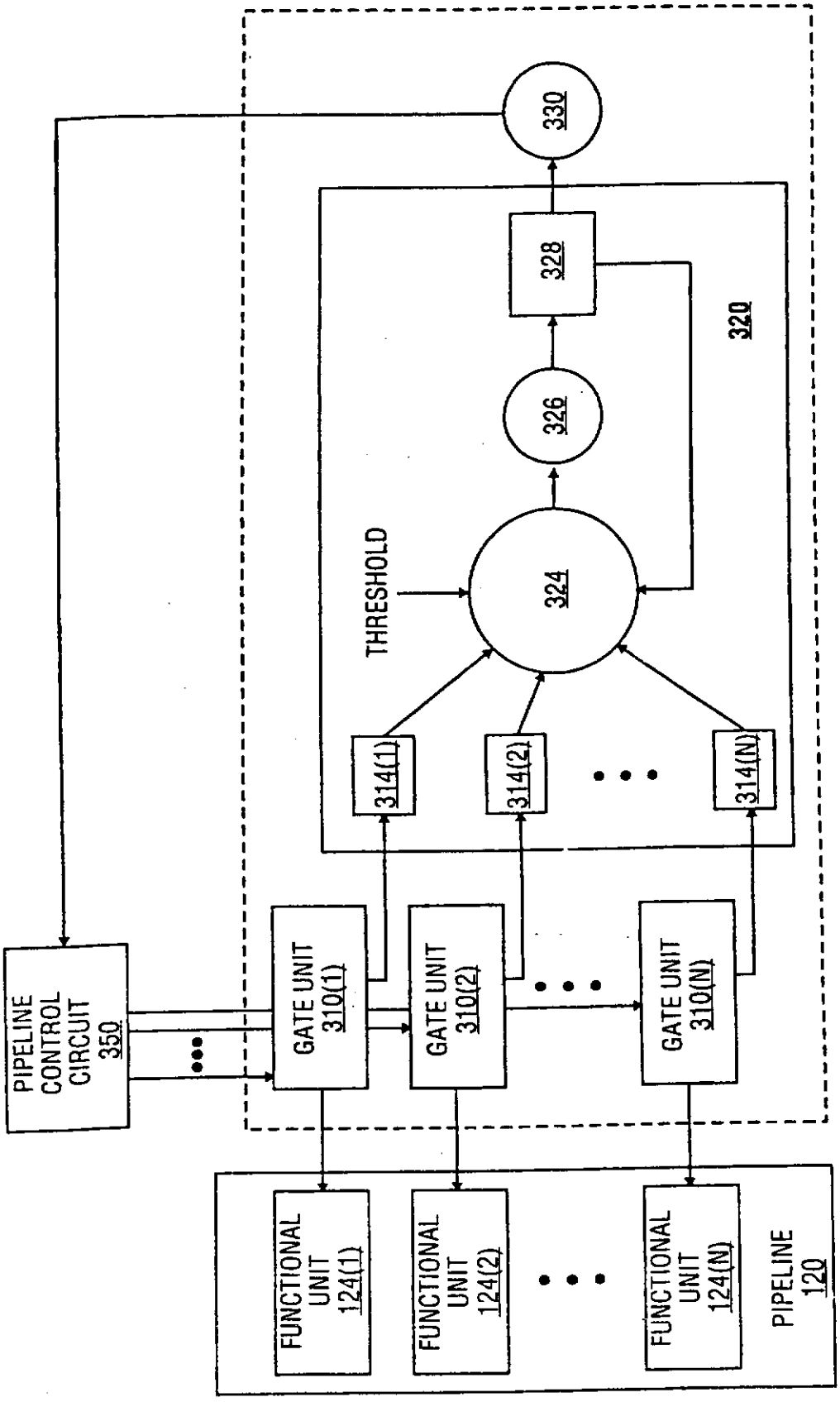

330
328
320
326
THRESHOLD
324
314(1)
314(2)
314(N)
PIPELINE CONTROL CIRCUIT 350
GATE UNIT 310(1)
GATE UNIT 310(2)
GATE UNIT 310(N)
FUNCTIONAL UNIT 124(1)
FUNCTIONAL UNIT 124(2)
FUNCTIONAL UNIT 124(N)
PIPELINE 120

FIG. 3

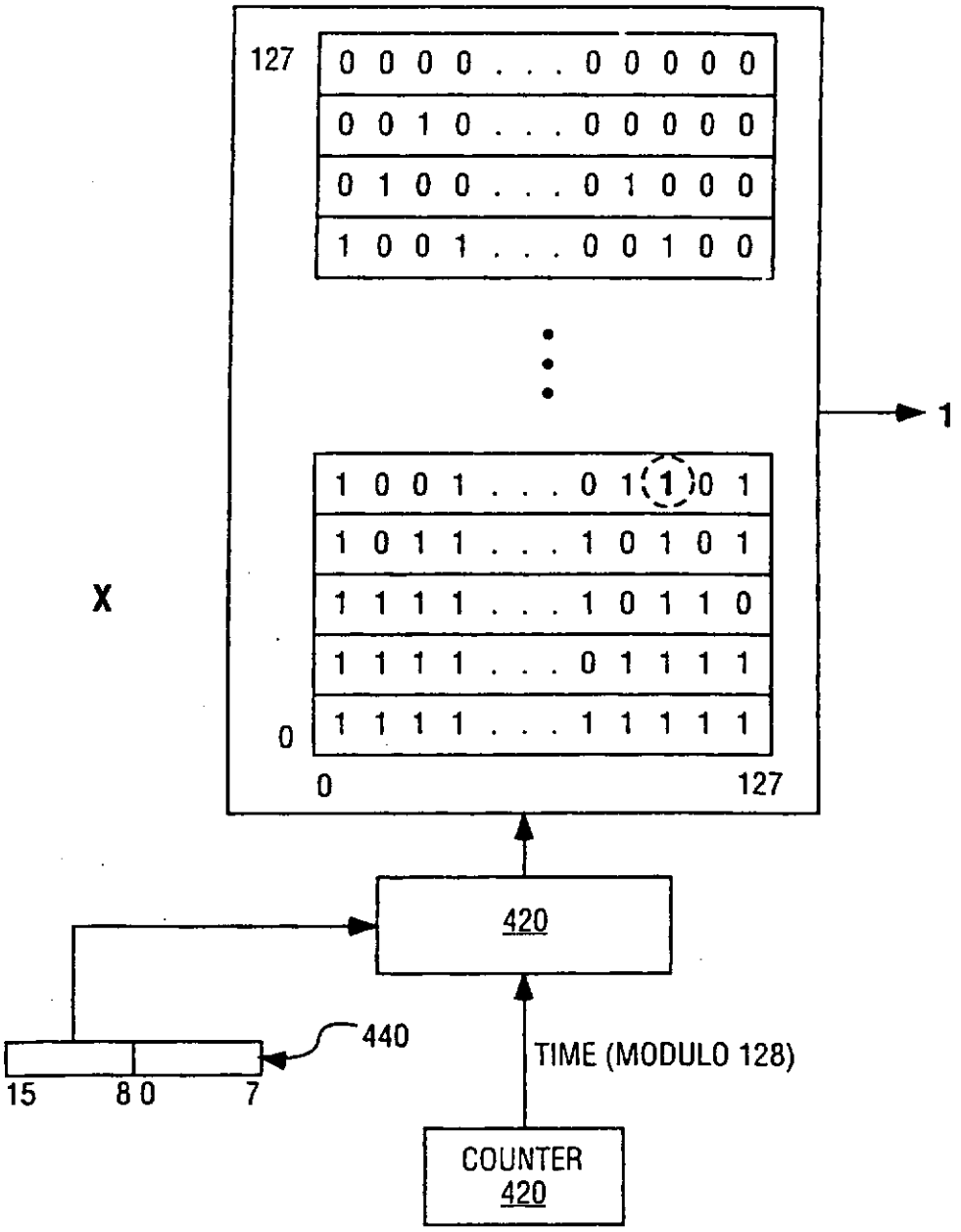

127
0 0 0 0 . . . 0 0 0 0 0
0 0 1 0 . . . 0 0 0 0 0
0 1 0 0 . . . 0 1 0 0 0
1 0 0 1 . . . 0 0 1 0 0
1
X
1 0 0 1 . . . 0 1 1 0 1
1 0 1 1 . . . 1 0 1 0 1
1 1 1 1 . . . 1 0 1 1 0
1 1 1 1 . . . 0 1 1 1 1
1 1 1 1 . . . 1 1 1 1 1
0
0
127
420
440
15 8 0 7
TIME (MODULO 128)
COUNTER
420

FIG. 4

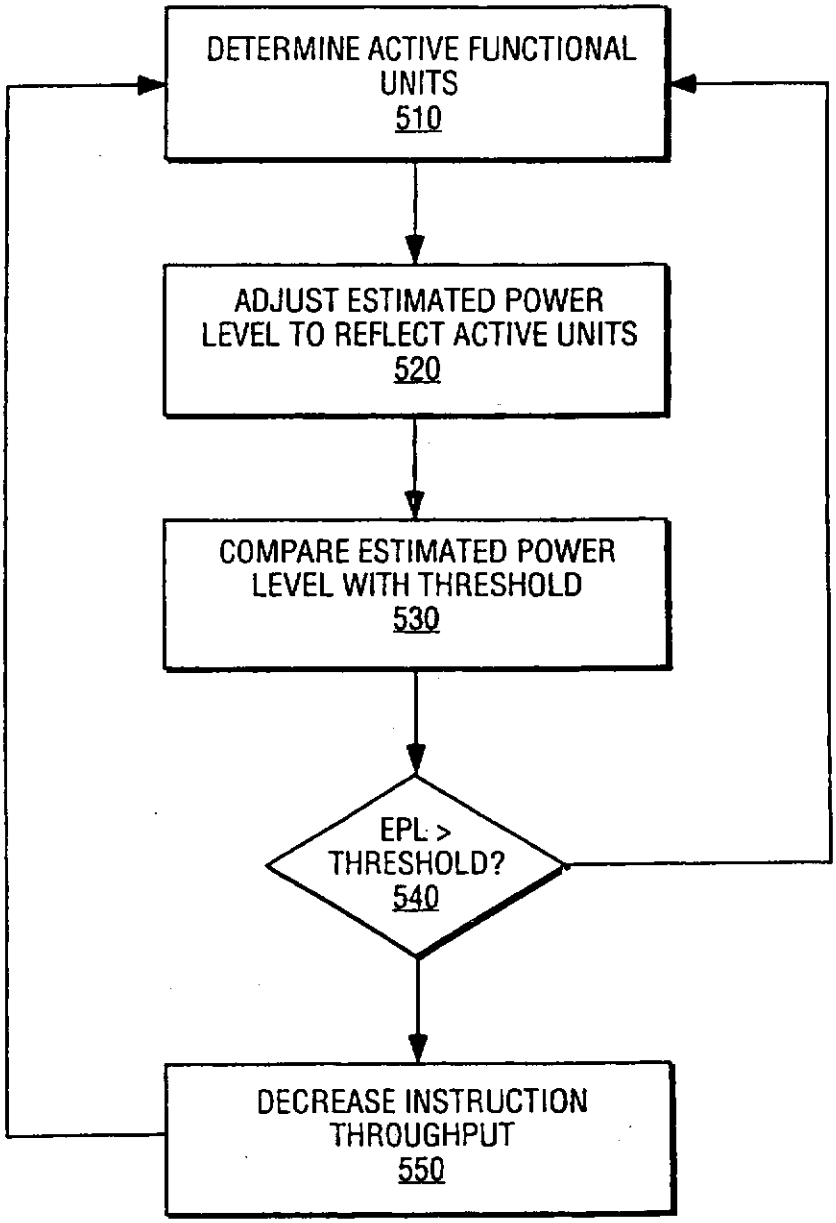

DETERMINE ACTIVE FUNCTIONAL UNITS
510
ADJUST ESTIMATED POWER LEVEL TO REFLECT ACTIVE UNITS
520
COMPARE ESTIMATED POWER LEVEL WITH THRESHOLD
530
EPL > THRESHOLD?
540
DECREASE INSTRUCTION THROUGHPUT
550

FIG. 5

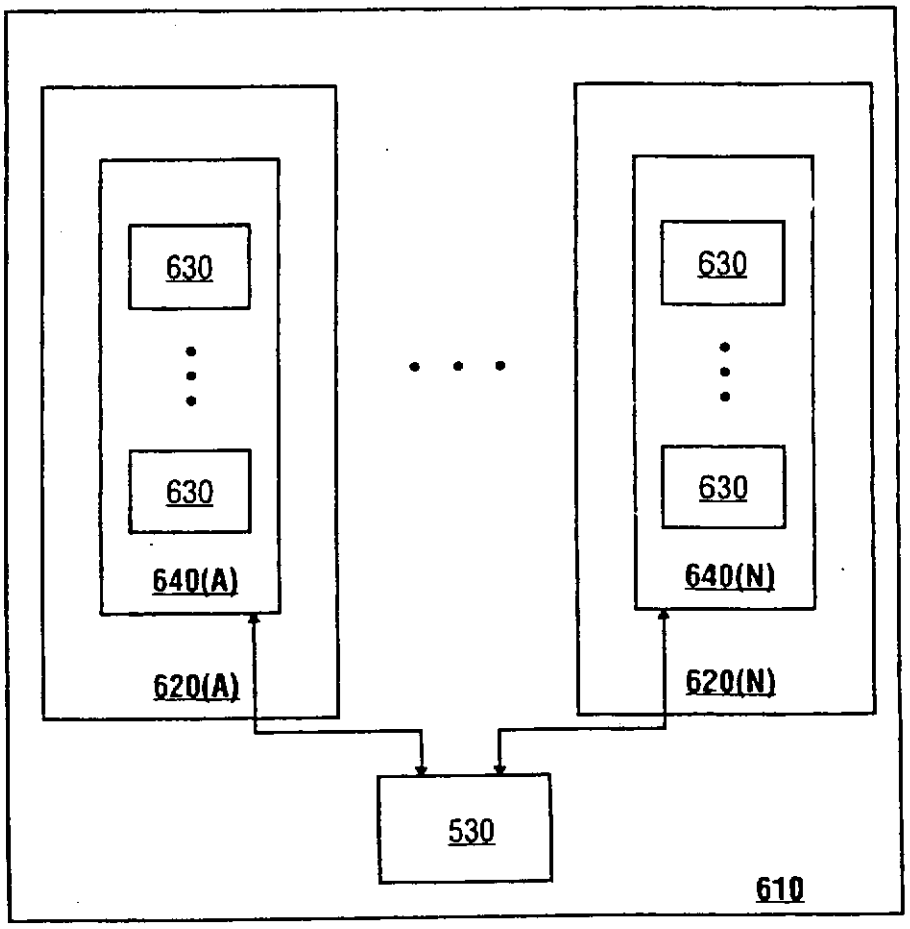

630
630
640(A)
620(A)
630
630
640(N)
620(N)
530
610

FIG. 6A

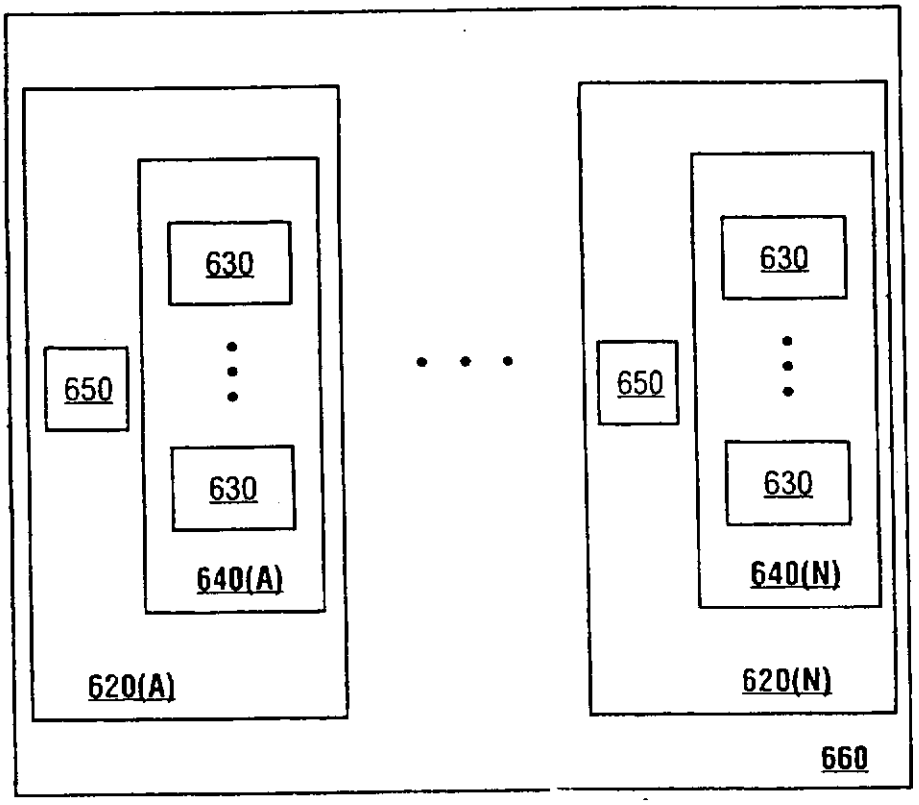

630
650
630
640(A)
620(A)
630
650
630
640(N)
620(N)
660

FIG. 6B