## Description

The present invention relates to the production of semiconductor devices, which includes sealing of the back side of a semiconductor wafer prior to growing an epitaxial layer on the opposite (front) side thereof.

In the production of integrated circuits and other semiconductor devices, an epitaxial layer on a silicon wafer is frequently used for the formation of the device structures in whole or in part. This allows, for example, a difference in the doping for the epitaxial layer as compared to the silicon wafer (substrate) on which it is formed. In order to form an epitaxial layer on a silicon wafer, the wafer is typically subjected to a high temperature while a carrier gas comprising the desired epitaxial material is flowed across the wafer, resulting in the chemical vapor deposition (CVD) of the desired material onto the wafer.

The high temperatures used in the epitaxial process tend to cause dopants present in the wafer to diffuse out of the back side of the wafer and into the surrounding vapor, and from there into the epitaxial layer being formed on the front side. This "autodoping", as it is referred to in the art, then changes the doping level in the epitaxial layer from its desired value. This is especially of concern when the desired doping in the epitaxial layer is much less than that of the wafer. For example, for the production of dynamic random access memories, a lightly doped p-type epitaxial layer is frequently formed on a more heavily doped p-type wafer. If an excessive amount of p-dopant transfers to the epitaxial layer by autodoping, then its doping level will exceed the desired level. In one typical process, the doping of the wafer is at least $10^{18}$ atoms of boron per cubic centimeter, and the doping of the epitaxial layer is less than $10^{16}$ boron atoms per cubic centimeter; see U.S. Patent 4,216,489.

To reduce autodoping, it is known in the art to grow a "cap" on the backside of the wafer prior to the epitaxial deposition process. The cap is one or more layers that are relatively impervious to the dopant in the wafer. The outdiffusion of the dopant from the wafer is thereby reduced. For capping a silicon wafer, the prior art technique typically calls for first thermally growing an oxide layer on the back side of the wafer by furnace heating the wafer to a high temperature, typically about 1050 degrees C, in an oxygen ambient. The wafer is then transported to a separate low pressure chemical vapor deposition (LPCVD) furnace for deposition of the silicon nitride cap at a lower temperature than that used for the oxide growth. The silicon nitride layer, being relatively impervious to the commonly used dopants, provides most of the protection against dopant outgassing. The silicon dioxide layer is included mainly to provide strain relief between the silicon wafer and the nitride cap, and to facilitate subsequent removal of the nitride cap after the epitaxial process is completed.

It is very important that the resulting structure be of high crystallographic quality. That is, the epitaxial deposition process should continue the single crystal structure of the wafer without introducing additional faults into either the wafer or the epitaxial layer. Hence, the capping process itself should not promote any mechanism that will have a significant adverse effect on crystal quality, either during the epitaxial layer formation, or during subsequent device processing steps. One known factor affecting quality is the presence of oxygen in the crystal. It is generally desirable to have some oxygen present in the silicon wafer, in order to "getter" defects before they propagate to the active surface of the wafer. For example, an oxygen concentration of at least 10 parts per million is presently desirable. On the other hand, oxygen itself can produce defects, particularly if it precipitates out of the crystal lattice prior to polishing the front side of the wafer. However, after polishing, some precipitation is desirable to promote the gettering. Such precipitation may occur due to the high temperature and long time required for the epitaxial deposition process, or during subsequent process heating steps.

The amount of oxygen typically varies as a function of position in the silicon ingot from which the wafers are cut. The top portion of the ingot typically contains the highest oxygen concentration, when grown by the Czochralski technique. For the production of integrated circuit dynamic memories, it is known in some cases to use only the bottom half of the ingot for wafers on which epitaxial layers are to be formed, in order to reduce the oxygen precipitation problem.

This requires sorting the wafers into groups, and adds extra costs to the production process. It also reduces the number of available wafers for use in the epitaxial process for a given number of silicon ingots grown.

Journal Electrochem. Soc. 126, No. 6 pages 1042-1046 discusses the deposition of $SiO_2$ films from TEoS gas at reduced pressure and fixed temperature. The deposition rate for both doped and undoped films, as well as the thickness uniformity are studied.

FR-A- 2 454 697 discloses epitaxial growth and the deposition of silicon dioxide and silicon nitride layers. The $SiO_2$ is deposited at temperatures above 1000°C.

According to the present invention there is provided a method as defined in claim 1.

This invention embodies production of semiconductor devices which involves capping a semiconductor wafer wherein a layer of silicon dioxide is deposited at a relatively low temperature on the back side of the wafer during the ramp-up in temperature of a LPCVD furnace. A layer of silicon nitride is then deposited on the silicon dioxide at the elevated temperature resulting from the ramp-up. The deposition of

the silicon dioxide is preferably accomplished by low pressure chemical vapor deposition using tetra ethoxy silane (TEOS).

FIG. 1 shows a furnace system suitable for use with the present invention.

FIG. 2 shows a typical temperature profile used in practicing the present invention.

The following detailed description relates to an improved method for capping semiconductor wafers to prevent outdoping during a subsequent epitaxial growth process. The improved technique provides for reduced oxygen precipitation, while shortening the time required for the capping process. This is achieved by making use of the ramp-up period of the furnace used for subsequent silicon nitride deposition. The temperature during this period is less than that used in prior-art capping processes. According to known principles, the amount of oxygen precipitation is reduced according to the reduction of the time-temperature product to which the semiconductor wafer is subjected. Hence, a time period otherwise not used for this purpose provides a useful environment for forming the silicon dioxide cap layer.

Referring to FIG. 1, semiconductor wafers (100), such a silicon wafers, are placed by pairs into wafer boats (101), so that the active face of one wafer contacts the active face of another. This helps ensure that the subsequently formed cap will not form on the active side of each wafer, but only on the exposed (back) side. The wafer boats are then covered to increase the uniformity of the deposits. The boats are loaded into the furnace (102), which may be of a conventional quartz tube type, so as to reside in the "hot zone". A vacuum is applied to a vacuum inlet (103). The TEOS used for the oxide deposition is supplied to the furnace from a bubbler (104). The nitrogen and silicon used for the nitride deposition are supplied from a source (105) of ammonia ($NH_3$) and a source (106) of dichlorosilane ($SiH_2Cl_2$), with other source gasses being possible. The flow of the source gasses into the furnace is regulated by mass flow controllers (107, 108).

Referring to FIG. 2, the temperature of the furnace is ramped up from the idling temperature of about 650 degrees C while the vacuum source pumps down the pressure to about 2.67 to 4.00 Pa (20 to 30 millitorr) base pressure. After about 5 minutes into the ramp-up, the TEOS is introduced into the furnace, while continuing to apply a vacuum. The flow of the TEOS produces a desired pressure of about 33.33 to 40.00 Pa (250 to 300 millitorr), resulting in a deposition of $SiO_2$ at a rate of about 5 nanometers per minute. The TEOS flow continues for about 5 minutes, resulting in a total deposit of about 25 nanometers of $SiO_2$. After the termination of the TEOS flow about 10 minutes into the ramp-up, the temperature continues to increase to about 775 degrees C.

At about 12 minutes into the cycle, the $NH_3$ is introduced into the furnace at a flow rate of about 300 cubic centimeters per minute, and the $SiH_2Cl_2$ is introduced at a flow rate of about 30 cubic centimeters per minute. This results in a deposition of the silicon nitride cap layer at a rate of about 2.9 nanometers per minute. The pressure during this deposition is about 38.66 Pa (290 millitorr). This deposition continues for about 17 minutes, resulting in a silicon nitride cap about 50 nanometers thick. The flow of the source gasses is then stopped, and the furnace pumped down to the base pressure to clean the furnace tube. The flow controllers for the source gasses are purged by a flow of $N_2$, while the temperature is ramped down to the idling value. The furnace is filled with $N_2$ gas at atmospheric pressure, and the wafer boats removed from the furnace.

Following the present capping technique, the front side of the wafers are polished to provide a highly specular, damage-free surface. This is typically accomplished by polishing the front side of the wafer using a caustic slurry as a polishing agent. They are then ready for the epitaxial growth process according to procedures known in the art. Although silicon, including dopants as desired, is typically grown as the epitaxial layer, other materials are possible. For example, the epitaxial growth of germanium and/or group III-V semiconductor materials on silicon wafers is being explored by workers in the art, and can benefit from the use of silicon wafers capped according to the present technique. A review of some current epitaxial techniques is given in "Low-Pressure Chemical Vapor Deposition", S. D. Hersee et al, Annual Review of Materials Science Vol. 12, pp. 65-80 (1982). The resulting wafers may then be used for integrated circuit production, or for the production of various other semiconductor devices.

## Claims

1. A method of capping the back side of a semiconductor wafer in preparation for forming an epitaxial layer of a semiconductor material on the front side of said wafer, comprising the steps of:

introducing said wafer into a furnace:

increasing the temperature in said furnace while introducing a source gas comprising a silicon compound and a source of oxygen into said furnace, thereby depositing silicon dioxide onto at least the back side of said wafer at a temperature below 775 degrees C during said temperature increase;

terminating said source gas flow and continuing to increase the temperature in said furnace; and

maintaining said furnace temperature and introducing a gaseous source of silicon and of nitrogen into said furnace, thereby depositing silicon nitride onto said silicon dioxide.

2. The method according to claim 1,

the silicon dioxide is preferably accomplished by low pressure chemical vapor deposition using tetra ethoxy silane (TEOS).

FIG. 1 shows a furnace system suitable for use with the present invention.

FIG. 2 shows a typical temperature profile used in practicing the present invention.

The following detailed description relates to an improved method for capping semiconductor wafers to prevent outdoping during a subsequent epitaxial growth process. The improved technique provides for reduced oxygen precipitation, while shortening the time required for the capping process. This is achieved by making use of the ramp-up period of the furnace used for subsequent silicon nitride deposition. The temperature during this period is less than that used in prior-art capping processes. According to known principles, the amount of oxygen precipitation is reduced according to the reduction of the time-temperature product to which the semiconductor wafer is subjected. Hence, a time period otherwise not used for this purpose provides a useful environment for forming the silicon dioxide cap layer.

Referring to FIG. 1, semiconductor wafers (100), such a silicon wafers, are placed by pairs into wafer boats (101), so that the active face of one wafer contacts the active face of another. This helps ensure that the subsequently formed cap will not form on the active side of each wafer, but only on the exposed (back) side. The wafer boats are then covered to increase the uniformity of the deposits. The boats are loaded into the furnace (102), which may be of a conventional quartz tube type, so as to reside in the "hot zone". A vacuum is applied to a vacuum inlet (103). The TEOS used for the oxide deposition is supplied to the furnace from a bubbler (104). The nitrogen and silicon used for the nitride deposition are supplied from a source (105) of ammonia ($NH_3$) and a source (106) of dichlorosilane ($SiH_2Cl_2$), with other source gasses being possible. The flow of the source gasses into the furnace is regulated by mass flow controllers (107, 108).

Referring to FIG. 2, the temperature of the furnace is ramped up from the idling temperature of about 650 degrees C while the vacuum source pumps down the pressure to about 2.67 to 4.00 Pa (20 to 30 millitorr) base pressure. After about 5 minutes into the ramp-up, the TEOS is introduced into the furnace, while continuing to apply a vacuum. The flow of the TEOS produces a desired pressure of about 33.33 to 40.00 Pa (250 to 300 millitorr), resulting in a deposition of $SiO_2$ at a rate of about 5 nanometers per minute. The TEOS flow continues for about 5 minutes, resulting in a total deposit of about 25 nanometers of $SiO_2$. After the termination of the TEOS flow about 10 minutes into the ramp-up, the temperature continues to increase to about 775 degrees C.

At about 12 minutes into the cycle, the $NH_3$ is introduced into the furnace at a flow rate of about 300 cubic centimeters per minute, and the $SiH_2Cl_2$ is introduced at a flow rate of about 30 cubic centimeters per minute. This results in a deposition of the silicon nitride cap layer at a rate of about 2.9 nanometers per minute. The pressure during this deposition is about 38.66 Pa (290 millitorr). This deposition continues for about 17 minutes, resulting in a silicon nitride cap about 50 nanometers thick. The flow of the source gasses is then stopped, and the furnace pumped down to the base pressure to clean the furnace tube. The flow controllers for the source gasses are purged by a flow of $N_2$, while the temperature is ramped down to the idling value. The furnace is filled with $N_2$ gas at atmospheric pressure, and the wafer boats removed from the furnace.

Following the present capping technique, the front side of the wafers are polished to provide a highly specular, damage-free surface. This is typically accomplished by polishing the front side of the wafer using a caustic slurry as a polishing agent. They are then ready for the epitaxial growth process according to procedures known in the art. Although silicon, including dopants as desired, is typically grown as the epitaxial layer, other materials are possible. For example, the epitaxial growth of germanium and/or group III-V semiconductor materials on silicon wafers is being explored by workers in the art, and can benefit from the use of silicon wafers capped according to the present technique. A review of some current epitaxial techniques is given in "Low-Pressure Chemical Vapor Deposition", S. D. Hersee et al, Annual Review of Materials Science Vol. 12, pp. 65-80 (1982). The resulting wafers may then be used for integrated circuit production, or for the production of various other semiconductor devices.

## Claims

1. A method of capping the back side of a semiconductor wafer in preparation for forming an epitaxial layer of a semiconductor material on the front side of said wafer, comprising the steps of:

introducing said wafer into a furnace:

increasing the temperature in said furnace while introducing a source gas comprising a silicon compound and a source of oxygen into said furnace, thereby depositing silicon dioxide onto at least the back side of said wafer at a temperature below 775 degrees C during said temperature increase;

terminating said source gas flow and continuing to increase the temperature in said furnace; and

maintaining said furnace temperature and introducing a gaseous source of silicon and of nitrogen into said furnace, thereby depositing silicon nitride onto said silicon dioxide.

2. The method according to claim 1,



* C L M S *

CHARACTERISED IN THAT said source gas comprising a silicon compound and said source of oxygen is $Si(OC_2H_5)_4$.

3. The method according to claim 1, CHARACTERISED IN THAT said source comprising a silicon compound is dichlorosilane.

4. The method according to claim 1, CHARACTERISED IN THAT said source of nitrogen is ammonia.

5. The method according to claim 1, CHARACTERISED BY accomplishing said depositing of silicon dioxide during a time period of less than 10 minutes.

6. The method according to claim 1, CHARACTERISED IN THAT said wafer as introduced into said furnace has a concentration of unprecipitated oxygen of at least 10 parts per million.

**Patentansprüche**

1. Verfahren zum Überkappen der Rückseite von Halbleiterwafern zur Vorbereitung der Bildung einer epitaxialen Schicht eines Halbleitermaterials auf der Vorderseite des Wafers mit den Verfahrensschritten:

Einbringen des Wafers in einen Ofen,

Erhöhen der Temperatur im Ofen, während ein Quellengas mit einer Siliciumverbindung und einer Sauerstoffquelle in den Ofen eingebracht werden, wodurch Siliciumdioxid auf wenigstens der Rückseite des Wafers bei einer Temperatur von unterhalb 775°C während des Temperaturanstiegs aufgebracht wird,

Beenden des Quellengasflusses und Fortsetzen der Temperaturerhöhung im Ofen und

Halten der Ofentemperatur und Einführen einer gasförmigen Quelle von Silicium und Stickstoff in den Ofen, wodurch Siliciumnitrid auf das Siliciumdioxid abgeschieden wird.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß das Quellengas eine Siliciumverbindung umfaßt und daß die Sauerstoffquelle $Si(OC_2H_5)_4$ ist.

3. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Quelle mit einer Siliciumverbindung Dichlorsilan ist.

4. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Stickstoffquelle Ammoniak ist.

5. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Abscheidung von Siliciumdioxid während einer Zeitspanne von weniger als 10 Minuten erfolgt.

6. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß der in den Ofen eingebrachte Wafer eine Konzentration von nicht ausgefälltem Sauerstoff von wenigstens 10 ppm hat.

**Revendications**

1. Un procédé d'encapsulation de la face arrière d'une tranche de semiconducteur en préparation pour la formation d'une couche épitaxiale d'un matériau semiconducteur sur la face avant de cette tranche, comprenant les étapes suivantes :

on introduit la tranche dans un four;

on augmente la température dans le four tout en introduisant dans le four un gaz de source comprenant un composé de silicium, et une source d'oxygène, pour déposer ainsi du dioxyde de silicium au moins sur la face arrière de la tranche, à une température inférieure à 775°C, pendant l'augmentation de température;

on arrête l'écoulement du gaz de source et on continue à augmenter la température dans le four; et

on maintient la température de four et on introduit une source gazeuse de silicium et d'azote dans le four, pour déposer ainsi du nitrure de silicium sur le dioxyde de silicium.

2. Le procédé de la revendication 1, CARACTERISE EN CE QUE le gaz de source comprend un composé de silicium et la source d'oxygène consiste en $Si(OC_2H_5)_4$.

3. Le procédé selon la revendication 1, CARACTERISE EN CE QUE la source comprenant un composé de silicium consiste en dichlorosilane.

4. Le procédé selon la revendication 1, CARACTERISE EN CE QUE la source d'azote consiste en ammoniac.

5. Le procédé selon la revendication 1, CARACTERISE EN CE QUE le dépôt de dixoyde de silicium est effectué pendant une durée inférieure à 10 minutes.

6. Le procédé selon la revendication 1, CARACTERISE EN CE QUE la tranche qui est introduite dans le four a une concentration d'oxygène non précipité d'au moins 10 parties par million.



* C L M S *