

## MEMRISTOR ARRAY AND METHOD OF MANUFACTURING THEREOF

## FIELD

[0001] The invention concerns memristor arrays, memristor structures, and methods  
5 of manufacturing memristor arrays and memristor structures.

## BACKGROUND

[0002] Memristors are electronic components with current-conducting properties  
dependent on previous electric conditions they have been subjected to. Properties of  
10 memristors include properties such as adjustable resistance and low energy consumption  
between states of different resistivity that make them useful for different applications.

[0003] A memristor or a memristive material may have the ability to exhibit a so-  
called high resistivity state HRS and a so-called low resistivity state LRS. A memristor may  
display bipolar switching between the HRS and the LRS states, in other words, a voltage at  
15 which a change from HRS to LRS occurs is different from a voltage at which a change from  
LRS to HRS occurs. However, it may be beneficial to have these changes from HRS to LRS,  
and LRS to HRS at, or near, a same voltage or a narrow voltage range. Conversely, in other  
applications, asymmetric changes from LRS to HRS may be beneficial. Furthermore, by  
obtaining a smaller voltage range for resistivity switching RS, lower energy consumption  
20 may be obtained.

## SUMMARY OF THE INVENTION

[0004] In the present disclosure there is provided a memristor array and a method of  
manufacturing thereof. The memristor array comprises a plurality of memristor devices,  
wherein at least one memristor device is connected to one other memristor device via a first  
25 pattern. The first pattern comprises a memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ ,  
wherein  $x$  has a value more than 0.6 and less than 0.99. Such a memristive material is  
sometimes abbreviated as GCMO. The memristor devices further comprise a second pattern  
comprising an oxidizable metal. The first pattern connecting and/or shared by two memristor

devices provides a simplified memristor device, and thus, a memristor array with scalable size and geometries.

[0005] The invention is defined by the features of the independent claims. Some specific embodiments are defined in the dependent claims.

5 [0006] According to a first aspect of the present invention, there is provided a memristor array, comprising at least two memristor devices, the memristor devices comprising

- a first pattern comprising memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein x has a value more than 0.6 and less than 0.99; and
- 10 – a second pattern comprising oxidizable metal, wherein the second pattern is in contact with the first pattern over an interface comprising at least one oxide of the oxidizable metal,

wherein at least one memristor device of the memristor array is connected to at least one other memristor device of the memristor array via the first pattern.

15 [0007] The manufacturing of memristor devices in a memristor array comprises providing a first pattern, for example, by depositing and patterning said first pattern using chemical vapor deposition or pulsed laser deposition. A second pattern comprising an oxidizable metal is provided using, for example, lift-off process, and said second pattern is in contact with the first pattern through an interface. The second pattern may be deposited  
20 on an electrically insulating layer deposited at least in part on the first pattern. Said electrically insulating layer may comprise a hole extending to the first pattern thus, the hole may delimit area of the interface between the first pattern and the second pattern. The plurality of memristor devices manufactured in such a way are connected to at least one other memristor device via a first pattern. For example, two memristor devices may share a first  
25 pattern, or the first patterns of said memristor devices are connected to one another forming a memristor array.

[0008] According to a second aspect of the present invention, there is provided a method for manufacturing at least two memristor devices comprised in a memristor array, the method comprising:

- providing a first pattern, the first pattern comprising memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein  $x$  has a value more than 0.6 and less than 0.99; and
- providing a second pattern comprising oxidizable metal such that the second pattern is in contact with the first pattern over an interface comprising at least one oxide of the oxidizable metal,

wherein at least one memristor device of the memristor array is connected to at least one other memristor device of the memristor array via the first pattern.

## BRIEF DESCRIPTION OF THE DRAWINGS

- [0009] FIG. 1A-1C illustrate examples of memristor devices in accordance with at least some embodiments of the present invention;
- [0010] FIG. 2A illustrates an example memristor array capable of supporting at least some embodiments of the present invention;
- 15 [0011] FIG. 2B illustrates a cross-sectional projection of the example memristor array of illustrated in FIG. 2A along a line between points A and A';
- [0012] FIG. 3A illustrates an example memristor array capable of supporting at least some embodiments of the present invention;
- [0013] FIG. 3B illustrates a cross-sectional projection of the example memristor array of illustrated in FIG. 3A along a line between points A and A';
- 20 [0014] FIG. 4 illustrates an example apparatus capable of supporting at least some embodiments of the present invention;
- [0015] FIG. 5A-5D illustrate an example manufacturing method for a memristor array according to at least some embodiments of the present invention;
- 25 [0016] FIG. 6A-6E illustrate an example manufacturing method for an apparatus comprising a plurality of memristor devices according to at least some embodiments of the present invention; and

[0017] FIG. 7A-7F illustrate an example manufacturing method for a memristor array comprising a plurality of memristor devices according to at least some embodiments of the present invention.

[0018] FIG. 8A illustrates a three-dimensional perspective view of an example memristor array capable of supporting at least some embodiments of the present inventions.

[0019] FIG. 8B illustrates a sideview of the example memristor array of FIG. 8A.

[0020] FIG. 9 illustrates an example memristor array capable of supporting at least some embodiments of the present invention; and

[0021] FIG. 10 illustrates an example memristor array capable of supporting at least some embodiments of the present invention.

#### EMBODIMENTS

[0022] Hereon is disclosed a memristor array comprising a plurality of memristor devices. The memristor array, and memristor devices therein, comprise a memristive material, the memristive material comprising gadolinium Gd, calcium Ca, manganese Mn and oxygen O with a formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x has a value more than 0.6 and less than 0.99. Furthermore, a method for manufacturing said memristor array is disclosed. The memristive materials with said formula may be abbreviated as GCMO.

[0023] The expression "memristive material" is used here for the purpose of unambiguously referring to the material that is comprised in a first pattern, although it is the current understanding that the memristor-type effects actually arise in the junction or interface between the memristor material and a contact, not in the bulk of the memristive material itself. Electrically conductive connections may be used to subject the piece of memristive material to desired voltages and to, for example, measure the resulting electric characteristics of the piece of memristive material.

[0024] In the present disclosure, a memristor device has a pattern comprising of GCMO in contact with another pattern comprising an oxidizable metal. An advantage of using the memristive material as a pattern, and not merely as a memristive layer separating two electrodes, provides simplified and scalable manufacturing possibilities and thus, use cases in manufactured memristor devices.

[0025] The memristive material with a formula  $Gd_{1-x}Ca_xMnO_3$  may be produced as a film or a layer using, for example, chemical solution deposition CSD, metalorganic chemical vapor deposition MOCVD, metalorganic deposition MOD or pulsed laser deposition, PLD. WO 2021/152215 A1 discloses the production of memristive materials having the formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x is a value greater than 0 and smaller than 1, from starting materials which are formed by pulsed laser deposition PLD of specific solid state materials, viz. gadolinium(III) oxide, calcium carbonate and manganese(IV) oxide. Further, WO 2024/003454 A1 discloses methods for producing, for example, GCMO films.

[0026] According to the present disclosure there is provided a memristor array, comprising at least two memristor devices, the memristor devices comprising

- a first pattern comprising memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x has a value more than 0.6 and less than 0.99; and
- a second pattern comprising oxidizable metal, wherein the second pattern is in contact with the first pattern over an interface comprising at least one oxide of the oxidizable metal,

wherein at least one memristor device of the memristor array is connected to at least one other memristor device of the memristor array via the first pattern.

[0027] The term “connected” in the context of connecting at least two memristor devices via the first pattern is to be understood the electrically joining together said memristor devices such that the at least two second patterns comprised therein, are electrically connected to one another using the properties of the GCMO memristive material.

[0028] In an embodiment, the at least one memristor device is connected to the at least one other memristor device via the first pattern such that memristive material with formula  $Gd_{1-x}Ca_xMnO_3$  of the first pattern extends from the second pattern of the at least one memristor device to the second pattern of the at least one other memristor device. In other words, in some such embodiments, the GCMO is arranged to connect at least two second patterns of the memristor array as a continuous item, such as a continuous strip of GCMO.

[0029] In an embodiment, the first pattern consists essentially of memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x has a value more than 0.6 and less than 0.99. In other words, in such an embodiment wherein the first pattern “consists essentially” of GCMO memristive material, components additional to that of GCMO can be present, but

those additional components do not materially affect the characteristics of the connection between the at least two memristor devices of the memristor array, and the connection of the respective second patterns therein.

[0030] In an embodiment, the first pattern consists of memristive material with  
5 formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein x has a value more than 0.6 and less than 0.99.

[0031] In an embodiment, the first pattern is obtained from a deposited and patterned layer of memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ .

[0032] In an embodiment, the composition of the first pattern contains at least 75% (volume percentage) of GCMO. In an embodiment, the composition of the first pattern  
10 contains at least 85% of GCMO. In an embodiment, the composition of the first pattern contains at least 99% of GCMO. In at least some embodiments, the first pattern is substantially uniform in terms of distribution of constituents. In other words, in at least some such embodiments, the first pattern has a homogenous composition.

[0033] In an embodiment, the memristor devices of the memristor array have at least  
15 the first pattern or the second pattern in common with at least one other memristor device of the memristor array.

[0034] In an embodiment, a contact area of an interface between a first pattern and a second pattern over the interface is between  $2 \text{ nm}^2$  and  $2500 \text{ }\mu\text{m}^2$ , such as between  $2 \text{ nm}^2$  and  $2000 \text{ }\mu\text{m}^2$ , such as between  $3 \text{ nm}^2$  and  $1500 \text{ }\mu\text{m}^2$ , such as between  $5 \text{ nm}^2$  and  $1000 \text{ }\mu\text{m}^2$ .  
20 In an embodiment, the contact area of the interface is between  $10 \text{ nm}^2$  and  $10 \text{ }\mu\text{m}^2$ .

[0035] In an embodiment, a contact area of an interface between a first pattern and a second pattern over the interface is between  $2 \text{ nm}^2$  and  $2500 \text{ }\mu\text{m}^2$ , or between  $5 \text{ nm}^2$  and  $500 \text{ }\mu\text{m}^2$ , or between  $10 \text{ nm}^2$  and  $10 \text{ }\mu\text{m}^2$ , or between  $20 \text{ nm}^2$  and  $50 \text{ nm}^2$ , or between  $30 \text{ nm}^2$  and  $100 \text{ nm}^2$ , or between  $50 \text{ nm}^2$  and  $500 \text{ nm}^2$ .

[0036] In an embodiment, x has a value between 0.65 and 0.975, or between 0.7 and 0.95, or between 0.75 and 0.9, or between 0.7676 and 0.89, or between 0.77 and 0.88, or between 0.78 and 0.87, or between 0.79 and 0.86. In a preferred embodiment, the x has a value between 0.8 and 0.85. The preferred embodiment, with x having a value between 0.8 and 0.85 is beneficial as it provides optimal resistive switching RS properties for the  
25  
30 memristor.

[0037] In an embodiment, for at least one memristor device 100, the first pattern 110 comprises a first portion 111 and a second portion 112; and the second pattern 120 comprises a third portion 121 and a fourth portion 122; wherein the first portion 111 is in contact with the third portion 121 over the interface 150 and the second portion 112 is separated from the fourth portion 122 by an electrically insulating layer 130. In a further embodiment, the third portion 122 comprises a protrusion through a hole in the electrically insulating layer 130, and the protrusion is in contact with the first portion 111 of the first pattern 110.

[0038] In an embodiment, the electrically insulating layer comprises at least one of aluminium oxide, silicon dioxide, titanium oxide and strontium titanate. Thickness of an electrically insulating layer is such that it acts as an electrical insulator, in other words, the electrically insulating layer substantially reduces or prevents the electrical connection of a first pattern and a second pattern in portions wherein said first pattern and said second pattern are separated by said electrically insulating layer. Further, it may be beneficial to exclude and/or omit materials exhibiting memristive properties, such as hafnium oxide ( $\text{HfO}_2$ ), to be comprised in the electrically insulating layer.

[0039] In an embodiment, the electrically insulating layer comprises an electrically insulating polymer, co-polymer or polymer composite. In some embodiments, the electrically insulating layer may comprise, for example, at least one of polyimide, polyethylene, polypropylene, polymethyl methacrylate (PMMA), polyolefin, epoxy novolac, siloxane polymer and polycarbonate.

[0040] In an embodiment, the second pattern comprises at least one of copper, molybdenum, indium, aluminium and titanium. A benefit of a second pattern comprising, for example, aluminium are its oxidizable properties and potential crystalline defects that protect the interface between the first pattern and the second pattern from external electromagnetic radiation. In some embodiments, the second pattern may comprise different materials in different portions of said second pattern, in other words, the third portion may comprise different materials than the fourth portion.

[0041] In an embodiment, thickness of the second pattern is more than 1 nm, or more than 1.8 nm, or more than 2 nm, or more than 5 nm, or more than 10 nm, or more than 20 nm, or more than 50 nm, or more than 100 nm, or more than 300 nm, or more than 500 nm. Thickness is defined substantially perpendicular to the interface 150 through which the first

pattern and second pattern are in contact. Thickness is measured along the normal of the area of said interface.

[0042] In an embodiment, thickness of the first pattern thickness of more than 20 nm, or more than 30 nm, or more than 50 nm, or more than 100 nm, or more than 300 nm, or  
5 more than 500 nm. Thickness is defined substantially perpendicular to the interface through which the first pattern and second pattern are in contact. Thickness is measured along the normal of the area of said interface.

[0043] In some embodiments, the first pattern is attached to at least one contact terminal, using which the resistive properties of the first pattern may be changed. This is  
10 beneficial to obtain a desired resistance for the memristive material, and thus, provide an increased or decreased electrical conductivity for the first pattern. In an embodiment, such at least one contact terminal attached to the first pattern, comprises a material such that an ohmic contact between the first pattern and the contact terminal is obtained. In an embodiment, the at least one contact terminal comprises at least one of gold and silver.

[0044] In an embodiment, the material of the third portion comprises the oxidizable metal of the second pattern and the fourth portion comprises material different from the material of the third portion. As such, said second pattern may comprise two portions comprising a third portion and a fourth portion. In some embodiments, the third portion comprises at least one of copper, molybdenum, indium, aluminium and titanium, and the  
20 fourth portion comprises at least one of copper, molybdenum, indium, aluminium and titanium. Furthermore, the third portion and fourth portion may comprise different materials, for example, the third portion may comprise aluminium, and the fourth portion of said second pattern, may comprise. Alternatively or additionally, the second pattern may comprise at least one contact terminal such that said at least one contact terminal comprise  
25 same material as the second pattern.

[0045] An advantage of the provided memristor array according to at least some embodiments is that because the GCMO memristive material is comprised in a first pattern, device-to-device variation in the manufactured devices and arrays is reduced and/or minimized, and such structures are more stable even in alternating environments. Such  
30 memristor arrays may have less manufacturing and other errors. Additionally, computing tasks may be localized in said memristor arrays and memristor devices. Furthermore, the memristor array disclosed herein may, because of modular structure or expandable

geometric structure, be expanded and/or extended by joining additional memristor arrays, memristor devices, and/or other electronics. Such expansion may also be done after said memristor array has been initially manufactured. Because of its properties, a memristor array according to at least some embodiments may endure high temperatures, low temperatures, radiation and/or high vacuum environments. At least in some embodiments comprise an electrically insulating layer. In such embodiments, the at least one hole in the electrically insulating layer delimits the contact area for the interface between the first pattern and the second pattern and thus, the present disclosure provides beneficial embodiments wherein resistivity switching RS may be more precisely controlled for memristor devices and memristor arrays.

[0046] Moreover, in at least some embodiments, a first pattern of a memristor device in a memristor array consists essentially of GCMO memristive material or consists of GCMO memristive material. An advantage of the provided memristor array is that because such a first pattern consists essentially of GCMO or consists of GCMO memristive material, device-to-device variation in the manufactured devices and arrays is reduced and/or minimized, and such structures are more stable even in alternating environments. Such memristor arrays may have less manufacturing and other errors.

[0047] A memristor array, such as those described above, comprises at least two memristor devices connected via a common first pattern. FIG. 1A – 1C illustrate examples of memristor devices in accordance with at least some embodiments of the present invention.

[0048] In FIG. 1A, there is provided a memristor device 100, comprising a first pattern 110 and a second pattern 120 in contact at an interface 150. The first pattern comprises GCMO, consists essentially of GCMO or consists of GCMO, and the second pattern comprises oxidizable metal, for example, aluminium and/or titanium. In some embodiments, the second pattern comprises at least one of copper, indium, molybdenum and tungsten. Additionally, the first pattern 110 and the second pattern 120 may have contact terminals 115, 125 such that the first pattern 110 and the second pattern 120 may be connected to additional and/or external electronics, such as a device capable of producing a voltage, such as a voltage source. Additionally or alternatively, the additional and/or external electronics may comprise an operational amplifier or a transistor or a memory cell. There may be a plurality of contact terminals 115 in a first pattern 110 and plurality of contact terminals 125 in a second pattern 120. In an embodiment, the contact terminals for the first pattern 115 are

at least one of gold and silver. In an embodiment, for the second pattern, the contact terminals 125 are at least one of aluminium and titanium. In some embodiments, the contact terminal or a plurality of contact terminals of a second pattern comprise at least one of copper, indium, molybdenum and tungsten.

5 [0049] In at least some embodiments, area of the interface 150 in a memristor device, formed by connecting a first pattern 110 to a second pattern 120, is such that preferred properties of the memristive material comprising GCMO, consisting essentially of GCMO or consisting of GCMO are obtained. Preferred properties may be, for example, resistive switching RS at a narrower voltage range, and/or at a smaller voltage. The area of the  
10 interface 150 is construed as a two-dimensional cross-sectional projection of an actual area of the interface. The actual area of the interface may thus, be larger than the interface area due to, for example, unevenness of the interface. Such unevenness may be caused by, for example, spikes protruding from the second pattern 120 material into the first pattern 110 material caused by heating, such as, aluminium spiking that may occur with aluminium.

15 [0050] The term “crosspoint” may be used to describe a memristor device, especially the interface formed through contact between a first pattern and a second pattern comprised in said memristor device. However, it is noted that such contact is not merely limited to perpendicular orientation of said first pattern and second pattern according to embodiments of the present disclosure. Further, the term “crossbar” may be construed as a first pattern  
20 connecting to at least two second patterns forming a memristor array. However, it is noted that such connections described in the present disclosure are not merely limited to perpendicular and parallel orientations of said first pattern and second patterns, and other suitable orientations for first pattern and second patterns are available depending on the application. Furthermore, neither “crosspoint” nor “crossbar” should be construed as  
25 limiting the shape of a first pattern and/or second pattern, as the shape of said patterns depend on the application and/or use-case of a memristor array and/or memristor devices comprised therein.

[0051] In FIG. 1B, an example memristor device 100 is presented, wherein a first pattern 110 comprises a first portion 111 and a second portion 112 and a second pattern 120  
30 comprises a third portion 121 and a fourth portion 122. The first pattern 110 and the second pattern 120 are connected such that the first portion 111 and the third portion 121 form an

interface 150 thus, forming a contact between the first pattern 110 and the second pattern 120.

[0052] As is illustrated in FIG. 1B, the second portion 112 and the fourth portion 122 are separated by an electrically insulating layer 130. The use of an electrically insulating layer 130 may be beneficial as the area of the interface 150 may be more precisely controlled. The electrically insulating layer 130 may comprise, for example, at least one of aluminium oxide, silicon oxide, titanium oxide and strontium titanate. The electrically insulating layer 130 has a thickness so as to substantially minimize leakage current between a first pattern and a second pattern through said electrically insulating layer 130. In an embodiment, the electrically insulating layer 130 has thickness of 5 nm – 50 nm, for example 10 – 25 nm. The thickness is measured from a region of the electrically insulating layer 130 wherein the first pattern 110 and second pattern 120 are on opposite sides of the electrically insulating layer 130, in other words, in FIG. 1B, between the second portion 112 and the fourth portion 122.

[0053] FIG. 1C illustrates an example memristor device according to at least some embodiments. Similarly to the memristor device of FIG. 1B, the memristor device of FIG. 1C comprises a first pattern 110, a second pattern 120, an electrically insulating layer 130 and a substrate 170. The first pattern 110 comprising GCMO, consisting essentially of GCMO or consisting of GCMO is attached to the substrate 170. As can be appreciated from FIG. 1C, the second pattern 120 of said memristor device comprises a third portion 121 and a fourth portion 122. The third portion 121 and the fourth portion 122 may comprise different materials, and said third portion and said fourth portion may be construed as separate elements attached together. This may be beneficial in, for example, manufacturing said memristor devices, as a hole delimited by an electrically insulating layer 130, may be first filled with a second pattern material, in other words the third portion, and afterwards a fourth portion may be attached to the third portion. The third portion may comprise different material than the fourth portion. Alternatively, the third portion may comprise the same material than the fourth portion.

[0054] In an embodiment, the first pattern comprising GCMO, consisting essentially of GCMO or consisting of GCMO, is connected to a contact terminal. Such a contact terminal may be, for example, a contact pin, a contact pad or a bond wire. The contact terminal may comprise gold or silver, for example. Alternatively or additionally, the second pattern may be connected to a contact terminal. Such a contact terminal may be, for example,

a contact pin, a contact pad or a bond wire. The contact terminal may comprise aluminium or titanium, for example. Such contact terminals may be used to connect the first pattern and/or the second pattern to external electronics. In FIG. 1A and FIG. 1B, one contact terminal 115 for the first pattern 110 and one contact terminal 125 for the second pattern 120 are illustrated.

[0055] Using at least some of the embodiments presented for the memristor device, more geometries, structures and/or constructions that utilize the memristor devices comprising a first pattern 110 and a second pattern 120 may be obtained. By using a plurality of first patterns and/or plurality of second patterns comprised in a plurality of memristor devices, a memristor array may be obtained wherein at least one memristor device has a first pattern in common with at least one other memristor device. For example, such a memristor array may comprise interlaced memristor devices forming a grid structure. It is to be understood that the shape or form of a first and/or second pattern may be different, depending on the memristor array and a memristor device comprised therein. For example, the first pattern and/or the second pattern may be substantially longitudinal sheets, or they may have different geometric patterns depending on, for example, wherein said first and/or second pattern need to be connected in a memristor array or to additional and/or external electronics. By using a different geometries for a first pattern, the at least two second patterns may be connected in various locations and orientations in a memristor array.

[0056] At least two memristor devices of a memristor array are connected via at least one common first pattern. This may be beneficial as the at least two memristor devices connected in such a way may have an electrically conductive connection or exhibit increased electrical resistivity, depending on the state of the memristive material, for example, low resistivity state LRS and high resistivity state HRS, respectively. Additionally or alternatively, more resistivity states for a memristor device, and a memristor array may be obtained. A memristor material comprising GCMO may have, for example, 3 differentiable resistivity states, or 5 differentiable resistivity states, or 10 differentiable resistivity states, or 20 differentiable resistivity states, or 50 differentiable resistivity states, or 100 differentiable resistivity states, or 500 differentiable resistivity states, or 1000 differentiable resistivity states. The resistivity may also be dynamically modulated to accommodate specific applications for memristor arrays and memristor devices disclosed herein, for example, artificial neurons or artificial synapses enabling analog functionality.

[0057] FIG. 2A and FIG. 2B illustrate an example apparatus 200 capable of supporting at least some embodiments. FIG. 2B is a cross-sectional projection through a line along points A and A' illustrated in FIG. 2A, in other words, FIG. 2B represents the same example apparatus to that illustrated in FIG. 2A. Two second patterns 120a, 120b are in contact with one first pattern 110 through interfaces 150. The second patterns 120a, 120b are connected to the first pattern 110, similarly to that of the memristor device 100 in FIG. 1B. Thus, the second pattern 120a is connect to another second pattern 120b via the first pattern 110, forming a memristor array 200. As can be seen from FIG. 2A and 2B, in the memristor array 200, the interface area 150 is delimited by an electrically insulating layer 130.

10 [0058] Similarly, a plurality of first patterns and a plurality of second patterns may also be connected through interfaces to form a memristor array comprising interconnected memristor devices. For example, in FIG. 3A there is provided a memristor array 300 in a form of a grid structure comprising a plurality of substantially parallel first patterns and a plurality of substantially parallel second patterns. Further, the plurality of substantially parallel first patterns and the plurality of substantially parallel second patterns are positioned substantially perpendicular to one another. The example memristor array depicted in FIG. 3A exhibits a layered structure, in other words the substantially parallel first patterns 310a, 310b & 310c are on a different layer to the substantially parallel second patterns 320a, 320b & 320c, and connected through interfaces 350 in between.

20 [0059] FIG. 3A and FIG. 3B illustrate the same example apparatus 300 capable of supporting at least some embodiments. FIG. 3B is a cross-sectional projection through a plane along points A and A' illustrated in FIG. 3A. The example apparatus 300 comprises altogether nine interfaces 350 between first patterns 310a, 310b & 310c and second patterns 320a, 320b & 320c forming a grid structure. Three of the nine interfaces 350 are visible in FIG. 3B, in other words, the three interfaces 350 are depicted in FIG. 3B along a line between points A and A' presented in FIG. 3A. The said three interfaces 350 are formed because first patterns 310a, 310b & 310c are in contact with a second pattern 320a.

30 [0060] A plurality of second patterns, comprised in a plurality of memristor devices, may be separated from one another, and have thus, no direct electrical contact with one another. However, such second patterns may be connected via a first pattern. The gap of said plurality of second patterns may be such that leakage current and/or quantum tunnelling is minimized, reduced or prevented. Thus, such a gap may be, for example, more than 2 nm,

or more than 3 nm, more than 5 nm, or more than 10 nm, or more than 20 nm, or more than 30 nm, or more than 50 nm, or more than 100 nm, or more than 200 nm, or more than 500 nm, or more than 1  $\mu\text{m}$ , or more than 5  $\mu\text{m}$ , or more than 10  $\mu\text{m}$ . Additionally or alternatively, in an embodiment, wherein a second pattern is in contact with another second pattern, such a plurality of second patterns may be construed as a single second pattern, forming part of a single memristor device. Such a memristor device may be comprised in a memristor array.

[0061] The first patterns may be separated from other first patterns comprised in a memristor array, and have thus, no direct electrical contact with one another, although such first patterns may be connected via a second pattern. The gap of said plurality of first patterns may be such that leakage current and/or quantum tunnelling is minimized, reduced or prevented. Thus, such a gap may be, for example, more than 2 nm, or more than 3 nm, more than 5 nm, or more than 10 nm, or more than 20 nm, or more than 30 nm, or more than 50 nm, or more than 100 nm, or more than 200 nm, or more than 500 nm, or more than 1  $\mu\text{m}$ , or more than 5  $\mu\text{m}$ , or more than 10  $\mu\text{m}$ . Additionally or alternatively, in an embodiment, wherein a first pattern is in contact with another first pattern, such a plurality of first patterns may be construed as a single first pattern, forming part of a single memristor device. Such a memristor device may be comprised in a memristor array.

[0062] An example of such a gap, is provided in FIG. 3A, comprising a memristor array 300 with a plurality of first patterns 310a, 310b & 310c and a plurality of second patterns 320a, 320b & 320c. The first patterns are separated from one another by a gap. The second patterns are separated from one another by a gap.

[0063] In FIG. 3A, the first patterns 310a, 310b & 310c are connected to the second patterns 320a through an interface 350, as illustrated also in FIG. 3B. As can be appreciated from FIG. 3A and FIG. 3B, the contact areas of the interfaces between the first patterns 310a, 310b & 310c and second patterns 320a, 320b & 320c may vary in size. The area of the interface is beneficial to obtain a suitable resistive switching, RS, voltage. Resistive switching voltage refers to a voltage at which the resistance of a memristive material changes from a higher/lower resistance to a lower/higher resistance.

[0064] The area of an interface 350 may be controlled using, for example, a hole in an electrically insulating layer 330, the electrically insulating layer 330 separating, in part, the first pattern 310 and the second pattern 320. The benefit of controlling the area of the interface 350 is that memristive properties of a memristor device are dependent on the area

of said interface 350, and by extension a contact of a first pattern and a second pattern. It is noted, that the shape of the interface, as presented in, for example, FIG. 3A, is circular. However, in some embodiments, shape of an interface 350 may be different, such as a square or a rectangle or it may be elliptical or polygonal. In some embodiments, the shape of an interface may be irregular or other than a simple geometric shape.

[0065] Although an insulating layer is absent in FIG. 3A and FIG. 3B, in some embodiments an insulating layer is present for such a structure as well. In an embodiment, the first pattern comprises a first portion and a second portion, and the second pattern comprises a third portion and a fourth portion, wherein the first portion is in contact with the third portion over the interface 350 and the second portion is separated from the fourth portion by an electrically insulating layer. Such an embodiment is beneficial as area of the interface, or so-called via size, may be controlled in a way that other dimensions of a first pattern and a second pattern in contact through said via, do not affect the interface size.

[0066] FIG. 3A and 3B illustrate a memristor array 300 comprising a grid structure. The term “grid” is to be understood as perpendicular and parallel overlapping structures, forming a mesh or a grating. However, it is noted that in some embodiments other orientations between a first pattern and a second pattern exist. Furthermore, in some embodiments, other orientations exist between a plurality of first patterns as well as between a plurality of second patterns.

[0067] FIG. 4 illustrates an example apparatus 400 located on a substrate 370 comprising multiple memristor arrays 300, similar to those shown in FIG. 3A and FIG. 3B. As can be appreciated from FIG. 4, a plurality of memristor arrays comprising grid structures may be on a same substrate 370. Further, plurality of interfaces 350 between first patterns and second patterns have varying sizes of said plurality of interfaces. For clarity in FIG. 4, the electrically insulating layer 330 separating in part the first patterns 310 and the second patterns 320, is illustrated by a solid outline of the electrically insulating layer.

[0068] According to the present disclosure, there is provided a method for manufacturing at least two memristor devices comprised in a memristor array, the method comprising:

providing a first pattern, the first pattern comprising  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein  $x$  has a value more than 0.6 and less than 0.99; and

providing a second pattern comprising oxidizable metal such that the second pattern is in contact with the first pattern over an interface comprising at least one oxide of the oxidizable metal,

wherein at least one memristor device of the memristor array is connected to at least one other memristor device of the memristor array via the first pattern.

[0069] In an embodiment, the memristor devices of the memristor array have at least the first pattern or the second pattern in common with at least one other memristor device of the memristor array.

[0070] In an embodiment, providing the first pattern 310 further comprises depositing a layer of memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ ; and patterning the layer of memristive material with formula  $Gd_{1-x}Ca_xMnO_3$  to obtain the first pattern 310. Such depositing may be done using, for example, chemical solution deposition, CSD metalorganic chemical vapor deposition MOCVD, metalorganic deposition MOD, pulsed laser deposition PLD or sputtering. Alternatively, depositing may be done using spin-coating, or by plasma jet printing or by ultraviolet lithography, or by flash imprint lithography or by nanoimprint lithography NIL, or by jet imprint lithography. Additionally or alternatively, depositing may be done using roll-to-roll processing. Patterning of the layer of memristive material with formula  $Gd_{1-x}Ca_xMnO_3$  may be done, for example, by etching, such as wet chemical etching, or dry etching such as reactive ion etching, ion beam etching and/or argon gas etching.

[0071] In an embodiment, x has a value between 0.65 and 0.975, or between 0.7 and 0.95, or between 0.75 and 0.9, or between 0.76 and 0.89, or between 0.77 and 0.88, or between 0.78 and 0.87, or between 0.79 and 0.86. In a preferred embodiment, the x has a value between 0.8 and 0.85. The preferred embodiment, with x having a value between 0.8 and 0.85 is beneficial as it provides optimal resistive switching RS properties for the memristor device and/or memristor array.

[0072] In an embodiment, providing the second pattern 320 comprises depositing an electrically insulating layer 330 at least in part on the first pattern; forming a hole 340 through the electrically insulating layer 330 to the first pattern 310, the hole 340 defining a location for the contact; and depositing oxidizable metal at least in the hole 340 in order to obtain the second pattern 320 such that the second pattern is in contact with the first pattern over the interface 350. In a further embodiment, forming the hole 340 is done by etching

the electrically insulating layer 330 using, for example, ion beam etching or reactive ion etching or argon gas etching. Alternatively, in another embodiment, forming the hole 340 is done by covering a region of a first pattern 310 using a mask prior to depositing the electrically insulating layer 330 on the first pattern 310. Such covering may be accomplished  
5 by using a laser writer or extreme ultraviolet lithography EUVL using a photoresist, electron beam lithography using a resist or ion beam lithography. After depositing the electrically insulating layer 330, the mask is removed thus, forming a hole 340 delimited by the electrically insulating layer 330, and said hole 340 extending to a first pattern 310.

[0073] In an embodiment, after the hole 340 has been formed, the second pattern is provided such that the first pattern and the second pattern are in contact over an interface  
10 350 in said hole 340. The second pattern may be provided, for example, using chemical vapor deposition CVD, molecular beam epitaxy MBE or physical vapor deposition PVD such as sputtering deposition, electron beam deposition, or thermal evaporation deposition.

[0074] In an embodiment, the electrically insulating layer comprises at least one of  
15 aluminium oxide, silicon nitride, silicon dioxide, titanium oxide, and strontium titanate. In an embodiment, the thickness of the electrically insulating layer is such that the electrically insulating layer is an electrical insulator, in other words, electrically separating a first pattern and a second pattern.

[0075] In an embodiment, the depositing of the oxidizable metal further comprises  
20 depositing an oxidizable metal in the hole; and depositing an electrically conductive metal such that the electrically conductive metal is in contact with the oxidizable metal in order to obtain the second pattern comprising the oxidizable metal and the electrically conductive metal. In an embodiment, the oxidizable metal may be at least one of copper, molybdenum, indium, aluminium and titanium. In an embodiment, the electrically conductive metal may  
25 be at least one of copper, molybdenum, indium, aluminium and titanium.

[0076] In an embodiment, the contact between the first pattern and the second pattern over the interface has an area between  $2 \text{ nm}^2$  and  $2500 \text{ }\mu\text{m}^2$ , such as between  $2 \text{ nm}^2$  and  $2000 \text{ }\mu\text{m}^2$ , such as between  $3 \text{ nm}^2$  and  $1500 \text{ }\mu\text{m}^2$ , such as between  $5 \text{ nm}^2$  and  $1000 \text{ }\mu\text{m}^2$ , such as between  $10 \text{ nm}^2$  and  $500 \text{ }\mu\text{m}^2$ , or between  $1 \text{ }\mu\text{m}^2$  and  $50 \text{ }\mu\text{m}^2$ . In an embodiment, the contact  
30 area of the interface is between  $10 \text{ nm}^2$  and  $10 \text{ }\mu\text{m}^2$ .

[0077] In an embodiment, a contact area of an interface between a first pattern and a second pattern over the interface is between  $2 \text{ nm}^2$  and  $2500 \text{ }\mu\text{m}^2$ , or between  $5 \text{ nm}^2$  and  $500 \text{ }\mu\text{m}^2$ , or between  $10 \text{ nm}^2$  and  $10 \text{ }\mu\text{m}^2$ , or between  $20 \text{ nm}^2$  and  $50 \text{ nm}^2$ , or between  $30 \text{ nm}^2$  and  $100 \text{ nm}^2$ , or between  $50 \text{ nm}^2$  and  $500 \text{ nm}^2$ .

5 [0078] In an embodiment, the method further comprises heat-treatment of the interface at a temperature between  $20 \text{ }^\circ\text{C}$  and  $400 \text{ }^\circ\text{C}$ , or between  $50 \text{ }^\circ\text{C}$  and  $300 \text{ }^\circ\text{C}$ , or between or between  $100 \text{ }^\circ\text{C}$  and  $200 \text{ }^\circ\text{C}$ . In an embodiment, duration of heat-treatment is between 1 minute and 20 minutes and in another embodiment, between 1 minute and 10 minutes. In an embodiment, the temperature is the temperature at a vacuum, in another  
10 embodiment the temperature is at a pressure of at most  $10^{-9}$  mbar, millibars. In some embodiments, the temperature is at a pressure of at most  $10^{-3}$  mbar, or at most  $10^{-4}$  mbar, or at most  $10^{-6}$  mbar, or at most  $10^{-9}$  mbar. After heat-treatment, the interface may then be allowed to passively cool. Heat-treatment may be beneficial for enhancing electrical contact of the first pattern 310 to the second pattern 320 at the interface 350.

15 [0079] In an embodiment, the second pattern 320 comprises at least one of copper, molybdenum, tungsten, indium, aluminium and titanium. In a further embodiment, the second pattern may comprise at least one contact terminal for additional electronics. In some embodiments, the at least one contact terminal for a second pattern comprises at least one of copper, molybdenum, tungsten, indium, aluminium and titanium. Contact terminals for a  
20 second pattern may be provided for example, by depositing, such as chemical vapor deposition CVD, physical vapor deposition PVD, sputtering, electron beam deposition, thermal evaporation, or molecular beam epitaxy MBE. Further, contact terminals for a second pattern may be patterned using wet chemical etching or dry etching such as reactive ion etching, ion beam etching and argon gas etching. Alternatively, the contact terminals of  
25 a second pattern may be provided concurrently with the provision of at least part of the second pattern.

[0080] In an embodiment, the first pattern may comprise at least one contact terminal for additional and/or external electronics. Such contact terminals may comprise gold and/or silver. Contact terminal for a first pattern may be a contact pad, which may be deposited  
30 using, for example, chemical vapor deposition CVD, physical vapor deposition PVD, sputtering, pulsed laser deposition PLD, electron beam deposition, thermal evaporation or molecular beam epitaxy, and patterned using for example, wet chemical etching or dry

etching, such as reactive ion etching, ion beam etching or argon gas etching. Alternatively, the contact terminals may be bond wire or contact pins, which may be attached to the first pattern.

[0081] FIG. 5A – 5D illustrate phases of an example of a method for manufacturing a memristor array according to at least some embodiments.

[0082] First, as illustrated in FIG. 5A, a first pattern 310 is provided on to a substrate 370, for example, by depositing a layer of GCMO onto the substrate 370 using deposition, such as chemical solution deposition CSD, metalorganic chemical vapor deposition MOCVD, metalorganic deposition MOD or pulsed laser deposition PLD, after which the said layer of GCMO is patterned in order to form a first pattern. Patterning may be done using, for example, wet chemical etching or dry etching, such as reactive ion etching, ion beam etching or argon gas etching. The substrate 370 may be strontium titanate  $\text{SrTiO}_3$  or silicon Si covered with strontium titanate  $\text{SrTiO}_3$ . In some embodiments, the substrate comprises at least one of lanthanum aluminium oxide ( $\text{LaAlO}_3$ ), strontium lanthanum aluminium oxide ( $\text{SrLaAlO}_4$ , SLAO), lanthanum aluminate - strontium aluminium tantalate (LSAT), magnesium oxide (MgO), neodymium gallium oxide ( $\text{NdGaO}_3$ , NGO) or silicon (Si), for example. The substrate may be beneficial for providing a first pattern comprising GCMO, as the unit cell of said substrate may be aligned with the unit cell of the GCMO, thus facilitating a possibility for epitaxial growth of a GCMO film.

[0083] Then, as illustrated in FIG. 5B, the first pattern 310 is at least in part covered with an electrically insulating layer 330. The electrically insulating layer 330 may be, for example, aluminium oxide ( $\text{Al}_2\text{O}_3$ ), silicon nitride (SiN), silicon dioxide ( $\text{SiO}_2$ ), magnesium oxide (MgO) or strontium titanate ( $\text{SrTiO}_3$ ). Such electrically insulating layer 330 used to cover at least in part the first pattern 310, may be obtained using, for example, atomic layer deposition, ALD, chemical vapour deposition CVD, physical vapour deposition PVD, sputtering, electron beam deposition and/or thermal evaporation. Alternatively, the electrically insulating layer may comprise, for example, an electrically insulating polymer such as polyimide, polyethylene, polypropylene and/or polycarbonate. Such electrically insulating layer 330 used to cover at least in part the first pattern 310, may be obtained using, for example, spin-coating, dip coating, and/or chemical solution deposition CSD, and/or inkjet printing, 3D printing and/or nanoimprint methods.

[0084] Then, as illustrated in FIG. 5C, at least one hole 340 is formed on the electrically insulating layer 330 such that said hole 340 extends to the first pattern 310. Such a hole 340 may be formed by, for example, wet chemical etching or dry etching such as reactive ion etching, ion beam etching and/or argon gas etching.

5 [0085] As shown in FIG. 5D, after at least one hole 340 has been formed, a second pattern 320 is provided such that the first pattern 310 and the second pattern 320 are in contact through said hole 340, forming an interface 350. The second pattern 320 may be provided using, for example a lift-off process, using for example, physical vapour deposition, PVD such as sputtering deposition, electron beam deposition or thermal  
10 evaporation deposition.

[0086] FIG. 6A – 6E illustrate phases of an example manufacturing method for an apparatus comprising a plurality of memristor arrays according to at least some embodiments of the present invention.

[0087] First in FIG. 6A, a substrate 370 is obtained whereon a plurality of first patterns  
15 310 is provided. The substrate 370 may comprise strontium titanate ( $\text{SrTiO}_3$ ), silicon (Si) coated with strontium titanate, lanthanum aluminium oxide ( $\text{LaAlO}_3$ ), strontium lanthanum aluminium oxide ( $\text{SrLaAlO}_4$ , SLAO), lanthanum aluminate – strontium aluminium tantalate (LSAT), magnesium oxide (MgO), neodymium gallium oxide ( $\text{NdGaO}_3$ , NGO) or silicon (Si), for example. In an embodiment, said providing is accomplished, for example, by  
20 depositing a layer of GCMO on to the substrate 370 using chemical solution deposition CSD, CSD, metalorganic chemical vapor deposition MOCVD, metalorganic deposition MOD or pulsed laser deposition PLD. Alternatively, the deposition may be accomplished by printing, jet printing, 3D printing, or for example by inkjet printing.

[0088] As illustrated in FIG. 6B, after the plurality of first patterns 310 are provided,  
25 plurality of contact terminals 315 comprising, for example, gold or silver are attached to the plurality of first patterns 310. In an embodiment, a first pattern comprises a plurality of such contact terminals, that may be used for attaching additional and/or external electronics, and may be used to, for example, set the resistance of the memristive material. In an embodiment, such connections may be added after the formation of the memristor.

30 [0089] Then, as illustrated in FIG. 6C, an electrically insulating layer 330 is provided on the first pattern 310. Such provision may be accomplished, for example, by depositing

said electrically insulating layer 330 using atomic layer deposition, ALD. Another examples for depositing said electrically insulating layer 330 comprise, chemical vapor deposition CVD, physical vapor deposition PVD, sputtering, electron beam deposition, thermal evaporation, spin-coating and chemical solution deposition CSD.

5 [0090] After providing the electrically insulating layer 330 onto the first pattern, at least one hole 340 is formed onto the electrically insulating layer 330 such that the at least one hole 340 extends to the first pattern 310, as illustrated in FIG. 6D. Forming of the at least one hole 340 may be done using wet chemical etching or dry etching, such as ion beam etching or reactive ion etching or argon gas etching.

10 [0091] Then, as illustrated in FIG. 6E, a plurality of second patterns 320 are provided on the electrically insulating layer 330 such that a first pattern 310 and a second pattern 320 are in contact through the at least one hole 340. An advantage of the at least one hole 340 delimiting the interface 350 between the first pattern 310 and the second pattern 320, is that the area of the interface can be controlled, for example, during the manufacturing process.

15 The area of the interface assists in the adjustment of the voltage range used for the resistive switching, RS, of the memristor. A benefit for the adjustment of the size of the interface is the ability to affect the packing density and resistance over said interface. For example, with a smaller area of the interface, a higher packing density and increased interface resistance may be obtained. Once the first pattern and the second pattern are in contact, such hole 340 defines a “via”. Providing a second pattern 320 may be done by lift-off process. The second pattern 320 may comprise, for example, copper, molybdenum, tungsten, indium, aluminium or titanium.

[0092] As can be appreciated from FIG. 6D and FIG. 6E, the holes 340 and the contacts of the first pattern and second pattern through the interfaces 350, respectively, may  
25 comprise varying size. In an embodiment, the second pattern comprises at least one connections such that said second pattern may be used for attaching said second pattern to external electronics. Such external and/or additional electronics include, for example, a voltage source. In another embodiment, the second pattern may have a form such that such connection are comprised in the second pattern, as can be seen in FIG. 6E.

30 [0093] It is noted, that forming a hole 340 is not only limited to the embodiment described above. In an alternative embodiment, using for example a lift-off process, a mask 380 is used prior to the application of the electrically insulating layer 330. An example of

such embodiments is presented in FIG. 7A – 7F illustrating phases of an example manufacturing method for an apparatus comprising a plurality of memristor arrays.

[0094] First, in FIG. 7A, a substrate 370 is obtained whereon at least one first pattern 310 is provided. In an embodiment, said providing is accomplished, for example, by depositing a layer of GCMO on to the substrate 370 using chemical solution deposition CSD metalorganic chemical vapor deposition MOCVD, metalorganic deposition MOD or pulsed laser deposition PLD. The substrate 370 may comprise strontium titanate ( $\text{SrTiO}_3$ ), silicon (Si) coated with strontium titanate, lanthanum aluminium oxide ( $\text{LaAlO}_3$ ), strontium lanthanum aluminium oxide ( $\text{SrLaAlO}_4$ , SLAO), lanthanum aluminate - strontium aluminium tantalate (LSAT), magnesium oxide ( $\text{MgO}$ ), neodymium gallium oxide ( $\text{NdGaO}_3$ , NGO) or silicon (Si), for example.

[0095] After the at least one first pattern 310 is provided, a mask 380 is formed on the surface of the at least one first pattern as illustrated in FIG. 7B. The mask 380 may be, for example, a set of cylindrically, or cubically, shapes, for example, comprising a photoresist.

[0096] In FIG. 7C, the electrically insulating layer 330 is formed at least in part on the at least one first pattern 310, and, in FIG. 7D, said mask 380 has been removed. Thus, a hole 340 delimited by the electrically insulating layer 330 is obtained such that the hole 340 extends through the electrically insulating layer 330 to the at least one first pattern 310.

[0097] As illustrated in FIG. 7E, after the hole 340 has been formed, at least one second pattern 320 is deposited at least in part into the hole 340, thus, forming a contact between the at least one first pattern 310 and at least one second pattern 320 through an interface 350.

[0098] According to the example embodiment illustrated in FIG. 7F, connections 325 are added to the at least one second pattern 320.

[0099] An advantage of the provided method for manufacturing a memristor device according to at least some embodiments is that because the GCMO provides the electrical connection between memristor devices, and said GCMO memristive material is comprised in a first pattern, the phases for manufacturing memristor devices are reduced. This is at least in part because no additional first pattern, made from, or comprising of, a non-memristive material, may need to be provided. In turn, reducing the number of manufacturing phases also reduces device-to-device variation in the manufactured devices and arrays. Further,

according to at least some embodiments, the at least one hole in the electrically insulating layer defines the contact area for the interface between the first pattern and the second pattern, which in turn provides beneficial embodiments wherein resistivity switching may be more precisely controlled for memristor devices and memristor arrays.

- 5   **[00100]**        Although at least some of the disclosed embodiments regarding manufacturing memristor devices comprised in a memristor array comprise phases in a specified order, for example, a specified order in which a first pattern is provided prior to the provision of a second pattern, other order for such phases may also be available.

- 10   **[00101]**        According to at least some embodiments, a first pattern and a second pattern may be provided in an alternative order. In other words, such embodiments comprise providing a second pattern of a memristor device prior to a first pattern of the same memristor device. Such embodiments may be beneficial in providing memristor arrays comprising multiple layers or multiple planes, connected to one another via first patterns and/or second patterns. Such multiple planes may be construed as so-called stacks of  
15   memristor devices, or three-dimensional memristor arrays with a plurality of layers comprising a plurality of first patterns and a plurality of second patterns. Such layers may comprise a plurality of layers comprising sequential, alternating and/or otherwise varying layers and/or planes comprising first patterns and second patterns.

- 20   **[00102]**        The terms “three-dimensional structure” and “three-dimensional memristor array” as it is to be understood in the context of memristor arrays and memristor devices disclosed, as a structure that comprises at least two different layers and/or planes comprising first patterns and/or at least two different layers and/or planes comprising second patterns. For example, such a three-dimensional structure may have two or more planes and/or layers comprising a first pattern, connecting two or more second patterns on different planes,  
25   through an interface. Such a structure may also be understood as a memristor array comprising a “multilayer” or “multiplane” structure.

- 30   **[00103]**        It can also be appreciated, that even though at least some of the disclosed embodiments comprise a layer of first patterns and a layer of second patterns, the second patterns connected to at least one first pattern via an interface, other configurations and/or orientations of such layers, and patterns exists. For example, first patterns and second patterns may exists on a same plane.

[00104] In FIG. 8A, there is provided a perspective view of a memristor array 500 comprising a multiple layers, and in FIG. 8B there is provided a side view of said memristor array 500. As can be appreciated from FIG. 8A, two second patterns 320a & 320b are connected via at least one common first pattern 310a, 310b & 310c. In FIG. 8A and 8B, a  
5 third first pattern 310c is connected to said two second patterns 320a and 320b via an interface 350c. Although an electrically insulating layer is not presented in FIG. 8A and 8B, such an electrically insulating layer may be comprised in such memristor array, thus delimiting the area of an interface through which a first pattern is in contact with a second pattern.

10 [00105] The layered structure is further illustrated in FIG. 9, wherein there is provided an example memristor array 600 capable of supporting at least some embodiments. The example memristor array 600 of FIG. 9 comprises four second patterns 320 and two first patterns 310. The second patterns are in contact with at least one first pattern through an interface 350. Further, the second patterns 320 of memristor array 600 are connected to at  
15 least one other second pattern 320 via a common first pattern 310. Furthermore, the first patterns 310 and second patterns 320 comprise different geometries. As can be also appreciated from FIG. 9, the memristor devices are layered, in other words, not all second patterns and/or first patterns are on, or near, the same layer or plane. Furthermore, a plurality of electrically insulating layers 330 are used to delimit the interface 350 through which a  
20 first pattern 310 is in contact with a second pattern 320. As can also be appreciated, said interfaces may have simple geometric shapes, or more complex geometric shapes. For illustrative purposes in FIG. 9, the superimposed non-visible layers and/or parts thereof are shown as a dashed line.

[00106] In FIG. 10, there is provided an example memristor array 700, wherein the  
25 second patterns 320a, 320b & 320c are non-perpendicular to a plurality of first patterns 310a, 310b & 310c. As can be appreciated, the example memristor array 700 also illustrates a layered structure, wherein a second pattern 320b is on a different layer to the two other second patterns 320a & 320c. Memristor arrays, such as the memristor array 700 of FIG. 10, may be beneficial to scale-up memristor arrays and thus, such arrays may provide compact  
30 structures and geometries for applications regarding memristors.

[00107] It is to be understood that the embodiments of the invention disclosed are not limited to the particular structures, process steps, or materials disclosed herein, but are

extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

5 [00108] Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment.

10 [00109] As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their  
15 presentation in a common group without indications to the contrary. In addition, various embodiments and example of the present invention may be referred to herein along with alternatives for the various components thereof. It is understood that such embodiments, examples, and alternatives are not to be construed as de facto equivalents of one another, but are to be considered as separate and autonomous representations of the present invention.

20 [00110] Furthermore, the described features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. In the following description, numerous specific details are provided, such as examples of lengths, widths, shapes, etc., to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more  
25 of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

[00111] While the forgoing examples are illustrative of the principles of the present invention in one or more particular applications, it will be apparent to those of ordinary skill  
30 in the art that numerous modifications in form, usage and details of implementation can be made without the exercise of inventive faculty, and without departing from the principles

and concepts of the invention. Accordingly, it is not intended that the invention be limited, except as by the claims set forth below.

[00112] The verbs “to comprise” and “to include” are used in this document as open limitations that neither exclude nor require the existence of also un-recited features. The features recited in depending claims are mutually freely combinable unless otherwise explicitly stated. Furthermore, it is to be understood that the use of "a" or "an", i.e. a singular form, throughout this document does not exclude a plurality.

INDUSTRIAL APPLICABILITY

[00113] The present disclosure may find use cases and industrial applicability in the field of memristive materials and memristor devices.

ACRONYMS LIST

|       |                                                        |
|-------|--------------------------------------------------------|
| ALD   | atomic layer deposition                                |
| CSD   | chemical solution deposition                           |
| CVD   | chemical vapor deposition                              |
| EUVL  | extreme ultraviolet lithography                        |
| GCMO  | memristive material with a formula $Gd_{1-x}Ca_xMnO_3$ |
| HRS   | high resistivity state                                 |
| LRS   | low resistivity state                                  |
| LSAT  | lanthanum aluminate - strontium aluminium tantalate    |
| MBE   | molecular beam epitaxy                                 |
| MOCVD | metalorganic chemical vapor deposition,                |
| MOD   | metalorganic deposition                                |
| NGO   | neodymium gallium oxide, $NdGaO_3$ , NGO               |

|   |     |                           |
|---|-----|---------------------------|
|   | NIL | nanoimprint lithography   |
|   | PLD | pulsed laser deposition   |
|   | PVD | physical vapor deposition |
|   | RS  | resistive switching       |
| 5 | STO | strontium titanate        |

REFERENCE SIGNS LIST

|                                  |                                          |
|----------------------------------|------------------------------------------|
| 100                              | memristor device                         |
| 200, 300, 400, 500, 600, 700     | memristor array                          |
| 110, 310, 310a, 310b, 310c       | first pattern                            |
| 111                              | first portion of a first pattern         |
| 112                              | second portion of a first pattern        |
| 115, 315                         | contact terminal of a first pattern      |
| 120, 120a, 120b, 320, 320a, 320b | second pattern                           |
| 121                              | third portion of a second pattern        |
| 122                              | fourth portion of a second pattern       |
| 125, 325                         | contact terminal of a second pattern     |
| 130, 330                         | electrically insulating layer            |
| 340                              | hole in an electrically insulating layer |

|                         |                                                                        |
|-------------------------|------------------------------------------------------------------------|
| 150, 350, 350a,<br>350c | interface, wherein a first pattern and a second pattern are in contact |
| 170, 370                | substrate                                                              |
| 380                     | mask                                                                   |

CITATION LIST

Patent Literature

WO 2021/152215 A1

5 WO 2024/003454 A1 (Appl. No. PCT/FI2023/050399)

## CLAIMS:

1. A memristor array, comprising at least two memristor devices, the memristor devices comprising
- 5       — a first pattern comprising memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein  $x$  has a value more than 0.6 and less than 0.99; and
- a second pattern comprising oxidizable metal, wherein the second pattern is in contact with the first pattern over an interface comprising at least one oxide of the oxidizable metal,
- 10   wherein at least one memristor device of the memristor array is connected to at least one other memristor device of the memristor array via the first pattern.
2. The memristor array according to claim 1, wherein the first pattern consists essentially of memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein  $x$  has a value more than 0.6 and
- 15   less than 0.99.
3. The memristor array according to claim 1 or claim 2, wherein the first pattern consists of memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ , wherein  $x$  has a value more than 0.6 and less than 0.99.
- 20   4. The memristor array according to any one of the preceding claims, wherein the first pattern is obtained from a deposited and patterned layer of memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ .
- 25   5. The memristor array according to any one of the preceding claims, wherein the at least one memristor device of the memristor array connected to the at least one other memristor device of the memristor array both comprise said interface over which the second pattern is in contact with the first pattern.
- 30   6. The memristor array according to any one of the preceding claims, wherein the at least one memristor device is connected to the at least one other memristor device via the first pattern such that the memristive material of the first pattern extends from the at least one memristor device to the at least one other memristor device.

7. The memristor array according to any one of the preceding claims, wherein memristor devices have at least the first pattern or the second pattern in common with at least one other memristor device.
- 5 8. The memristor array according any one of the preceding claims, wherein a contact area between the first pattern and the second pattern over the interface is between  $2 \text{ nm}^2$  and  $2500 \text{ }\mu\text{m}^2$ , or between  $5 \text{ nm}^2$  and  $500 \text{ }\mu\text{m}^2$ , or between  $10 \text{ nm}^2$  and  $10 \text{ }\mu\text{m}^2$ , or between  $20 \text{ nm}^2$  and  $50 \text{ nm}^2$ , or between  $30 \text{ nm}^2$  and  $100 \text{ nm}^2$ , or between  $50 \text{ nm}^2$  and  $500 \text{ nm}^2$ .
- 10 9. The memristor array according to any one of the preceding claims, wherein  $x$  has a value between 0.65 and 0.975, or between 0.7 and 0.95, or between 0.75 and 0.9, or between 0.76 and 0.89, or between 0.77 and 0.88, or between 0.78 and 0.87, or between 0.79 and 0.86.
10. The memristor array according to any one of the preceding claims, wherein for at least  
15 one memristor device  
the first pattern comprises a first portion and a second portion; and  
the second pattern comprises a third portion and a fourth portion;  
wherein the first portion is in contact with the third portion over the interface and the second portion is separated from the fourth portion by an electrically insulating layer.
- 20 11. The memristor array according to claim 10, wherein for at least one memristor device, the third portion comprises a protrusion through a hole in the electrically insulating layer, and the protrusion is in contact with the first portion of the first pattern.
- 25 12. The memristor array according to claim 10 or claim 11, wherein the electrically insulating layer comprises at least one of aluminium oxide, silicon dioxide, titanium oxide, silicon nitride and strontium titanate.
- 30 13. The memristor array according to any one of the preceding claims, wherein the second pattern comprises at least one of copper, molybdenum, tungsten, indium, aluminium and titanium.

14. The memristor array according to any one of claims 10 to 13, wherein material of the third portion comprises the oxidizable metal of the second pattern and the fourth portion comprises material different from the material of the third portion.
- 5 15. The memristor array according to any one of the preceding claims, wherein the second pattern has a thickness of more than 1 nm, or more than 1.8 nm, or more than 2 nm, or more than 5 nm, or more than 10 nm, or more than 20 nm, or more than 30 nm, or more than 50 nm, or more than 100 nm, or more than 300 nm, or more than 500 nm.
- 10 16. The memristor array according to any one of the preceding claims, wherein the first pattern has a thickness of more than 10 nm, or more than 20 nm, or more than 30 nm, or more than 50 nm, or more than 100 nm, or more than 300 nm, or more than 500 nm.
- 15 17. A method for manufacturing at least two memristor devices comprised in a memristor array, the method comprising:  
providing a first pattern, the first pattern comprising memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x has a value more than 0.6 and less than 0.99; and  
providing a second pattern comprising oxidizable metal such that the second pattern is in contact with the first pattern over an interface comprising at least one oxide of the  
20 oxidizable metal,  
wherein at least one memristor device of the memristor array is connected to at least one other memristor device of the memristor array via the first pattern.
- 25 18. The method according to claim 17, wherein the first pattern consists essentially of memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x has a value more than 0.6 and less than 0.99.
- 30 19. The method according to claim 17 or 18, wherein the first pattern consists of memristive material with formula  $Gd_{1-x}Ca_xMnO_3$ , wherein x has a value more than 0.6 and less than 0.99.

20. The method according to any one of claims 17 to 19, wherein the memristor devices have at least the first pattern or the second pattern in common with at least one other memristor device of the array.
- 5 21. The method according to any one of claims 17 to 20, wherein providing the first pattern further comprises
- depositing a layer of memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$ ; and
- patterning the layer of memristive material with formula  $\text{Gd}_{1-x}\text{Ca}_x\text{MnO}_3$  to obtain the first pattern.
- 10 22. The method according to any one of claims 17 to 21, wherein x has a value between 0.65 and 0.975, or between 0.7 and 0.95, or between 0.75 and 0.9, or between 0.76 and 0.89, or between 0.77 and 0.88, or between 0.78 and 0.87, or between 0.79 and 0.86.
- 15 23. The method according to any one of claims 17 to 22, wherein providing the second pattern comprises
- depositing an electrically insulating layer at least in part on the first pattern;
- forming a hole through the electrically insulating layer to the first pattern, the hole defining a location for the contact; and
- 20 24. depositing oxidizable metal at least in the hole in order to obtain the second pattern such that the second pattern is in contact with the first pattern over the interface.
24. The method according to claim 23, wherein the electrically insulating layer comprises at least one of aluminium oxide, silicon dioxide, silicon nitride, titanium oxide, and strontium
- 25 titanate.
25. The method according to claim 23 or claim 24, wherein depositing oxidizable metal further comprises
- depositing an oxidizable metal in the hole; and
- 30 26. depositing an electrically conductive metal such that the electrically conductive metal is in contact with the oxidizable metal in order to obtain the second pattern comprising the oxidizable metal and the electrically conductive metal.

26. The method according to any one of claims 17 to 25, wherein the contact between the first pattern and the second pattern over the interface is between  $2 \text{ nm}^2$  and  $2500 \text{ }\mu\text{m}^2$ , or between  $5 \text{ nm}^2$  and  $500 \text{ }\mu\text{m}^2$ , or between  $10 \text{ nm}^2$  and  $10 \text{ }\mu\text{m}^2$ , or between  $20 \text{ nm}^2$  and  $50 \text{ nm}^2$ , or between  $30 \text{ nm}^2$  and  $100 \text{ nm}^2$ , or between  $50 \text{ nm}^2$  and  $500 \text{ nm}^2$ .

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27. The method according to any one of claims 17 to 26, wherein the method further comprises heat-treatment of the interface at a temperature between  $20 \text{ }^\circ\text{C}$  and  $400 \text{ }^\circ\text{C}$ .

28. The method according to any one of claims 17 to 27, wherein the second pattern  
10 comprises at least one of copper, molybdenum, tungsten, indium, aluminium and titanium.