

Abstract of Disclosure

METHOD FOR FORMING AN OFFSET SPACER OF A MOS DEVICE

A method for forming an offset spacer of a MOS device is disclosed. The method includes the steps of: providing a substrate having a gate structure thereon; forming a dielectric stack on the substrate and the gate structure, wherein the dielectric stack comprises a first dielectric layer, a second dielectric layer, a third dielectric layer, and a fourth dielectric layer; and performing an etching process on the dielectric stack to form an offset spacer around the gate structure.

Figure 4