Description

This invention relates to digital processing of video signals and, in particular, to the delay of video signals to eliminate raster distortion and convergence errors.

A digital color television system may sample an analog video signal at a predetermined rate, for example, 14.32 MHz, which, for NTSC color signals, is four times the color subcarrier frequency. The signal amplitude of each sample is converted to a digital value by an analog-to-digital converter (ADC). The digitized video signal is processed to form red, green and blue drive signals which, after conversion back to the analog domain by a digital-to-analog converter (DAC), are applied to the electron guns of the color cathode ray tube.

Both digital and analog television receivers are subject to raster distortion and convergence errors. Horizontal convergence errors and raster distortion, such as side pincushion distortion, may be corrected by selectively delaying one or more of the individual color signals in a given horizontal scan line in order to converge the three colors on the cathode ray tube display screen and correct the distortion. In a digital system, this delay may be accomplished by clocking the digital samples into a storage device, such as a random access memory (RAM) and clocking the samples out of the RAM after a predetermined number of clock pulses. This technique permits video information and, consequently, entire video lines to be moved in steps equal to the distance between adjacent digital samples, or pixels, on the cathode ray tube display screen.

Actual convergence and distortion errors may require that the video information be moved a fraction of a whole sample to provide correction within a specified tolerance. US-A-480,907, filed March 31, 1983, in the name of T. V. Bolger and entitled, "Digital Video Processing System with Raster Distortion Correction", corresponding to UK published application GB-A-2137849A, published 10 October 1984, describes a digital television system having a multiphase clock for reading samples out of a digital sample storage device. The phase of the clock is selected to provide the amount of sample delay necessary to give the desired raster distortion or convergence correction for each of the three colors.

The present invention provides in a video apparatus incorporating a cathode ray tube producing an electron beam that impinges on a display screen to form an image representative of a video information signal, which comprises a plurality of video information samples, an apparatus for correcting in an advantageous manner a predetermined amount of horizontal electron beam landing position error for said image on said display screen. This apparatus is characterized by combining, with means for providing in accordance with said electron beam landing error a first amount of beam landing position error time delay for said plurality of video information samples equal to a whole number of delay steps corresponding to respective amounts of electron beam landing error correction, means for providing a nominal amount of time delay for said plurality of video information samples, said first amount of time delay corresponding to an increase or decrease of said nominal amount, and means for combining in accordance with said electron beam landing error selected fractional values of pairs of said plurality of video information samples to provide an apparent amount of time delay for said plurality of video information samples, which delay represents fractional delay steps also corresponding to an increase or decrease of time delay with respect to said nominal amount of time delay, the resultant of said first, nominal and apparent amounts of time delay substantially providing correction for said predetermined amount of horizontal beam landing position error. In this way it becomes possible, while using a sampling clock having a fixed frequency and a single phase to provide an equivalent of fractional sample delays in order to correct distortions within closely defined tolerances.

In the accompanying drawing:

FIGURE 1 is a schematic diagram of a digital signal processing circuit in accordance with an aspect of the present invention, and

FIGURE 2 illustrates waveforms useful in understanding the theory of operation of the circuit of FIGURE 1.

Referring to FIGURE 1 an analog composite video signal, from a source of video signals (not shown), is applied to an analog-to-digital converter (ADC) 10. ADC 10 generates digital signals at a sample rate determined by the clock signal frequency from a clock generator 11. The circuit of FIGURE 1 illustratively uses a sampling frequency equal to four times the color subcarrier frequency. For NTSC color signals having a color subcarrier of 3.58 MHz,the sampling frequency is 14.32 MHz. ADC 10 is illustratively shown as providing an 8-bit digital sample, thereby generating samples having $2^8 = 256$ quantizing steps.

The digitized video signal is applied to a synchronizing separator circuit 12, where it is processed to remove the horizontal and vertical synchronizing information, and to a digital comb filter 13. Digital comb filter 13 separates the luminance and chrominance information and applies the luminance information to luminance processing circuitry 14 which provides a luminance signal on a conductor designated Y to a digital matrix 15. Chrominance information from digital comb filter 13 is applied to chrominance processing circuitry 16, which generates the I and Q color signals in response to the properly phased I and Q clock signals, on conductors designated ICK and QCK, from clock generator 11. The I and Q color signals, on conductors I and Q, are also applied to digital matrix 15, which combines the luminance signal and the I and Q

color signals to produce the digital red, green and blue color signals on conductors DR, DG and DB, respectively.

Each of the digital red, green and blue color signals is applied to a digital delay circuit. FIGURE 1 shows, in detail, a digital delay circuit 20 which acts on the digital blue color signal via conductor DB. Similar delay circuits 21 and 22 for the digital red and green color signals are illustrated in block diagram form, for simplicity.

Digital matrix 15 generates digital color signal samples illustratively comprising 8 bits. These samples are applied to a buffer 24 via the digital blue signal conductor DB which produces a 16-bit sample pair comprising two adjacent 8-bit color signal samples. For example, subsequent sample pairs in a given horizontal scan line may comprise digital samples one and two, samples two and three, and samples three and four, such that each subsequent sample pair comprises one new 8-bit sample not included in the previous sample pair. The 16-bit sample pairs are stored in a random access memory (RAM) 25 in locations determined by a write address generator 26. Write address generator 26 is incremented by a write clock signal provided by clock generator 11 via conductor WRCK. The write clock signal is first applied to a gate circuit 27 which prevents the write clock signal from being applied to the write address generator 26 during the horizontal blanking interval. Gate circuit 27 operates in response to a signal from synchronizing pulse separator circuit 12. Write address generator 26 is reset each horizontal scan line by a horizontal reset pulse that may also be generated by synchronizing pulse separator 12.

A delay of the blue video signal is accomplished by writing a predetermined number of sample pairs into RAM 25 before any reading of sample pairs out of RAM 25 is begun. Sample pairs are written into RAM 25 at the write clock rate, i.e., 14.32 MHz, which corresponds to one sample pair being written into RAM 25 approximately every 70 nanoseconds. Each sample pair written into RAM 25 before sample pairs are read out of RAM 25 corresponds therefore to a delay of 70 nanoseconds. RAM 25, configured to accommodate 128 sample pairs, could therefore produce a maximum delay of 128 samples x 70 nanoseconds/sample = 8.96 µS. In order to provide horizontal movement of the digital red, green and blue color signals in either direction with respect to each other, a nominal delay is provided for each of the digital color signals on each horizontal scan line. The amount of actual delay desired for each of the color signals can then be provided by increasing or decreasing the delay relative to the nominal delay. For delay circuit 20 of FIGURE 1, a nominal delay of 4.48 µS, corresponding to 64 samples x 70 nS/sample, gives the maximum amount of relative sample movement that can be produced by RAM 25. For example, if the digital green color signal is processed by delay circuit 22 to have the nominal delay of 4.48 µS, the blue color signal, processed by delay circuit 20, may be delayed with respect to the green signal by a maximum of 4.48 µS, or the blue signal may be advanced with respect to the green signal by a maximum of 4.48 µS. The amount of the delay is determined by the time at which samples are read from RAM 25 relative to the time at which those samples were written into RAM 25.

The units of signal delay that have been discussed up to this point have been determined by whole numbers of clock pulses, i.e., 70 nanosecond steps. In actual operation, however, the amount of convergence or raster distortion requiring correction may not correspond to whole numbers of delay steps, but may require a fraction of a delay step in order to bring the convergence or distortion errors within desired tolerances or specifications.

Delay circuits 20, 21 and 22 incorporate means providing an equivalent of fractional amounts of whole delay steps in order to accurately correct convergence and raster distortion errors. In accordance with an aspect of the present invention, the fractional delay steps are achieved via sample interpolation circuitry which operates in the following manner.

The convergence errors and amounts of raster distortion (side pincushion distortion, for example) for a given video display apparatus are determined during assembly of the video display apparatus. One technique for determining this error utilizes photodiodes placed at various screen locations to sense actual electron beam landing positions. Knowing the desired beam landing positions in order to produce a raster without misconvergence or distortion errors allows a determination of the amount of shift needed in the beam landing positions in order to accomplish the desired corrections. This shift information is utilized to program a read-only-memory (ROM) 30 during assembly or alignment of the video display apparatus. The ROM 30, which illustratively includes misconvergence and distortion information for each digital sample of each horizontal scan line, is individually programmed for a particular cathode ray tube of a particular video display apparatus.

For a given horizontal scan line, the amount of blue signal delay needed (nominal delay plus or minus delay shift) to effect the desired corrections is provided by ROM 30 to a read delay counter 31 via a conductor identified as PRESET. Read delay counter 31 is incremented by the write clock signal and begins to produce output pulses in response to write clock pulses when the number of preset sample delay steps from ROM 30 is reached. The output pulses from read delay counter 31 are applied to the input of an AND gate 32. Another input of AND gate 32 is coupled to the input of gate circuit 27, which is the write clock pulses. AND gate 32 will therefore produce output pulses representative of write clock pulses whenever the preset delay count has been exceeded. The AND gate 32 output pulses are applied to a read address generator 33, which is reset each horizontal line by a signal from sync separator 12.

Read address generator 33 is coupled to RAM 25 and accesses particular sample locations of RAM 25 at the frequency of the clock pulses from AND gate 32. Samples are read out of RAM 25 from addresses accessed by read address generator 33 in the order they were written into RAM 25 from buffer 24, i.e., first in first out. Read address generator 33 will always lag write address generator 26 so that information is always available to be read out.

As previously described, merely delaying the reading out of video samples from RAM 25 by a multiple of clock pulses may not provide accurate enough convergence or raster distortion correction. It may be necessary to have a delay equal to a fraction of the delay provided by one clock pulse delay. This fractional delay may be effected by sample interpolation, which will be explained with reference to FIGURE 2. FIGURE 2 illustrates a portion of an analog video waveform 35. Waveform 35 is illustratively shown as being digitally sampled, by an analog-to-digital converter, similar to ADC 10, for example, at sample points 35a—f. Sample interpolation combines a fraction of the digital amplitude values of adjacent samples to form a new sample having a new amplitude value. The fractions selected illustratively comprise a unity fractional complement; that is, the sum of the fractions selected for an adjacent sample pair should sum to unity.

In FIGURE 2, sample points 35a—f occur at times T_1—T_6, respectively, and have amplitude values of S_1—S_6, respectively. As an illustration of sample interpolation, the amplitude values of adjacent samples, such as the amplitude of sample 35a, equal to S_1, and the amplitude of sample 35b, equal to S_2, are combined, for example, using 1/2 as the fractional coefficient for each sample. The resultant samples will have amplitude values intermediate the original sample amplitudes, as shown by sample 36b, having an amplitude S^o, between S_1 and S_2. If the resultant samples are used to replace the original samples, as shown by samples 36b—36f in FIGURE 2, the effect is to generate a new encoded waveform 36 that gives the appearance of being shifted or delayed with respect to waveform 35 by an amount equal to one half a whole sample period. The fractional coefficients selected will determine the amount of apparent delay with respect to time T_1. For example, using 7/8 of the amplitude S_1 and 1/8 of the amplitude S_2 will produce an apparent delay of 1/8 the sample period from T_1 to T_2.

Similarly, if adjacent digital samples of a horizontal line of video information are combined in the previously described manner by using unity fractional complement coefficients, it is possible to shift the video information in as small an increment as desired, merely by selecting the proper fractional coefficients. A greater number of fractional parts of a selected coefficient will result in smaller possible apparent delay steps.

In an application such as is shown in FIGURE 1, the number of whole and fractional delay periods for each horizontal scanline is stored in ROM 30 to establish a horizontal starting point for the video signal information of each line. As described previously, the number of whole delay periods is applied to read delay counter 31 via the PRESET conductor, in order to determine when samples will begin to be read from RAM 25. A three-bit digital word, representative of the fractional delay coefficient, is applied to a coefficient control and counter circuit 40, which in turn applies the three-bit digital word to a sample interpolator circuit 41. Interpolator circuit 41 incorporates a buffer 42, shift and add circuits 43 and 44, inverter 45 and a summer 46. Buffer 42 reforms the 16-bit sample pair from RAM 25 into two 8-bit samples which are respectively applied to shift and add circuits 43 and 44. The three-bit word from coefficient control and counter circuit 40 is applied to shift and add circuit 43 and to inverter 45. The digital word value determines the number of digit shifts required by shift and add circuit 43. Inverter 45 forms a digital word representative of the unity fractional complement coefficient, which is applied to shift and add circuit 44 and determines the number of digit shifts. Shift and add circuits 43 and 44 perform the function of multiplying the values of samples from buffer 42 by their respective fractional coefficients. This is accomplished by shifting the appropriate number of bits of the digital samples based on the coefficient representative 3-bit words. Shifting bits therefore allows 8-bit digital samples to be moved in delay increments equal to 1/8 of the total sample period. Therefore, apparent delay increments of 8.75 nsec are possible. The outputs from shift and add circuits 43 and 44 are combined by summer 46 to form the resultant delay corrected video information sample. The output signal from summer 46 comprising delay corrected digital data occurring at the 14.32 MHz sample rate, is applied to a digital-to-analog (DAC) converter 47, which converts the digital data to the analog blue drive signal. The blue drive signal is then applied to the kinescope or cathode ray tube drive circuits which act to produce the desired blue-designated electron beam. Similarly, the outputs of delay circuits 21 and 22 are applied to digital-to-analog converters 50 and 51, respectively, which produce the red and green drive signals.

The previously described interpolation method, utilizing a single fractional coefficient pair, will provide the same amount of delay for each sample of a given horizontal scan line. This is appropriate for certain types of correction, such as raster centering; however, other types of misconvergence or distortion errors will require different amounts of correction, or sample delay, for different positions along a given horizontal scan line. For example, misconvergence is usually more severe at the ends of a horizontal line than at the center of the line. Similarly, side pincushion distortion will decrease in severity away from the edges of the cathode ray tube display screen. This requires a variable amount of sample delay for a given horizontal scan line. Since the amount of

delay change from sample to sample is relatively small, it is possible to accomplish the desired variable delay by changing the fractional coefficients.

The rate of delay change (the number of digital samples occurring between coefficient changes), and the delay change direction (whether the delay is increased or decreased) are also programmed into ROM 30 as a result of the error measurements taken during circuit assembly and alignment. The coefficient change and delay change direction data is applied to coefficient control and counter circuit 40. This delay change data either increments or decrements the coefficient counter, which in turn controls the operation of interpolator 41. When the coefficient counter of coefficient control and counter circuit 40 becomes incremented or decremented to its upper or lower limit, respectively, an output signal is applied to advance/hold control circuit 52. When the coefficient counter becomes incremented to its upper limit, advance/hold control circuit 52 increments read address generator 33 by one sample address. This is in addition to the normal address increments which occur in response to the clock pulses from AND gate 32. Similarly, when the coefficient counter becomes decremented to its lower limit, advance/hold control circuit 52 prevents read address generator from being incremented for a period of one clock pulse. This effectively resets the advance/hold control circuit 52.

In an analogous manner, the offsets and scan differences of the red, green and blue pickup devices of a color video camera can be compensated by utilizing the previously described technique of apparent signal delay by sample interpolation. A ROM may be programmed during assembly of the camera which will provide the appropriate correction amounts for each horizontal scan line.

The previously described sample interpolation technique therefore provides apparent delays of digitized video signals of small increments in order to correct misconvergence and raster distortion errors to within very small tolerances, thereby making the arrangement described in accordance with the present invention appropriate for high resolution cathode ray tubes.

Claims

1. In a video apparatus incorporating a cathode ray tube producing an electron beam that impinges on a display screen to form an image representative of a video information signal, said signal comprising a plurality of video information samples, apparatus for correcting a predetermined amount of horizontal electron beam landing position error for said image on said display screen comprising:

means (30, 31) for providing in accordance with said electron beam landing error a first amount of beam landing position error time delay for said plurality of video information samples equal to a whole number of delay steps corresponding to respective amounts of electron beam landing error correction,

and characterized by the combination with said means of:

means (31) for providing a nominal amount of time delay for said plurality of video information samples, said first amount of time delay corresponding to an increase or decrease of said nominal amount,

and means (42, 43, 44, 46) for combining in accordance with said electron beam landing error selected fractional values of pairs of said plurality of video information samples to provide an apparent amount of time delay for said plurality of video information samples, which delay represents fractional delay steps also corresponding to an increase or decrease of time delay with respect to said nominal amount of time delay, the resultant of said first, nominal and apparent amounts of time delay substantially providing correction for said predetermined amount of horizontal beam landing position error.

2. Apparatus as claimed in Claim 1, including means (30, 40) for selectively choosing first and second fractional sample coefficients for said fractional values.

3. Apparatus as claimed in Claim 1, wherein said selected fractional values represent amplitude weighting of said first and second samples, respectively.

4. Apparatus as claimed in Claim 1, arranged to receive, as said video information signal, a horizontal line of video information.

Patentansprüche

1. Anordnung zur Korrektur eines vorgegebenen Betrags eines horizontalen Elektronenstrahlauftreffpunktfehlers für ein Bild auf einem Anzeigeschirm für eine Videoeinrichtung mit einer Kathodenstrahlröhre, die einen auf den Anzeigeschirm auftreffenden Elektronenstrahl erzeugt, um das ein Videoinformationssignal darstellende Bild zu erzeugen, wobei das Signal eine Mehrzahl von Videoinformationsabtastwerten enthält, mit.

einer Einrichtung (30, 31) zum Erzeugen eines ersten Betrags einer Zeitverzögerung für den Strahlauftreffpunktfehler für die Mehrzahl der Videoinformationsabtastwerte gleich einer ganzen Anzahl von Verzögerungsschritten entsprechend jeweiligen Beträgen einer Elektronenstrahlauftreffehlerkorrektur, und

gekennzeichnet durch die Kombination der genannten Einrichtung mit:

einer Einrichtung (31) zum Erzeugen eines nominellen Betrages an Zeitverzögerung für die Mehrzahl von Videoinformationsabtastwerten, wobei der erste Betrag der Zeitverzögerung einer Zunahme oder Abnahme des nominellen Betrages entspricht, und einer Einrichtung (42, 43, 44, 46) zum Kombinieren ausgewählter gebrochenzahliger Werte von Paaren aus der Mehrzahl von Videoinformationsabtastwerten entsprechend dem Elektronenstrahlauftreffehler, um einen

delay change from sample to sample is relatively small, it is possible to accomplish the desired variable delay by changing the fractional coefficients.

The rate of delay change (the number of digital samples occurring between coefficient changes), and the delay change direction (whether the delay is increased or decreased) are also programmed into ROM 30 as a result of the error measurements taken during circuit assembly and alignment. The coefficient change and delay change direction data is applied to coefficient control and counter circuit 40. This delay change data either increments or decrements the coefficient counter, which in turn controls the operation of interpolator 41. When the coefficient counter of coefficient control and counter circuit 40 becomes incremented or decremented to its upper or lower limit, respectively, an output signal is applied to advance/hold control circuit 52. When the coefficient counter becomes incremented to its upper limit, advance/hold control circuit 52 increments read address generator 33 by one sample address. This is in addition to the normal address increments which occur in response to the clock pulses from AND gate 32. Similarly, when the coefficient counter becomes decremented to its lower limit, advance/hold control circuit 52 prevents read address generator from being incremented for a period of one clock pulse. This effectively resets the advance/hold control circuit 52.

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The previously described sample interpolation technique therefore provides apparent delays of digitized video signals of small increments in order to correct misconvergence and raster distortion errors to within very small tolerances, thereby making the arrangement described in accordance with the present invention appropriate for high resolution cathode ray tubes.

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means (30, 31) for providing in accordance with said electron beam landing error a first amount of beam landing position error time delay for said plurality of video information samples equal to a whole number of delay steps corresponding to respective amounts of electron beam landing error correction,

and characterized by the combination with said means of:

means (31) for providing a nominal amount of time delay for said plurality of video information samples, said first amount of time delay corresponding to an increase or decrease of said nominal amount,

and means (42, 43, 44, 46) for combining in accordance with said electron beam landing error selected fractional values of pairs of said plurality of video information samples to provide an apparent amount of time delay for said plurality of video information samples, which delay represents fractional delay steps also corresponding to an increase or decrease of time delay with respect to said nominal amount of time delay, the resultant of said first, nominal and apparent amounts of time delay substantially providing correction for said predetermined amount of horizontal beam landing position error.

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3. Apparatus as claimed in Claim 1, wherein said selected fractional values represent amplitude weighting of said first and second samples, respectively.

4. Apparatus as claimed in Claim 1, arranged to receive, as said video information signal, a horizontal line of video information.

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1. Anordnung zur Korrektur eines vorgegebenen Betrags eines horizontalen Elektronenstrahlauftreffpunktfehlers für ein Bild auf einem Anzeigeschirm für eine Videoeinrichtung mit einer Kathodenstrahlröhre, die einen auf den Anzeigeschirm auftreffenden Elektronenstrahl erzeugt, um das ein Videoinformationssignal darstellende Bild zu erzeugen, wobei das Signal eine Mehrzahl von Videoinformationsabtastwerten enthält, mit.

einer Einrichtung (30, 31) zum Erzeugen eines ersten Betrags einer Zeitverzögerung für den Strahlauftreffpunktfehler für die Mehrzahl der Videoinformationsabtastwerte gleich einer ganzen Anzahl von Verzögerungsschritten entsprechend jeweiligen Beträgen einer Elektronenstrahlauftreffehlerkorrektur, und

gekennzeichnet durch die Kombination der genannten Einrichtung mit:

einer Einrichtung (31) zum Erzeugen eines nominellen Betrages an Zeitverzögerung für die Mehrzahl von Videoinformationsabtastwerten, wobei der erste Betrag der Zeitverzögerung einer Zunahme oder Abnahme des nominellen Betrages entspricht, und einer Einrichtung (42, 43, 44, 46) zum Kombinieren ausgewählter gebrochenzahliger Werte von Paaren aus der Mehrzahl von Videoinformationsabtastwerten entsprechend dem Elektronenstrahlauftreffehler, um einen

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anscheinenden Betrag an Zeitverzögerung für die Anzahl der Videoinformationsabtastwerte zu erzeugen, wobei die Verzögerung gebrochenzahlige Verzögerungsschritte repräsentiert, die ebenfalls einer Zunahme oder Abnahme der Zeitverzögerung in Bezug auf den nominellen Betrag der Zeitverzögerung entsprechen, und wobei das Ergebnis des ersten, nominellen und anscheinenden Betrags der Zeitverzögerung im wesentlichen eine Korrektur des vorgegebenen Betrags des horizontalen Strahlauftreffpunktfehlers bewirkt.

2. Anordnung nach Anspruch 1, gekennzeichnet durch eine Einrichtung (30, 40) zur jeweiligen Auswahl eines ersten und eines zweiten gebrochenzahligen Abtastwertkoeffizienten für die gebrochenzahligen Werte.

3. Anordnung nach Anspruch 1, dadurch gekennzeichnet, daß die ausgewählten gebrochenzahligen Werte eine Amplitudenwichtung des ersten bzw. des zweiten Abtastwerts repräsentieren.

4. Anordnung nach Anspruch 1, dadurch gekennzeichnet, daß sie zur Aufnahme einer Horizontalzeile einer Videoinformation als Videoinformationssignal eingerichtet ist.

Revendications

1. Dans un dispositif vidéo incorporant un tube à rayons cathodiques produisant un faisceau d'électrons qui fait impact sur un écran de visualisation pour former une image représentative d'un signal d'information vidéo, ledit signal comprenant un certain nombre d'échantillons d'information vidéo, un dispositif pour corriger une quantité prédéterminée d'erreur de position horizontale d'impact du faisceau d'électrons pour ladite image sur ledit écran de visualisation comprenant:

un moyen (30, 31) pour produire, selon ladite erreur d'impact du faisceau d'électrons, une première quantité de retardement d'erreur de position d'impact du faisceau pour ladite quantité d'échantillons d'information vidéo égale à un nombre entier d'étapes de retardement correspondant à des quantités respectives de correction d'erreur d'impact du faisceau d'électrons,

et caractérisé par la combinaison avec ledit moyen de:

un moyen (31) pour produire une quantité nominale de retardement pour ladite quantité d'échantillons d'information vidéo, ladite première quantité de retardement correspondant à une augmentation ou une diminution de ladite quantité nominale,

et un moyen (42, 43, 44, 46) pour combiner, selon ladite erreur d'impact du faisceau d'électrons, des valeurs fractionnées choisies de paires desdits échantillons d'information vidéo pour produire une quantité apparente de retardement pour ladite quantité d'échantillons d'information vidéo, lequel retardement représente des étapes fractionnées de retardement correspondant également à une augmentation ou une diminution du retardement relativement à ladite quantité nominale de retardement, le résultat de ladite première quantité et desdites quantités nominale et apparente de retardement donnant sensiblement la correction de ladite quantité prédéterminée d'erreur de position horizontale d'impact du faisceau.

2. Dispositif selon la revendication 1, comprenant un moyen (30, 40) pour choisir sélectivement des premier et second coefficients d'échantillon fractionnés pour lesdites valeurs fractionnées.

3. Dispositif selon la revendication 1, où lesdites valeurs fractionnées choisies représentent une pondération d'amplitude desdits premier et second échantillons respectivement.

4. Dispositif selon la revendication 1, agencé pour recevoir, en tant que signal d'information vidéo, une ligne horizontale de l'information vidéo.