ABSTRACT

A METHOD TO FORM SHALLOW TRENCH ISOLATIONS WITHOUT A CHEMICAL MECHANICAL POLISH

A new method of fabricating shallow trench isolations has been achieved. No final polishing down process is needed. A silicon substrate is provided. A pad oxide layer is formed overlying the silicon substrate. A silicon nitride layer is deposited overlying the pad oxide layer. The silicon nitride layer, the pad oxide layer, and the silicon substrate are patterned to form trenches for planned shallow trench isolations. A liner oxide layer is grown overlying the semiconductor substrate is the trenches. A silicon dioxide spacer layer is deposited overlying the silicon nitride layer and the liner oxide layer to partially fill the trenches. The silicon dioxide spacer layer and the liner oxide layer are anisotropically etched to form sidewall spacers inside the trenches and to expose the bottom of said trenches. A silicon layer is selectively grown overlying the semiconductor substrate in the trenches. The silicon layer partially fills the trenches. A trench oxide layer is formed overlying the silicon layer. The silicon nitride layer is removed. The pad oxide layer is removed to complete the shallow trench isolation, and the integrated circuit device is completed.

FIGURE 3 IS SUGGESTED FOR PUBLICATION