CLAIMS

1. A semiconductor processing method comprising:

forming a semiconductor layer stack from pairs of Si-and-SiGe layers, wherein the pairs of Si-and-SiGe layers are formed by:

forming a silicon layer;

forming a germanium barrier layer on the silicon layer,

wherein the germanium barrier layer is less than or equal to 20 Å; and

wherein the germanium barrier layer comprises a silicon oxide layer that is formed by exposing the silicon layer to an oxidation plasma generated from an oxidation precursor comprising O_2; and

forming a silicon-germanium layer on the germanium barrier layer, wherein the silicon-germanium layer comprises greater than or equal to 30 at.% germanium.

2. The semiconductor processing method of claim 1, wherein the silicon layer is exposed to the oxidation plasma for less than or equal to 5 seconds.

3. The semiconductor processing method of claim 1, wherein the silicon-germanium layer comprises greater than or equal to 35 at.% germanium.

4. The semiconductor processing method of claim 1,

wherein the method further comprises forming a second germanium barrier layer on the silicon-germanium layer; and

wherein the second germanium barrier layer is less than or equal to 20 Å.

5. The semiconductor processing method of claim 1, wherein the method further comprises annealing the semiconductor layer stack at a temperature greater than or equal to 800 ºC.

6. The semiconductor processing method of claim 1, wherein the method further comprises treating the semiconductor layer stack to a rapid thermal anneal at a temperature greater than or equal to 1000 ºC.

7. The semiconductor processing method of claim 1, wherein the semiconductor layer stack has greater than or equal to 50 pairs of the Si-and-SiGe layers.

8. A semiconductor processing method comprising:

forming a silicon layer on a substrate;

exposing the silicon layer to an oxidation plasma generated from an oxidation precursor comprising O_2,

wherein the silicon layer is exposed to the oxidation plasma for less than or equal to 5 seconds; and

wherein the exposure forms a silicon oxide layer on the silicon layer;

depositing a silicon-germanium layer on the silicon oxide layer; and

annealing the substrate containing the silicon-germanium layer at a temperature greater than or equal to 1000 ºC.

9. The semiconductor processing method of claim 8, wherein the oxidation precursor further comprises argon.

10. The semiconductor processing method of claim 8, wherein a plasma power is delivered to the oxidation precursor to generate the oxidation plasma, and wherein the plasma power delivered to the oxidation precursor is less than or equal to 500 Watts.

11. The semiconductor processing method of claim 8,

wherein the oxidation plasma is generated in a substrate processing chamber that holds the substrate; and

wherein the substrate processing chamber is characterized by a pressure greater than or equal to 5 Torr during the generation of the oxidation plasma.

12. The semiconductor processing method of claim 8, wherein the silicon oxide layer is characterized by a thickness less than or equal to 10 Å.

13. A semiconductor structure comprising:

a silicon-germanium layer;

a silicon layer, wherein the silicon layer is characterized by less than or equal to 0.1 wt. % germanium; and

a germanium barrier layer in direct contact with the silicon layer and the silicon-germanium layer and positioned between the silicon layer and silicon-germanium layer,

wherein the germanium barrier layer is characterized by a thickness less than or equal to 10 Å; and

wherein the germanium barrier layer comprises a silicon oxide layer that is formed by exposing the silicon layer to an oxidation plasma generated from an oxidation precursor comprising O_2.

14. The semiconductor structure of claim 13, wherein the silicon layer is exposed to the oxidation plasma for less than or equal to 5 seconds.

15. The semiconductor structure of claim 13, wherein the less than or equal to 0.1 wt.% germanium in the silicon layer comprises crystalline germanium.

16. The semiconductor structure of claim 13,

wherein the structure further comprises a second germanium barrier layer in contact with the silicon-germanium layer; and

wherein the second germanium barrier layer is less than or equal to 20 Å.

17. The semiconductor structure of claim 13, wherein at least one of the silicon-germanium layer and the silicon layer is characterized by a thickness greater than or equal to 20 nm.

18. The semiconductor structure of claim 13, wherein the silicon-germanium layer is characterized by greater than or equal to 5 at.% germanium.

19. The semiconductor structure of claim 13, wherein the silicon layer comprises crystalized silicon.