FIG. 1

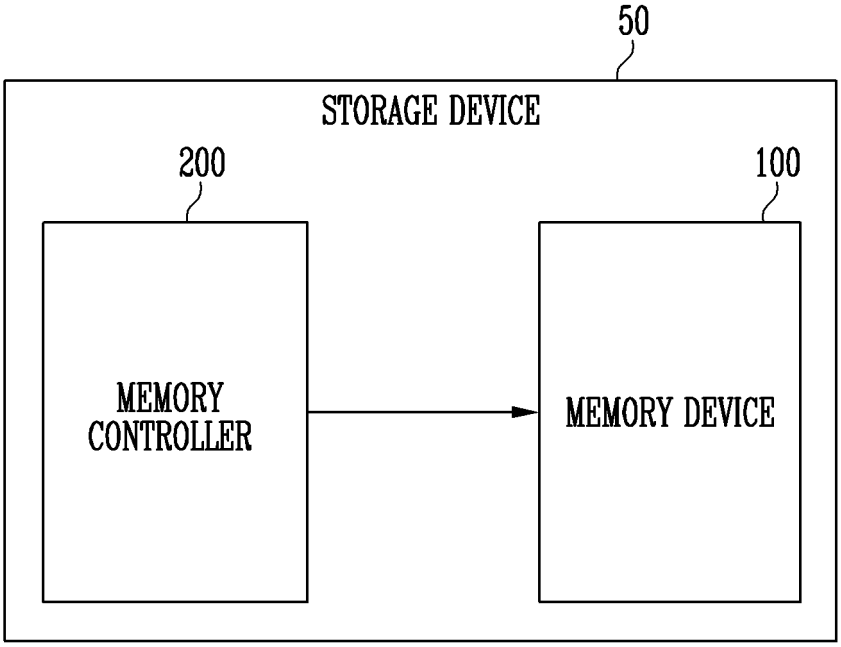


FIG. 2

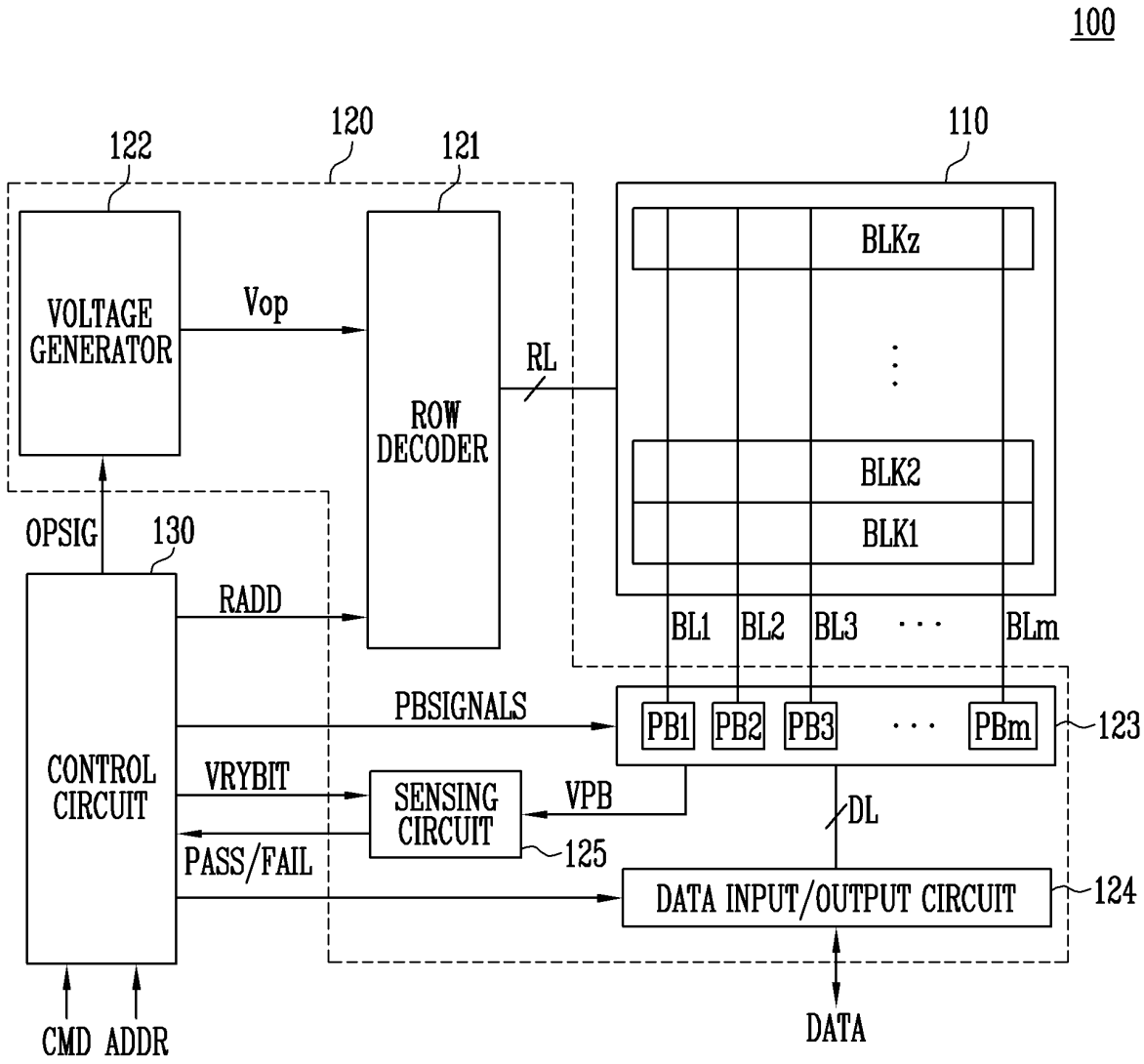

100
120
122
121
110
VOLTAGE GENERATOR
Vop
ROW DECODER
RL
BLKz
BLK2
BLK1
OPSIG
130
RADD
BL1
BL2
BL3
BLm
PBSIGNALS
PB1
PB2
PB3
PBm
123
CONTROL CIRCUIT
VRYBIT
SENSING CIRCUIT
VPB
DL
125
PASS/FAIL
DATA INPUT/OUTPUT CIRCUIT
124
CMD
ADDR
DATA

FIG. 3

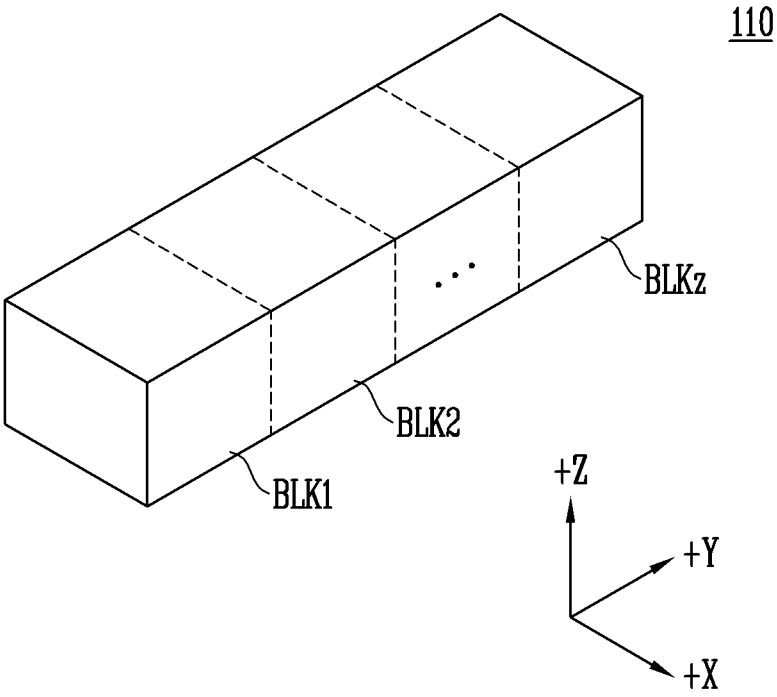


FIG. 4

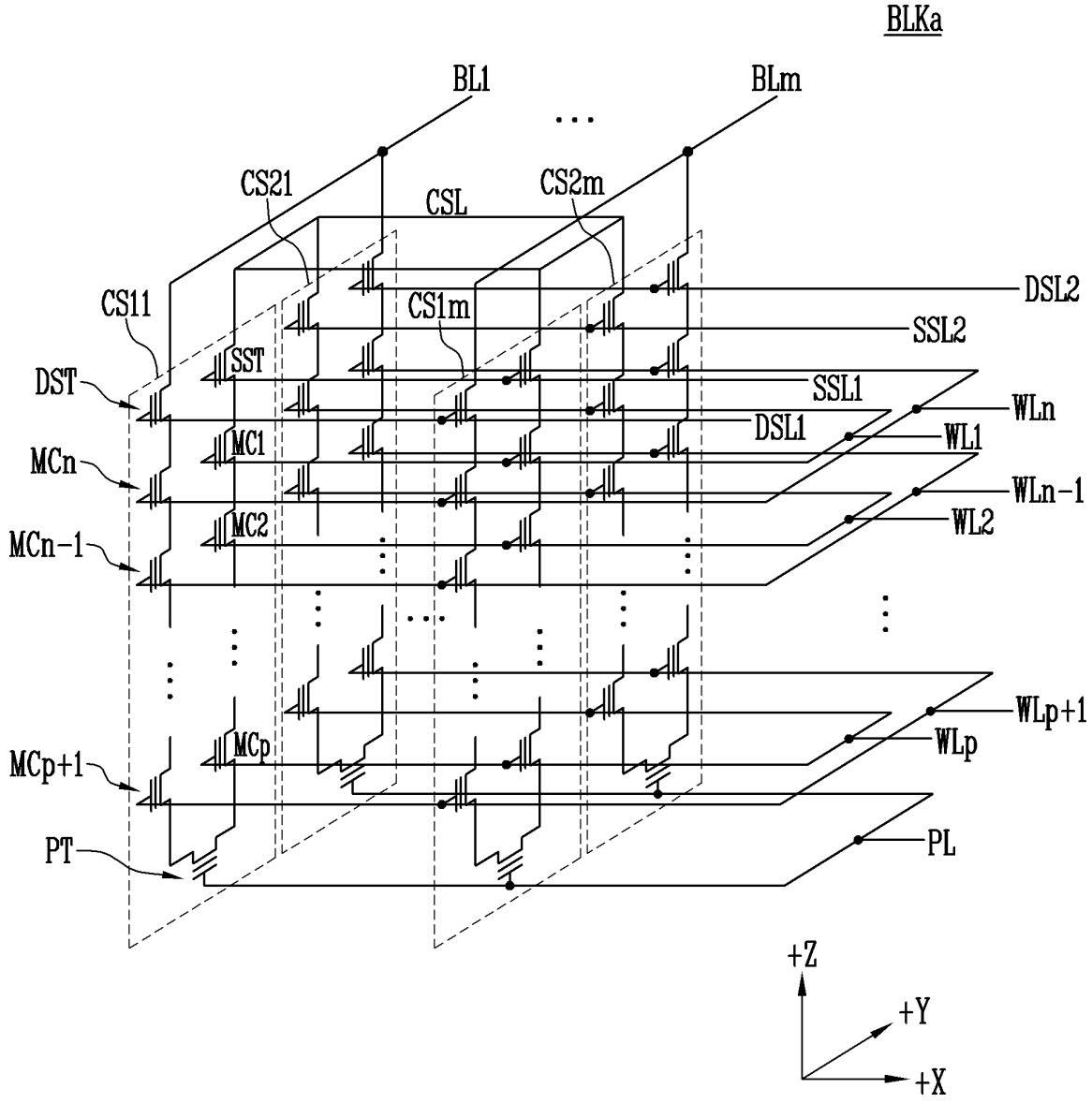

BLKa
BL1
BLm
CS21
CSL
CS2m
CS11
CS1m
DSL2
SSL2
SST
DST
SSL1
WLn
DSL1
WL1
MCn
MC1
WLn-1
MC2
WL2
MCn-1
WLp+1
MCp
WLp
MCp+1
PT
PL
+Z
+Y
+X

FIG. 5

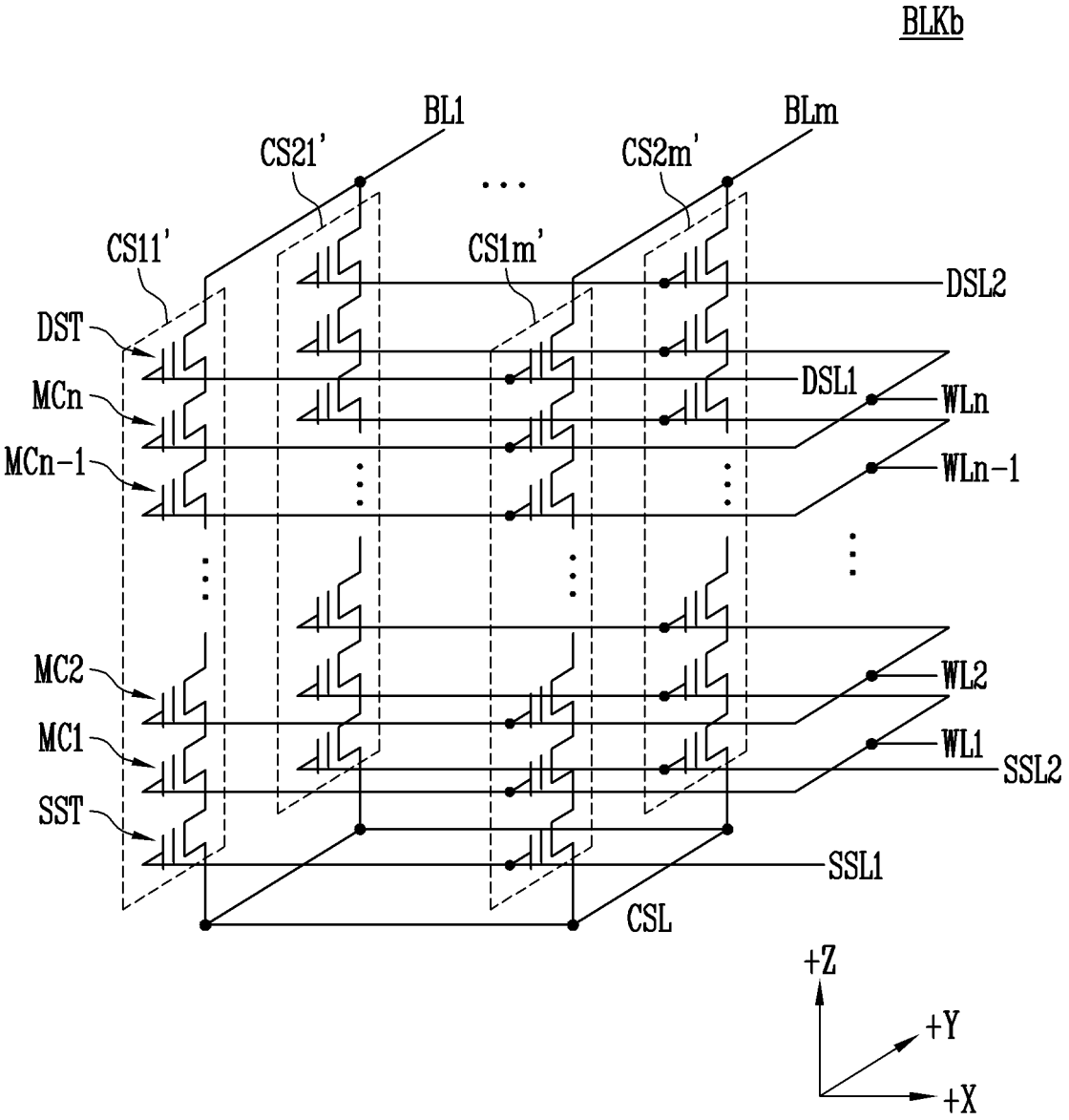

BLKb
BL1
BLm
CS21'
CS2m'
CS11'
CS1m'
DSL2
DST
DSL1
MCn
WLn
MCn-1
WLn-1
MC2
WL2
MC1
WL1
SSL2
SST
SSL1
CSL
+Z
+Y
+X

FIG. 6

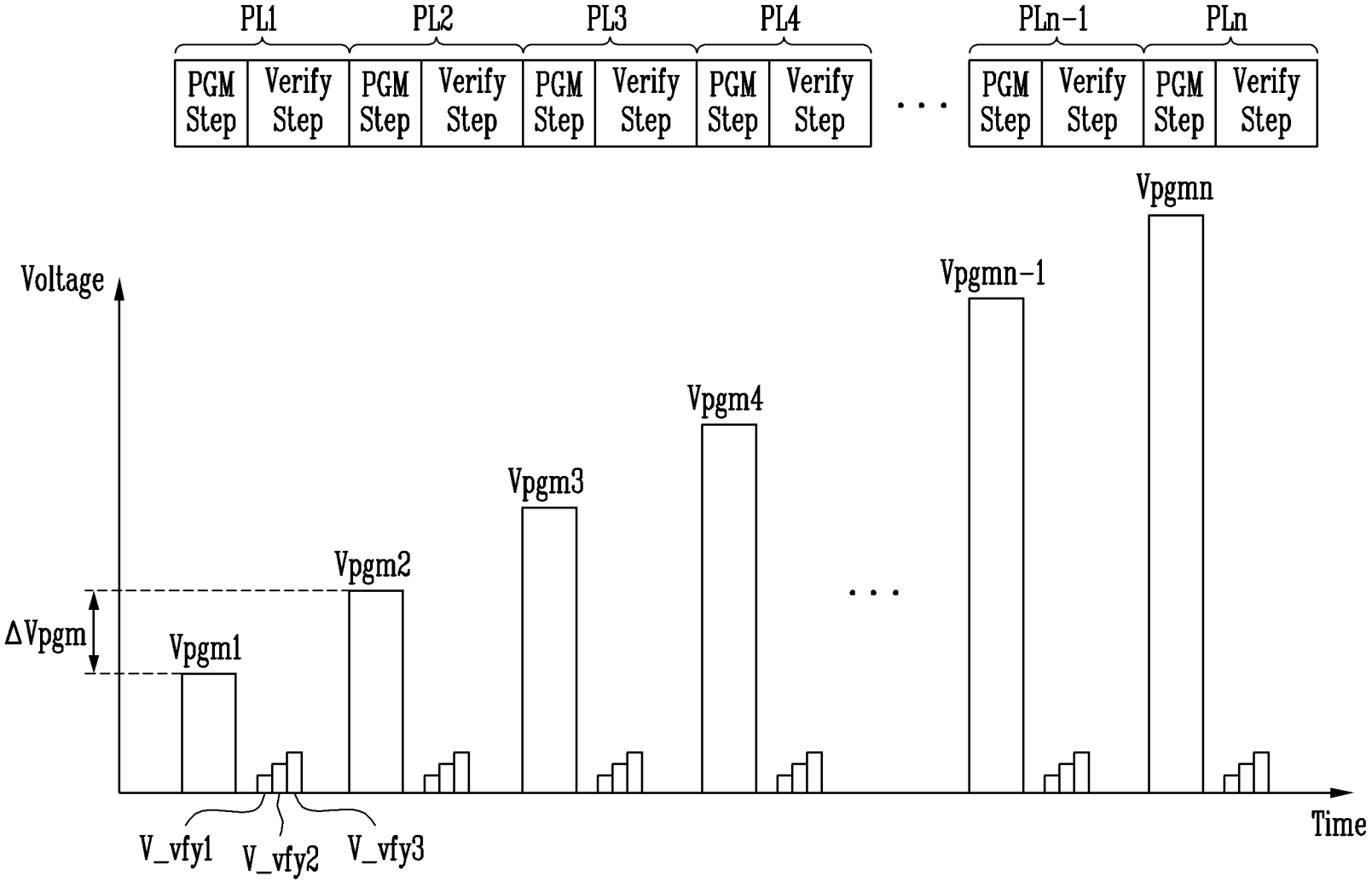

PL1
PL2
PL3
PL4
PLn-1
PLn
PGM Step
Verify Step
Voltage
Vpgm1
Vpgm2
Vpgm3
Vpgm4
Vpgmn-1
Vpgmn
ΔVpgm
V_vfy1
V_vfy2
V_vfy3
Time

FIG. 7

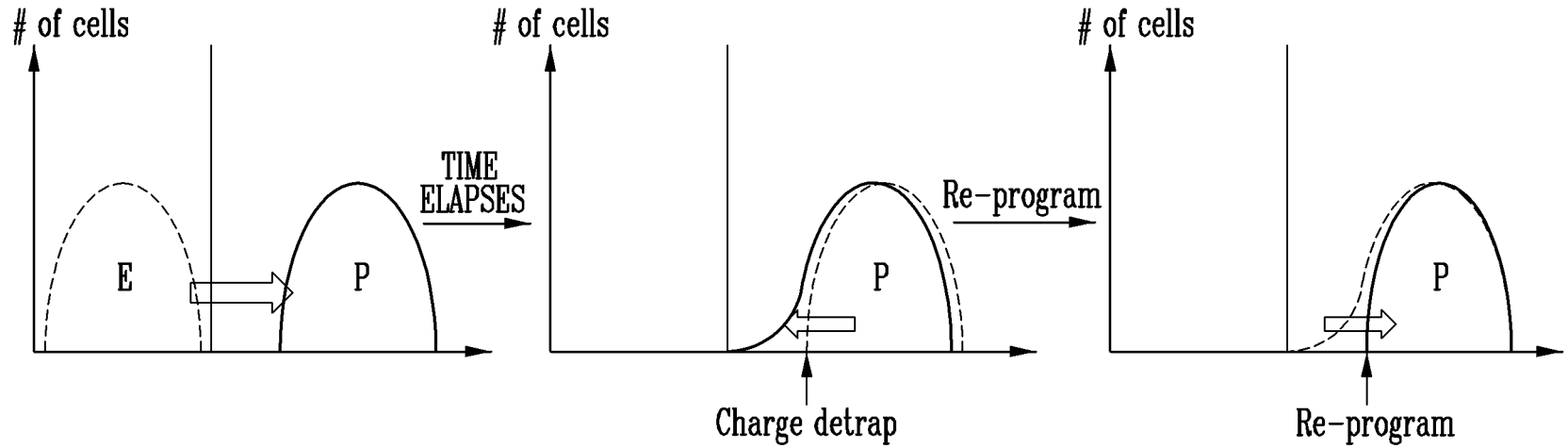

# of cells
E
P
TIME
ELAPSES
# of cells
P
Charge detrap
Re-program
# of cells
P
Re-program

FIG. 8

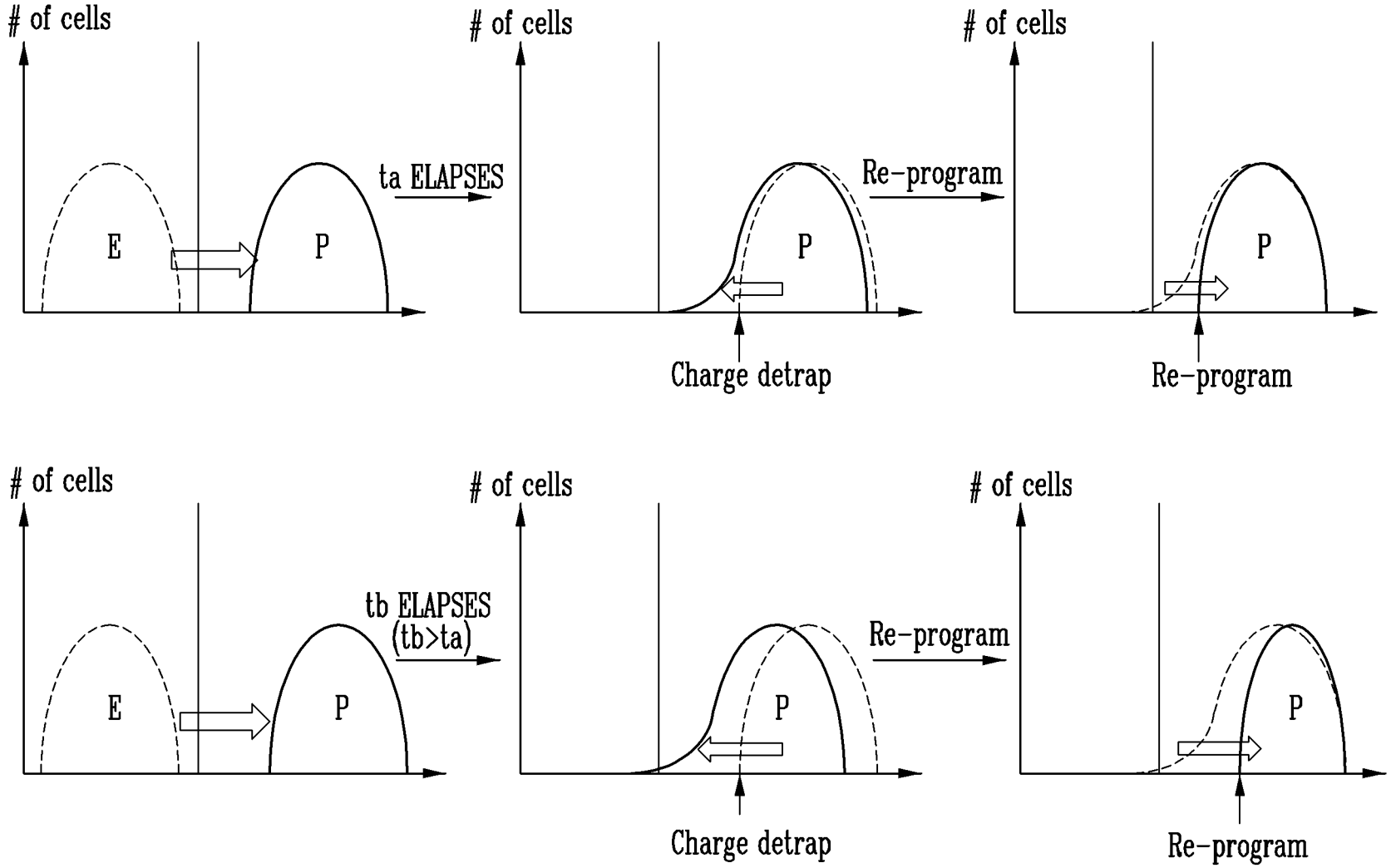

# of cells
E
P
ta ELAPSES
# of cells
P
Charge detrap
Re-program
# of cells
P
Re-program
# of cells
E
P
tb ELAPSES
(tb>ta)
# of cells
P
Charge detrap
Re-program
# of cells
P
Re-program

FIG. 9

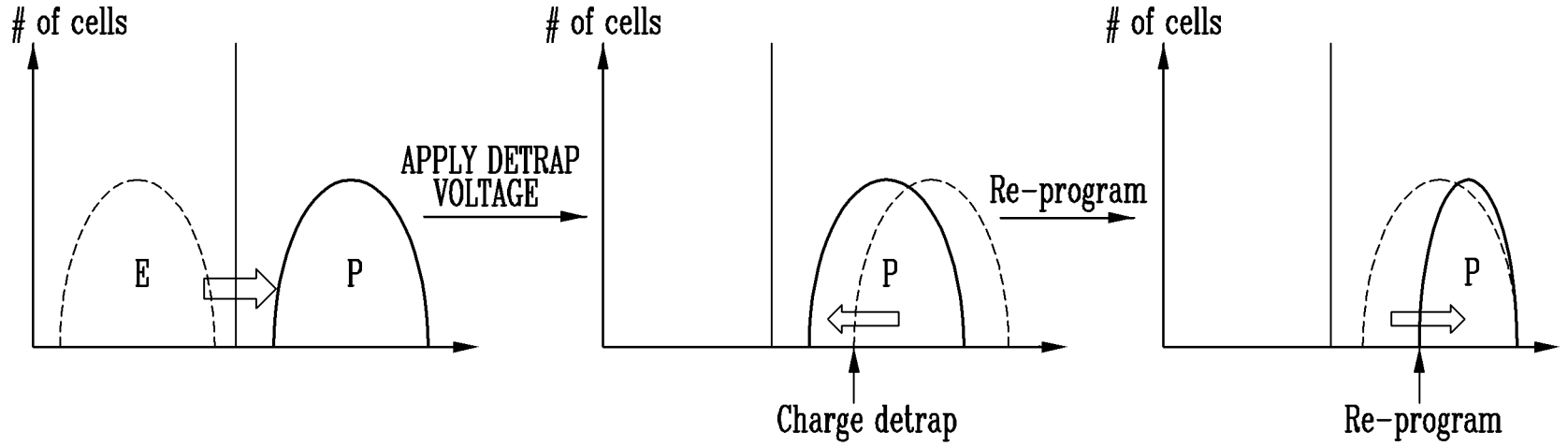

# of cells
E
P
APPLY DETRAP VOLTAGE
# of cells
P
Charge detrap
Re-program
# of cells
P
Re-program

FIG. 10

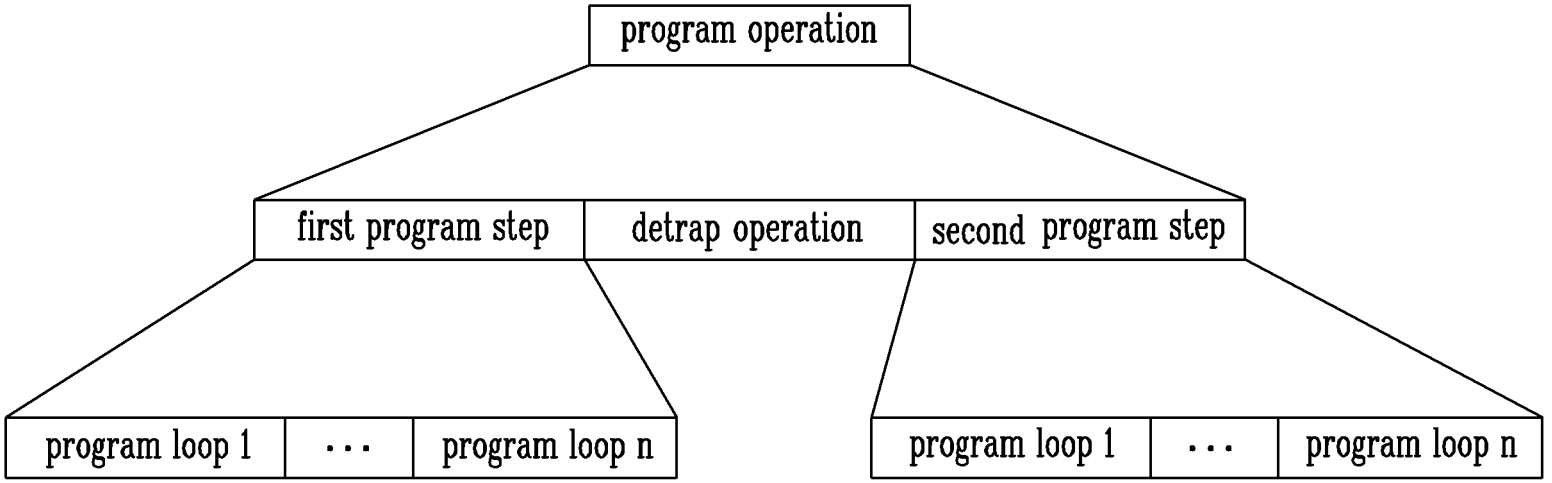

program operation
first program step
detrap operation
second program step
program loop 1
· · ·
program loop n
program loop 1
· · ·
program loop n

FIG. 11

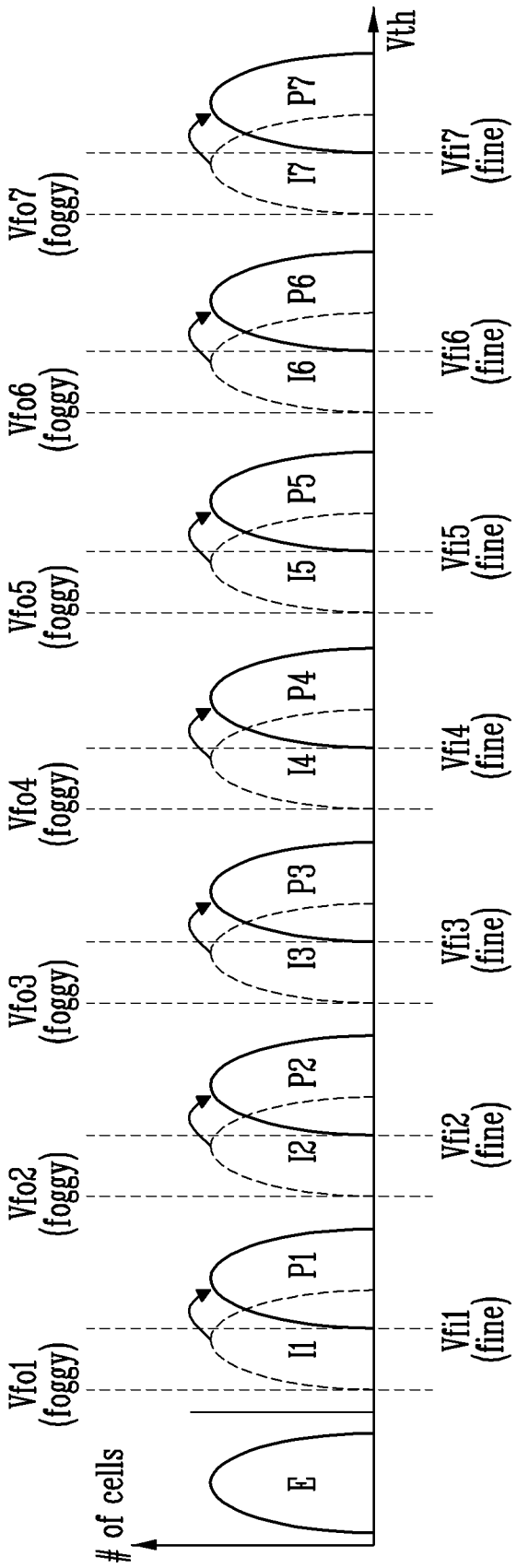

Vth
# of cells
E
I1
P1
I2
P2
I3
P3
I4
P4
I5
P5
I6
P6
I7
P7
Vfo1 (foggy)
Vfo2 (foggy)
Vfo3 (foggy)
Vfo4 (foggy)
Vfo5 (foggy)
Vfo6 (foggy)
Vfo7 (foggy)
Vfi1 (fine)
Vfi2 (fine)
Vfi3 (fine)
Vfi4 (fine)
Vfi5 (fine)
Vfi6 (fine)
Vfi7 (fine)

FIG. 12

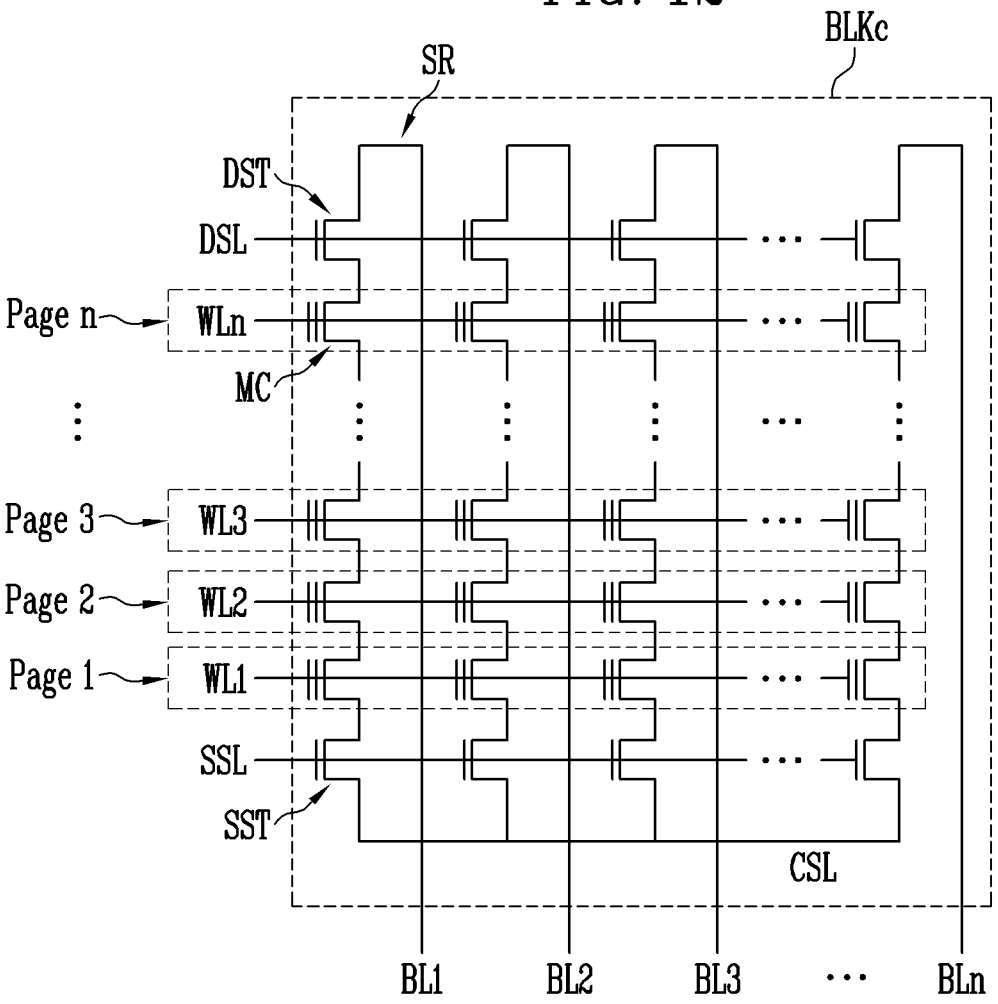

BLKc
SR
DST
DSL
Page n
WLn
MC
Page 3
WL3
Page 2
WL2
Page 1
WL1
SSL
SST
CSL
BL1
BL2
BL3
BLn

FIG. 13

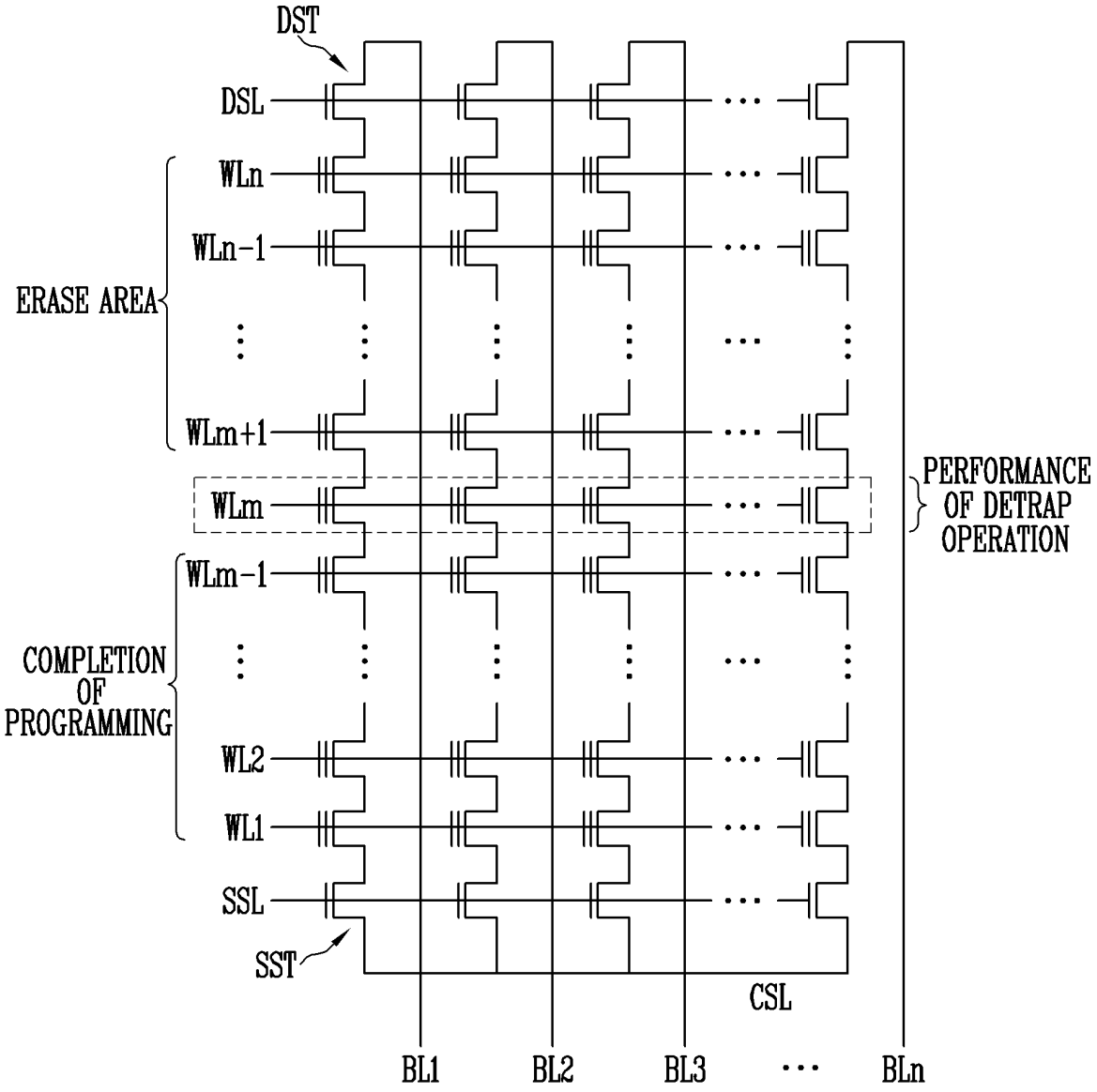

DST
DSL
WLn
WLn-1
ERASE AREA
WLm+1
WLm
PERFORMANCE OF DETRAP OPERATION
WLm-1
COMPLETION OF PROGRAMMING
WL2
WL1
SSL
SST
CSL
BL1
BL2
BL3
BLn

FIG. 14

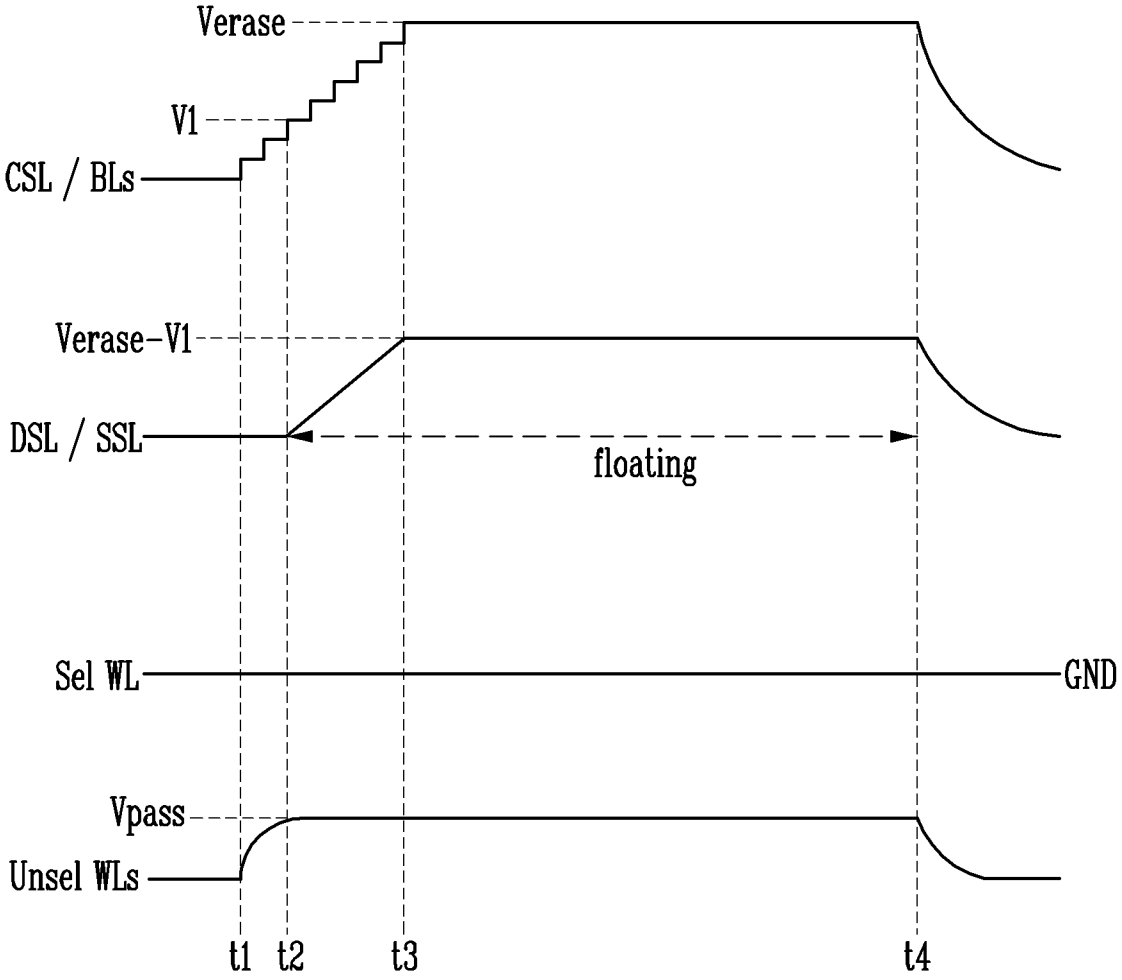

Verase
V1
CSL / BLs
Verase-V1
DSL / SSL
floating
Sel WL
GND
Vpass
Unsel WLs
t1
t2
t3
t4

FIG. 15

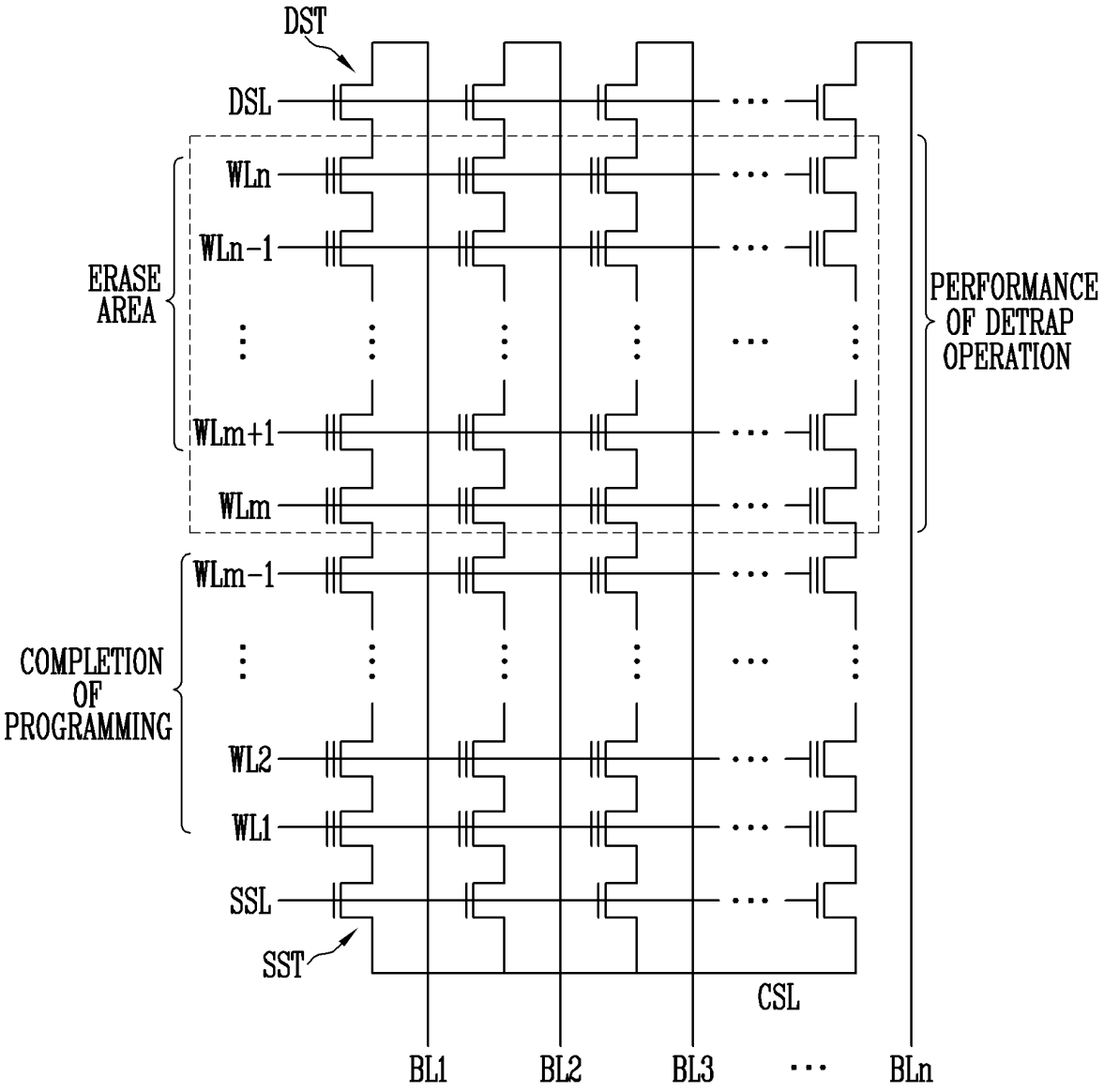

DST
DSL
WLn
WLn-1
ERASE AREA
WLm+1
WLm
WLm-1
COMPLETION OF PROGRAMMING
WL2
WL1
SSL
SST
CSL
PERFORMANCE OF DETRAP OPERATION
BL1
BL2
BL3
BLn

FIG. 16

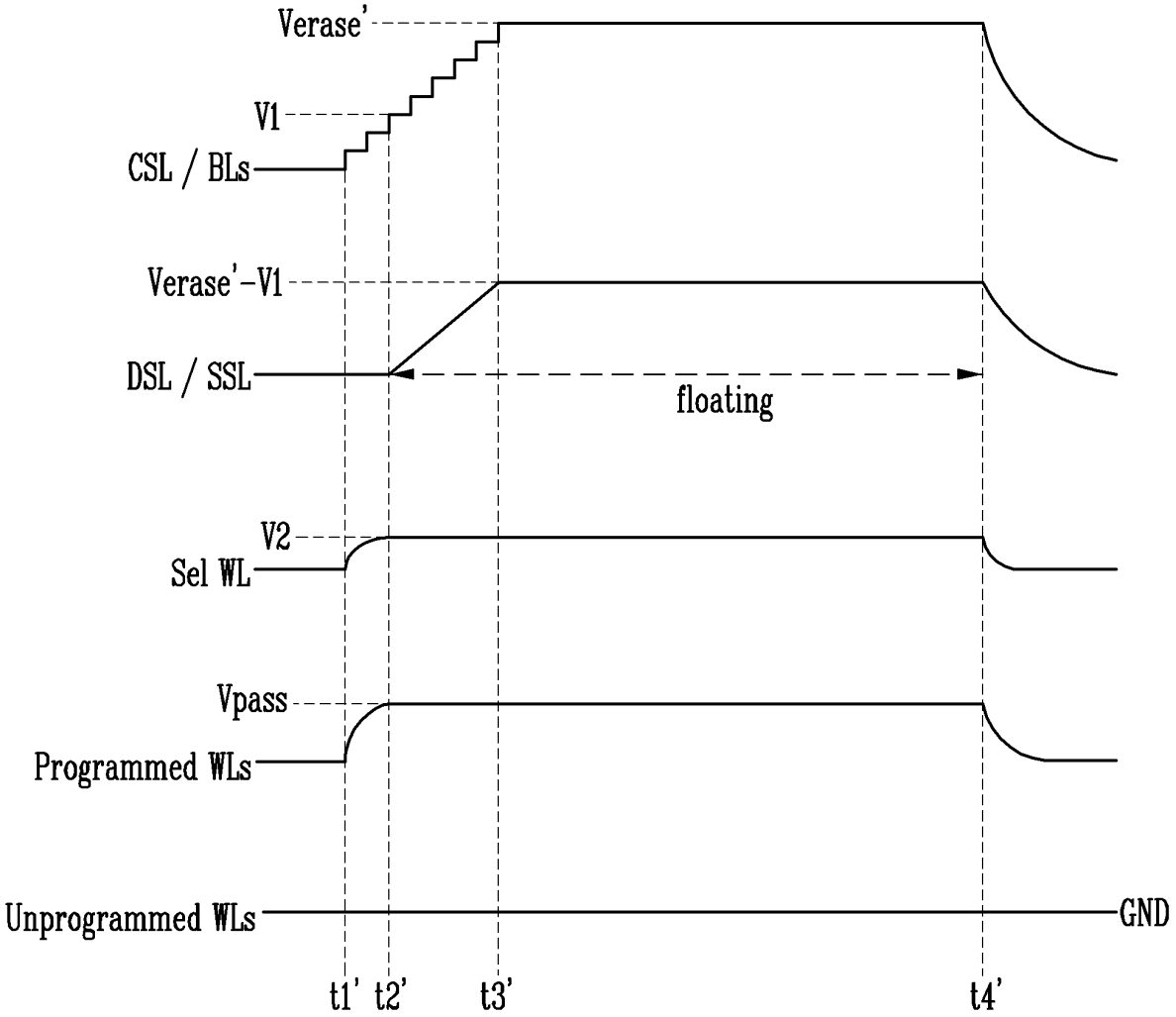

Verase'
V1
CSL / BLs
Verase'-V1
DSL / SSL
floating
V2
Sel WL
Vpass
Programmed WLs
Unprogrammed WLs
GND
t1'
t2'
t3'
t4'

FIG. 17

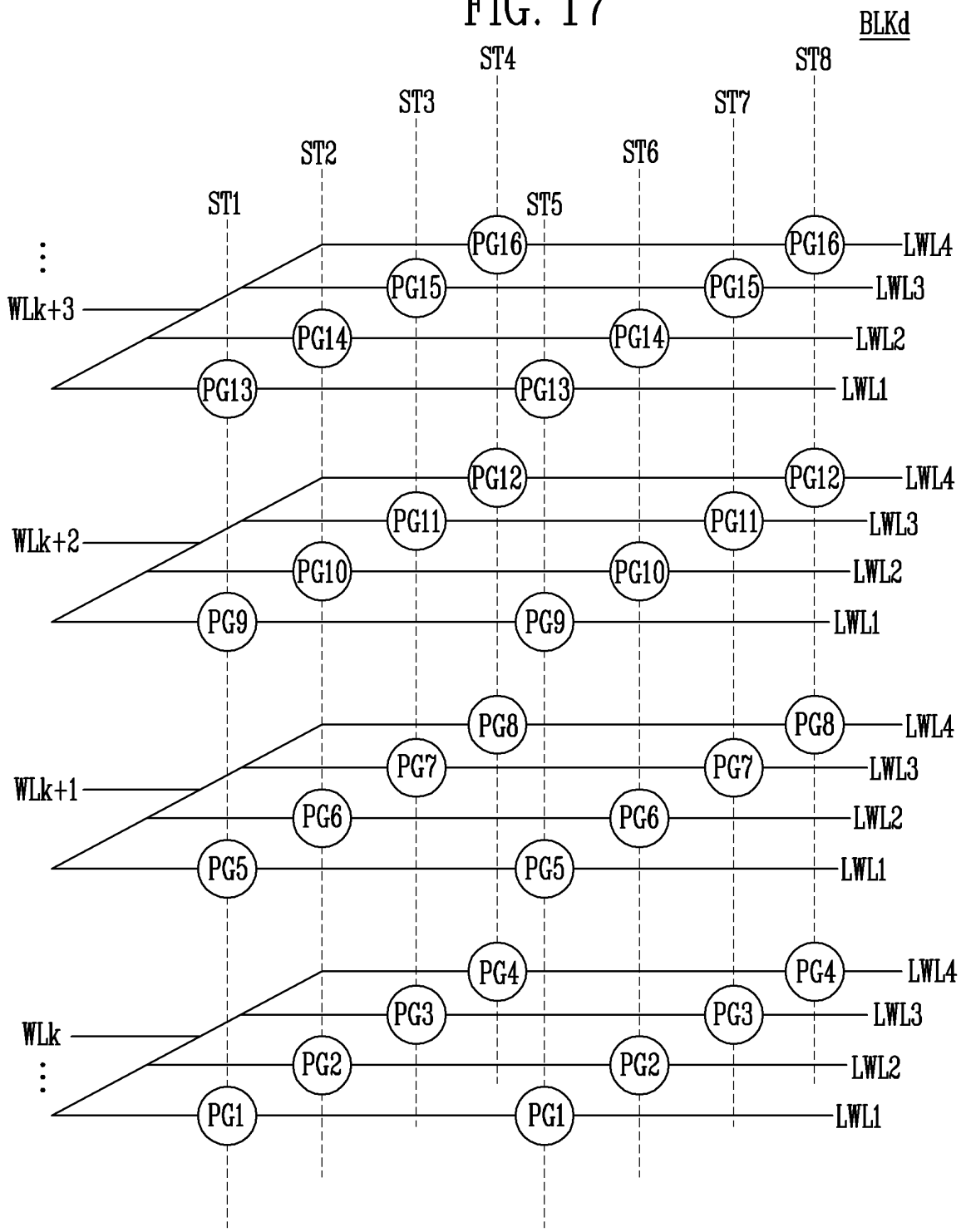

BLKd
ST1
ST2
ST3
ST4
ST5
ST6
ST7
ST8
WLk+3
WLk+2
WLk+1
WLk
PG16
PG15
PG14
PG13
PG12
PG11
PG10
PG9
PG8
PG7
PG6
PG5
PG4
PG3
PG2
PG1
LWL4
LWL3
LWL2
LWL1

FIG. 18

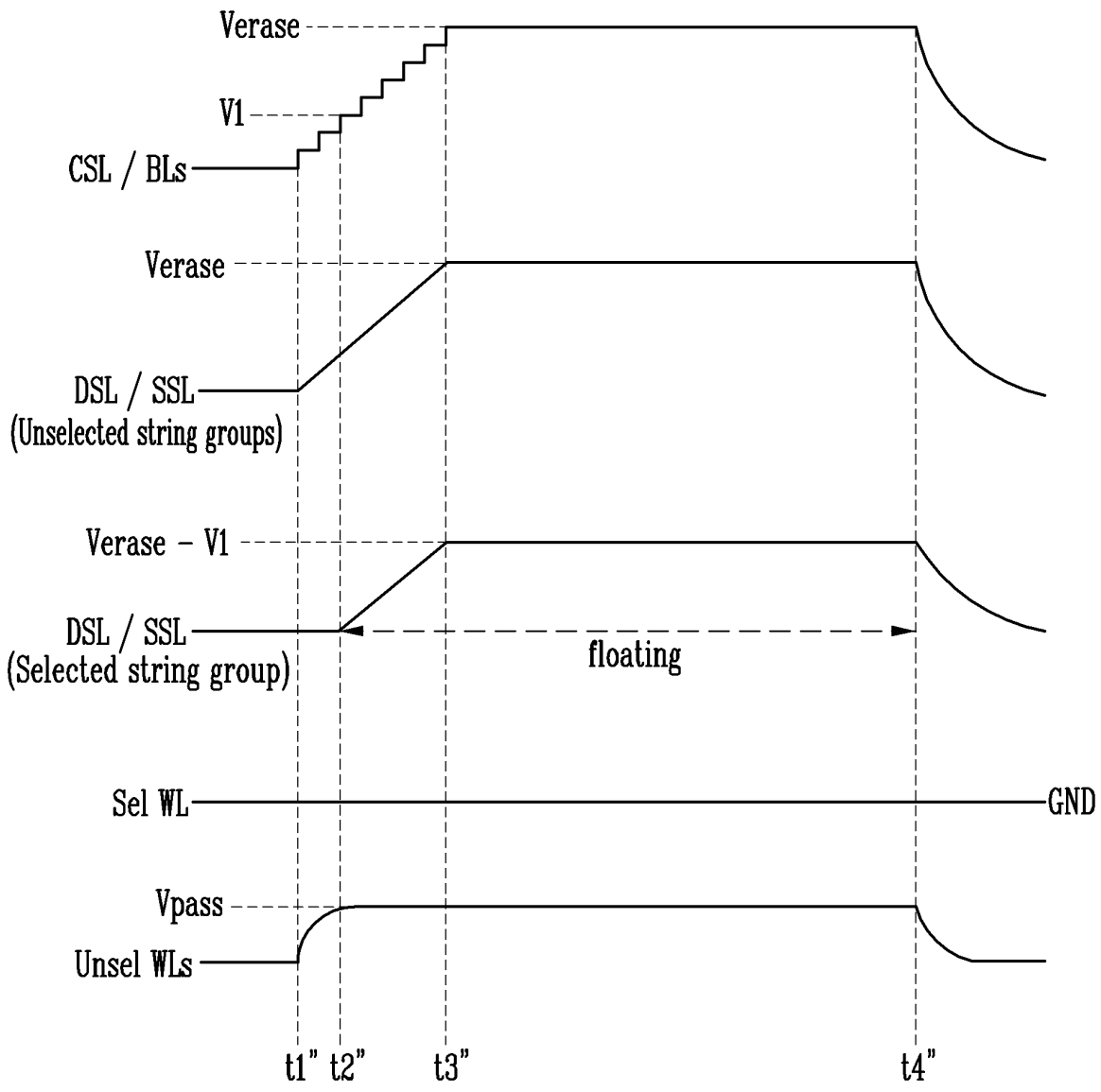

Verase
V1
CSL / BLs
Verase
DSL / SSL
(Unselected string groups)
Verase - V1
DSL / SSL
(Selected string group)
floating
Sel WL
GND
Vpass
Unsel WLs
t1"
t2"
t3"
t4"

FIG. 19

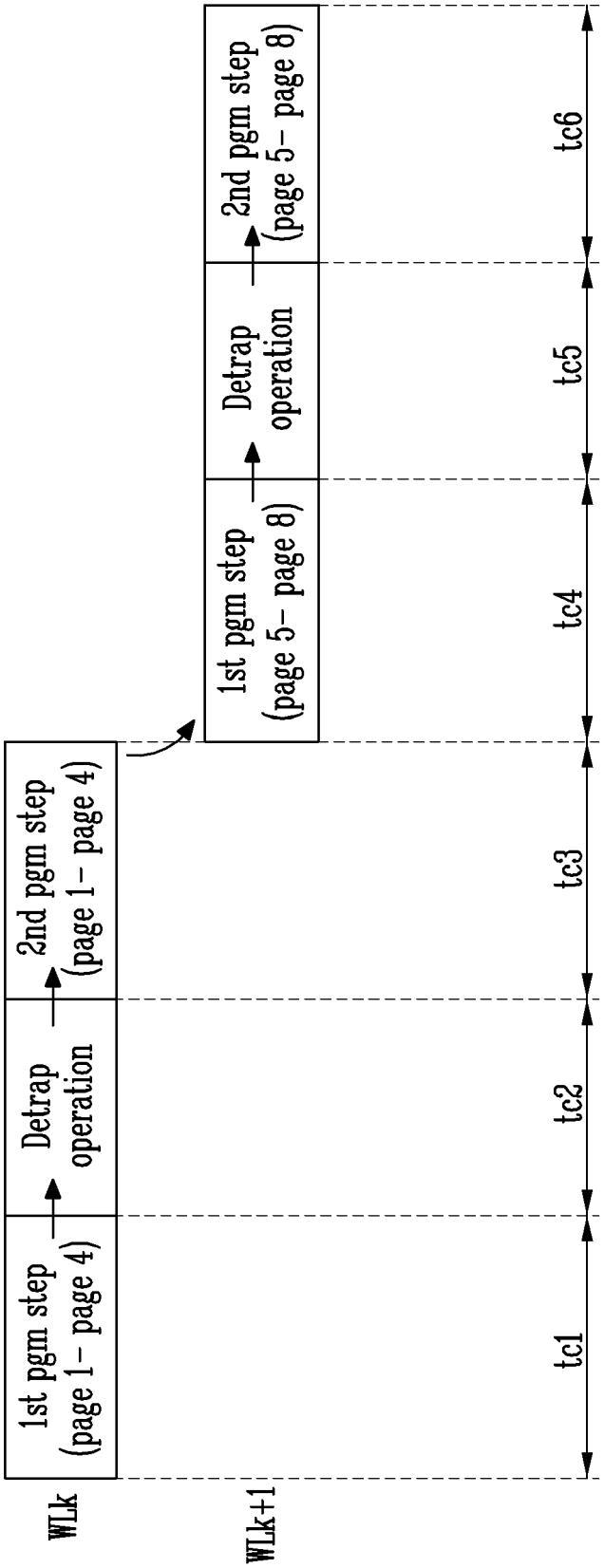

WLk
WLk+1
1st pgm step (page 1– page 4)
Detrap operation
2nd pgm step (page 1– page 4)
1st pgm step (page 5– page 8)
Detrap operation
2nd pgm step (page 5– page 8)
tc1
tc2
tc3
tc4
tc5
tc6

FIG. 20

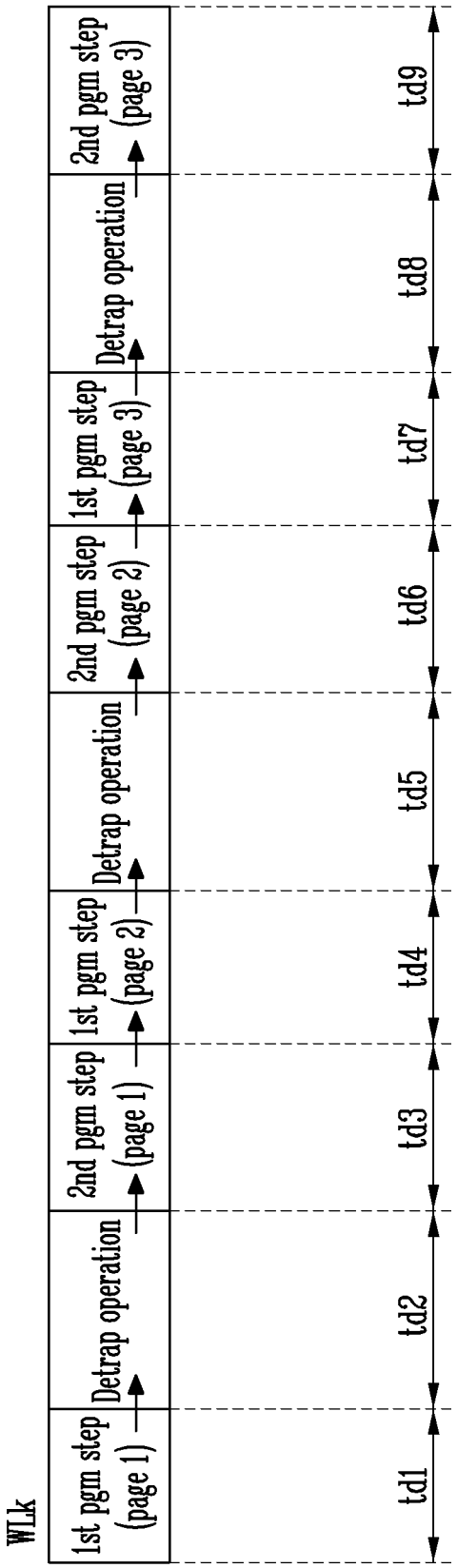

WLk
1st pgm step (page 1)
Detrap operation
2nd pgm step (page 1)
1st pgm step (page 2)
Detrap operation
2nd pgm step (page 2)
1st pgm step (page 3)
Detrap operation
2nd pgm step (page 3)
td1
td2
td3
td4
td5
td6
td7
td8
td9

FIG. 21

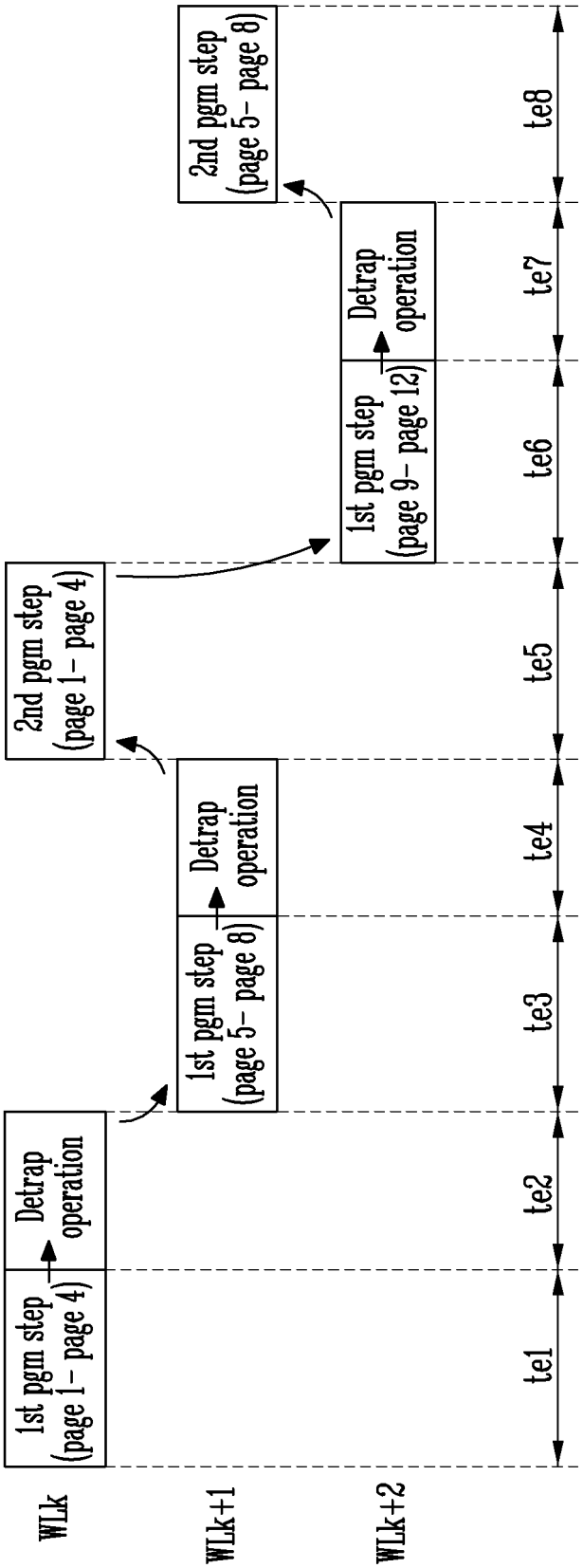

WLk
WLk+1
WLk+2
1st pgm step (page 1– page 4)
Detrap operation
1st pgm step (page 5– page 8)
Detrap operation
2nd pgm step (page 1– page 4)
1st pgm step (page 9– page 12)
Detrap operation
2nd pgm step (page 5– page 8)
te1
te2
te3
te4
te5
te6
te7
te8

FIG. 22

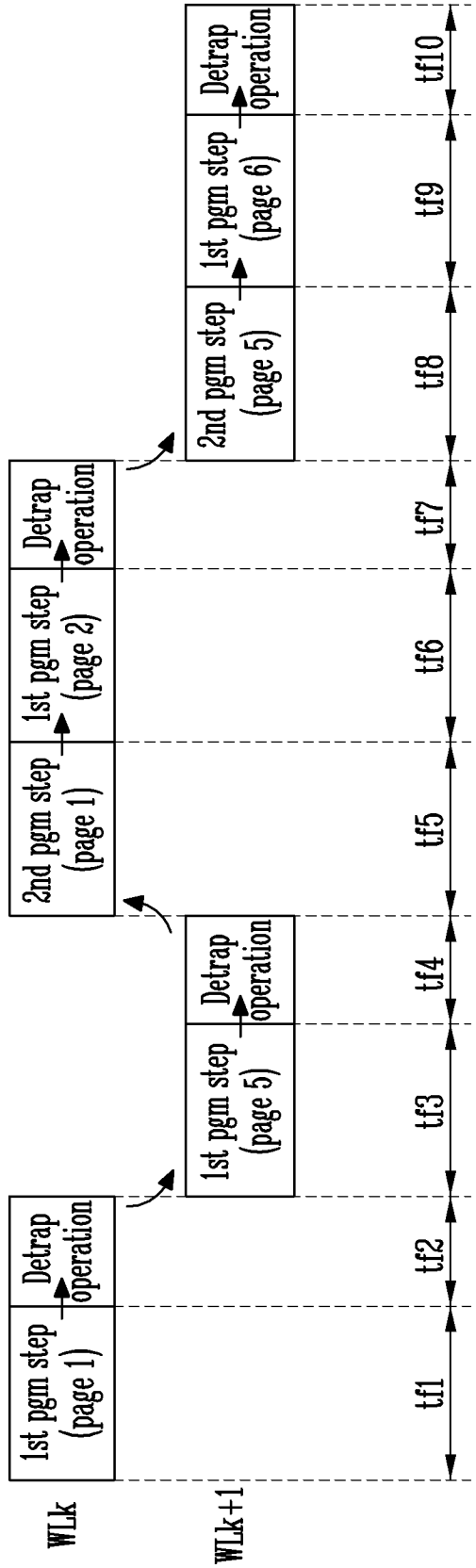

WLk
WLk+1
1st pgm step (page 1)
Detrap operation
1st pgm step (page 5)
Detrap operation
2nd pgm step (page 1)
1st pgm step (page 2)
Detrap operation
2nd pgm step (page 5)
1st pgm step (page 6)
Detrap operation
tf1
tf2
tf3
tf4
tf5
tf6
tf7
tf8
tf9
tf10

FIG. 23

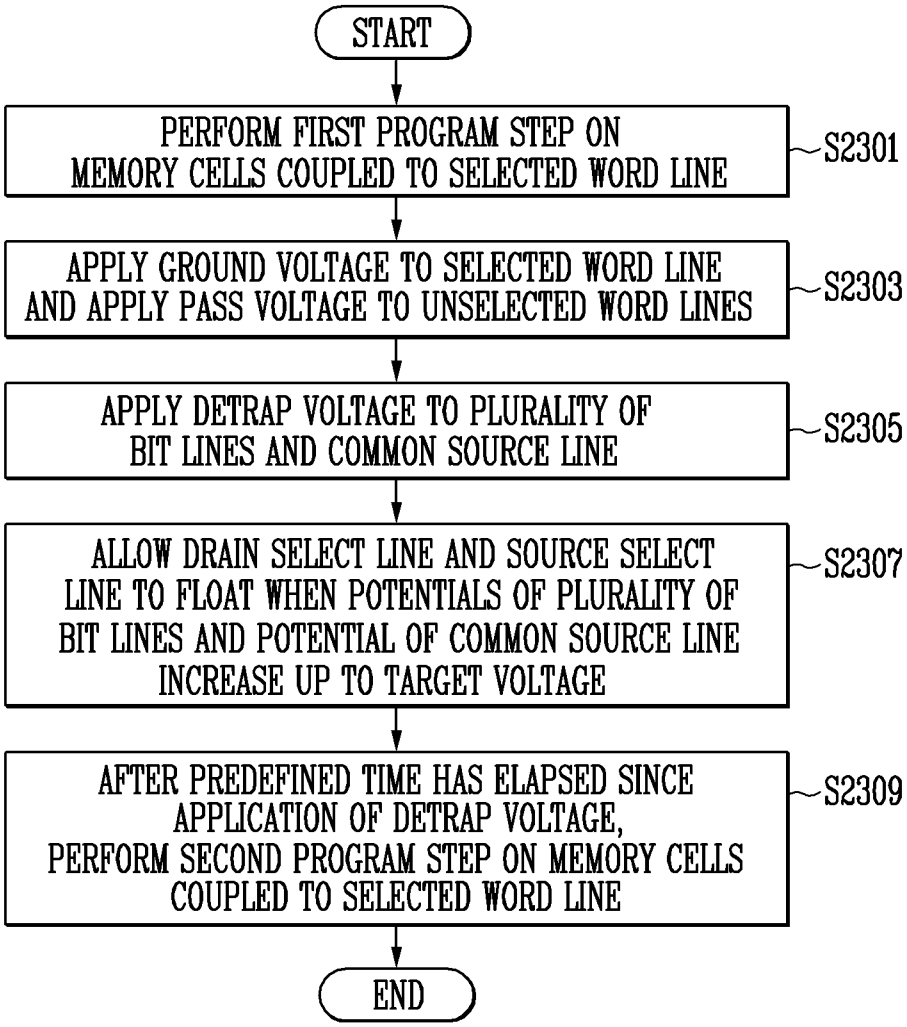

START
PERFORM FIRST PROGRAM STEP ON MEMORY CELLS COUPLED TO SELECTED WORD LINE
S2301
APPLY GROUND VOLTAGE TO SELECTED WORD LINE AND APPLY PASS VOLTAGE TO UNSELECTED WORD LINES
S2303
APPLY DETRAP VOLTAGE TO PLURALITY OF BIT LINES AND COMMON SOURCE LINE
S2305
ALLOW DRAIN SELECT LINE AND SOURCE SELECT LINE TO FLOAT WHEN POTENTIALS OF PLURALITY OF BIT LINES AND POTENTIAL OF COMMON SOURCE LINE INCREASE UP TO TARGET VOLTAGE
S2307
AFTER PREDEFINED TIME HAS ELAPSED SINCE APPLICATION OF DETRAP VOLTAGE, PERFORM SECOND PROGRAM STEP ON MEMORY CELLS COUPLED TO SELECTED WORD LINE
S2309
END

FIG. 24

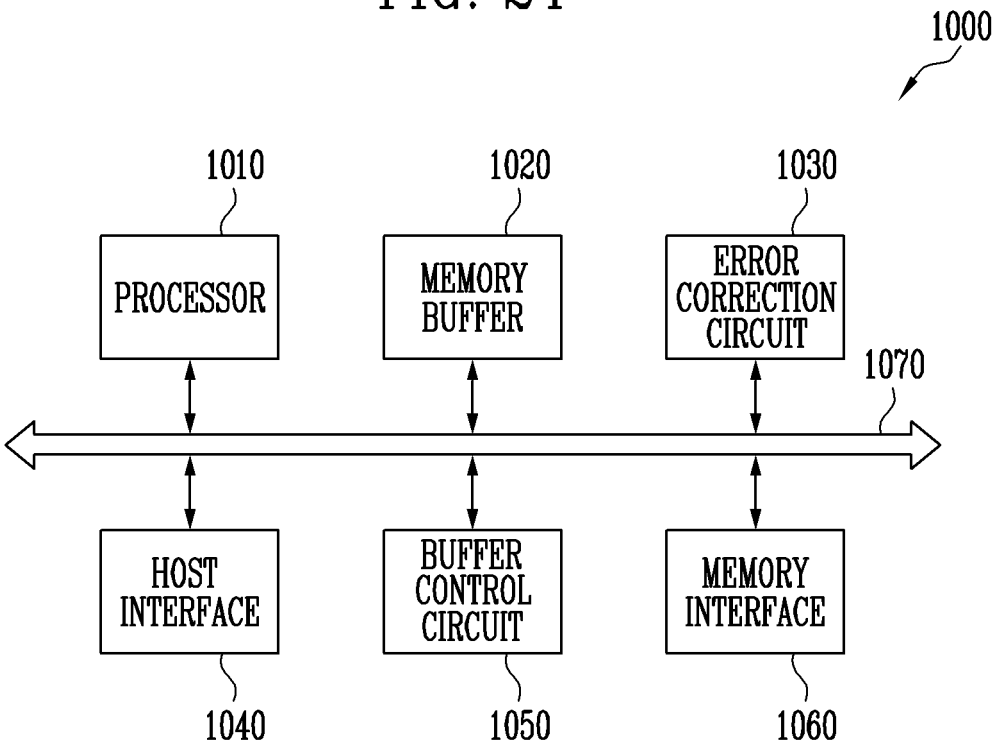

1000
1010
1020
1030
PROCESSOR
MEMORY BUFFER
ERROR CORRECTION CIRCUIT
1070
HOST INTERFACE
BUFFER CONTROL CIRCUIT
MEMORY INTERFACE
1040
1050
1060

FIG. 25

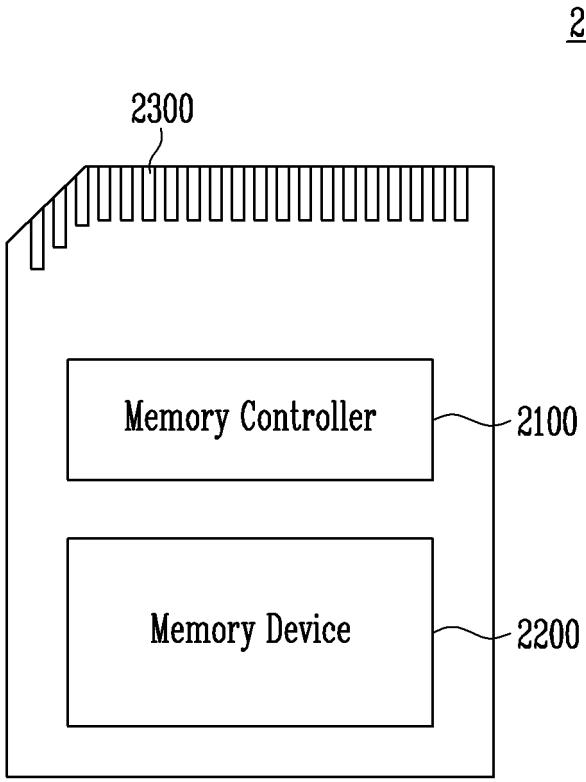


FIG. 26

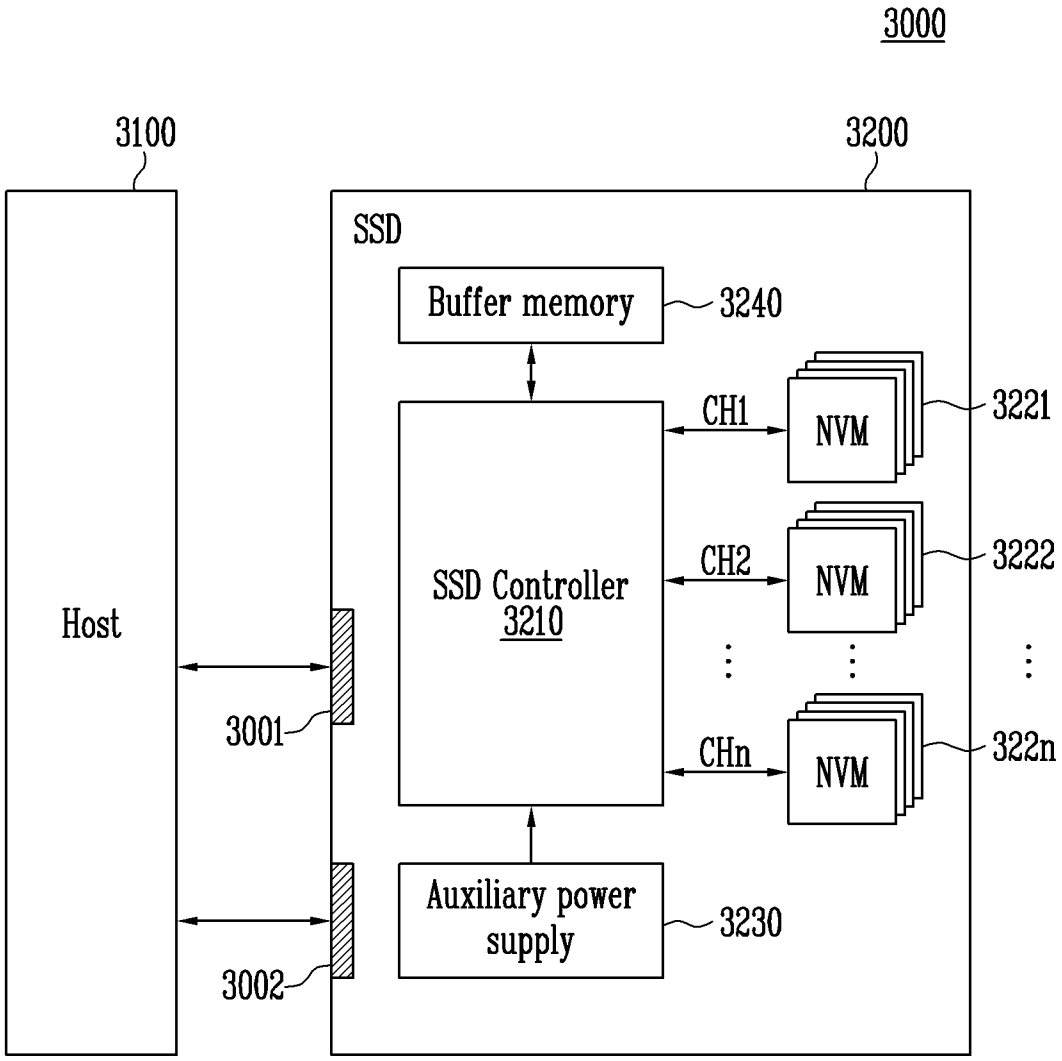
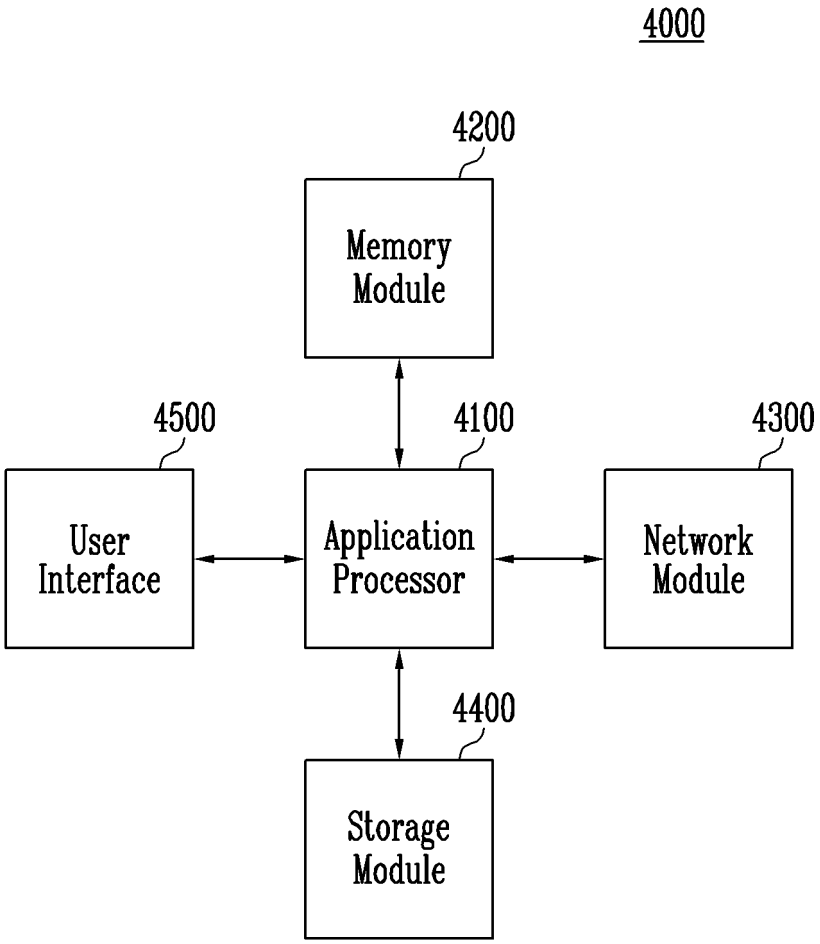

3000
3100
3200
Host
SSD
Buffer memory
3240
SSD Controller
3210
CH1
CH2
CHn
NVM
NVM
NVM
3221
3222
322n
3001
3002
Auxiliary power supply
3230

FIG. 27


4000
4200
Memory Module
4500
4100
4300
User Interface
Application Processor
Network Module
4400
Storage Module