FIG. 1

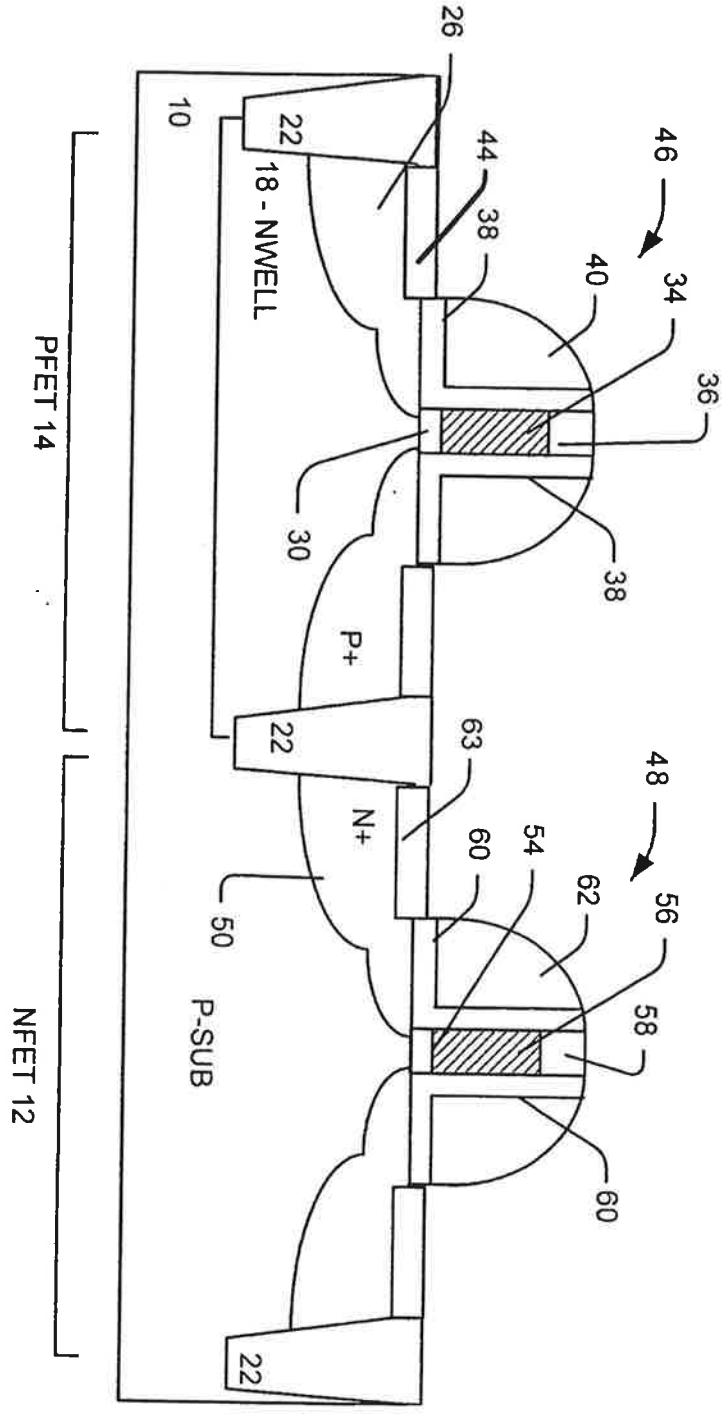

26
10
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18 - NWELL
44
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36
30
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P+
22
63
48
N+
60
54
62
56
50
58
P-SUB
60
22
PFET 14
NFET 12

FIG. 2

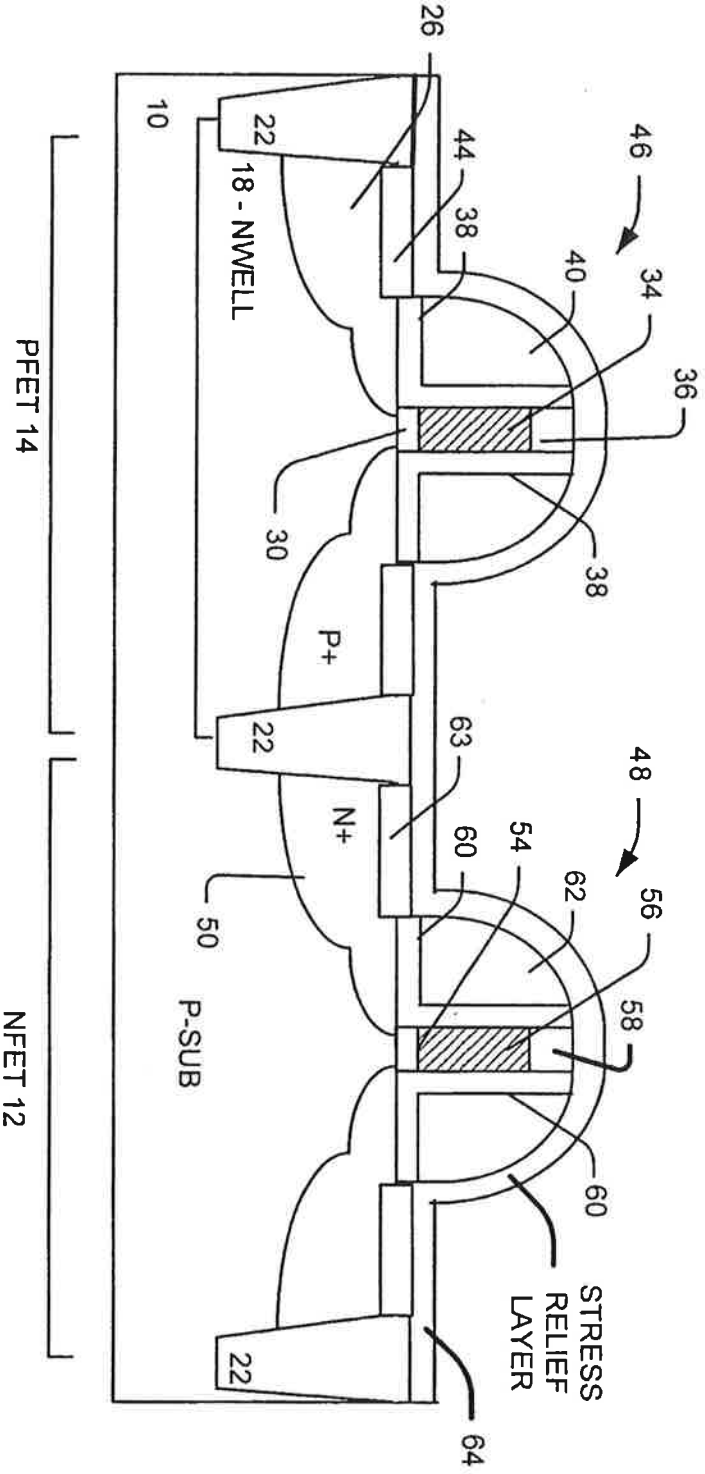

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P+
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N+
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62
56
50
58
P-SUB
60
STRESS
RELIEF
LAYER
22
64
PFET 14
NFET 12

FIG. 3

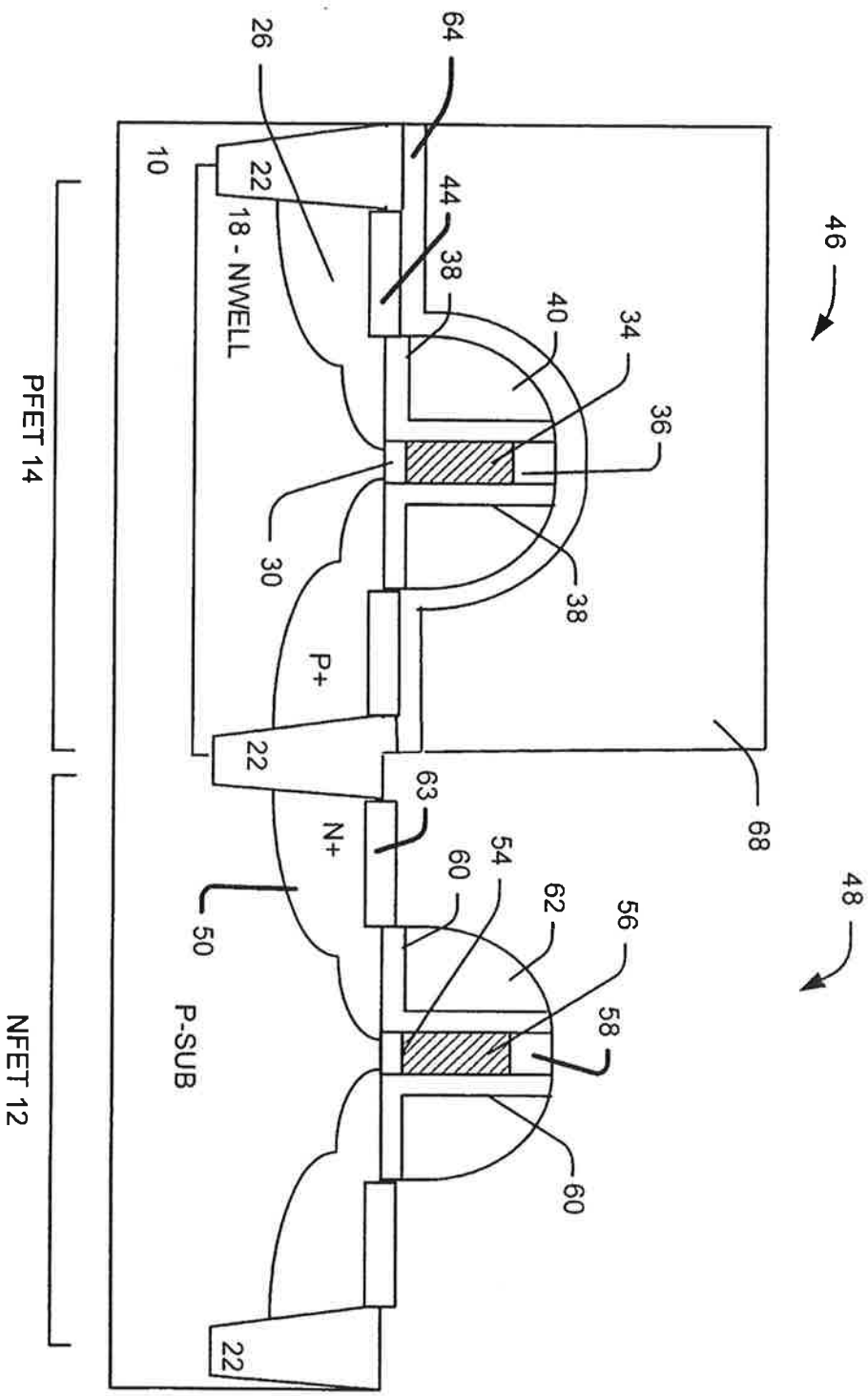
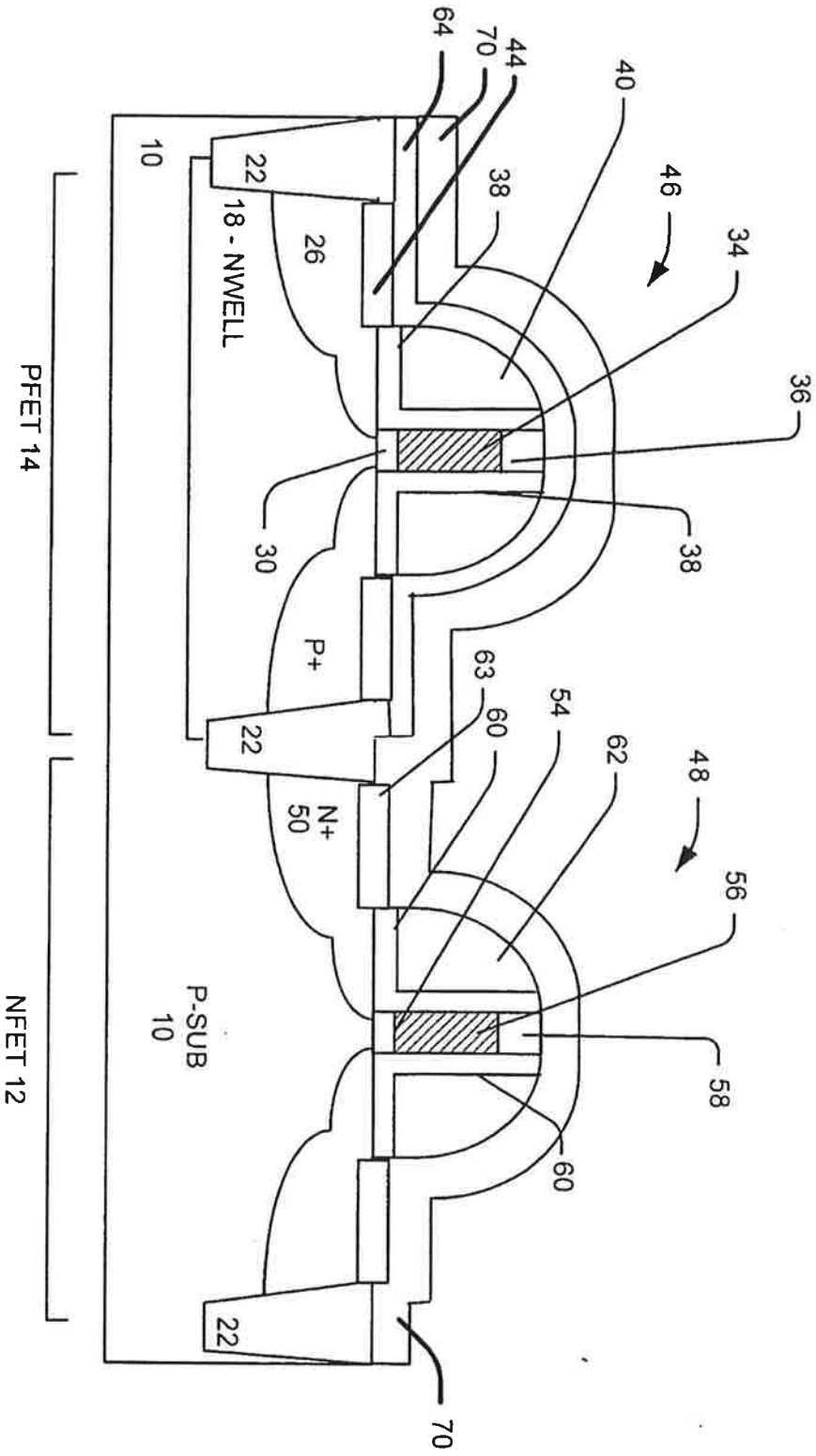

64
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18 - NWELL
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P+
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N+
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P-SUB
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22
68
46
48
PFET 14
NFET 12

FIG. 4


64
70
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18 - NWELL
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38
P+
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22
N+
50
56
58
60
P-SUB
10
PFET 14
NFET 12
22
70

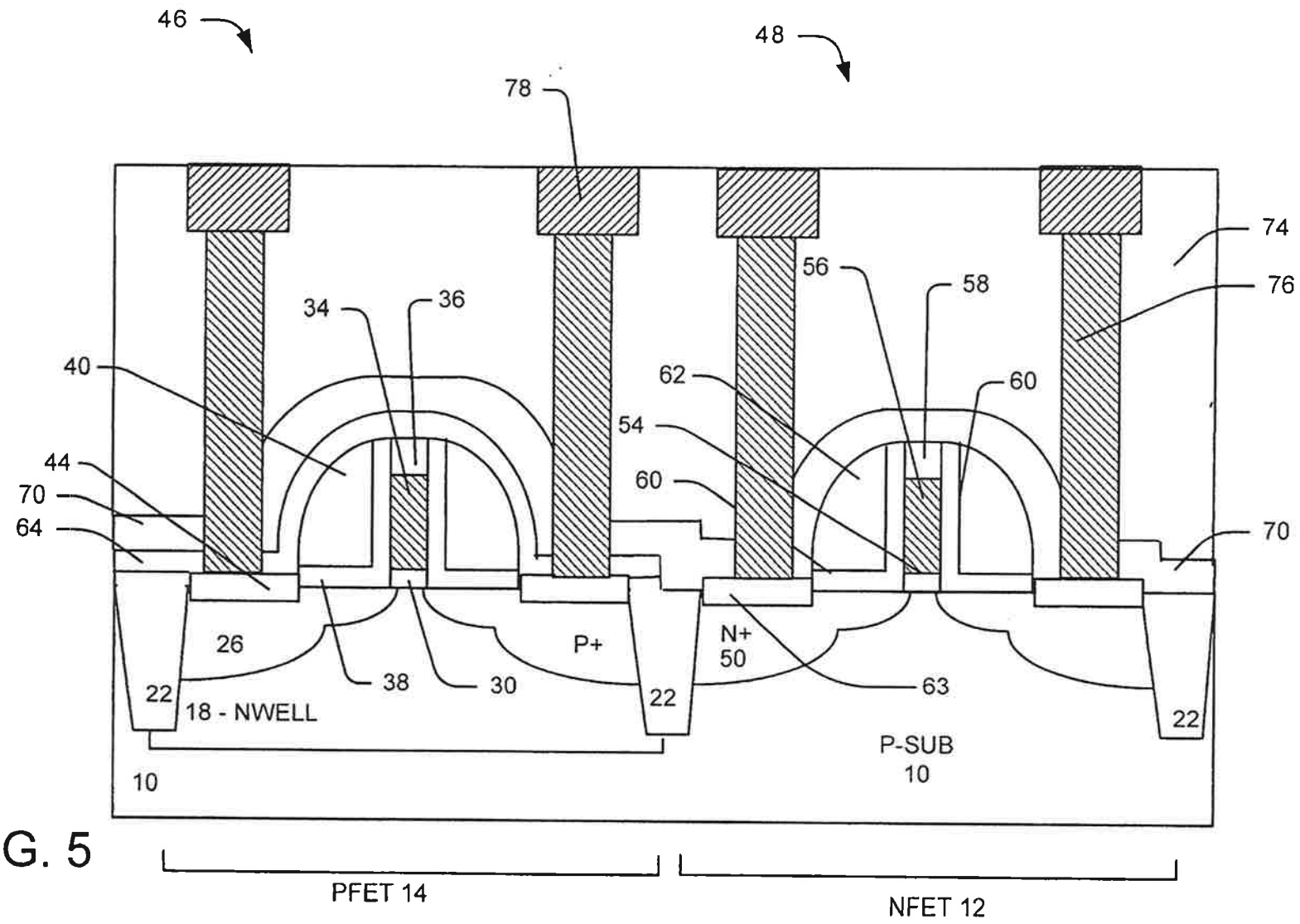

46
48
78
74
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76
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36
40
62
60
54
44
60
70
64
70
26
P+
N+
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38
30
63
22
18 - NWELL
22
22
P-SUB
10
10
PFET 14
NFET 12

FIG. 5

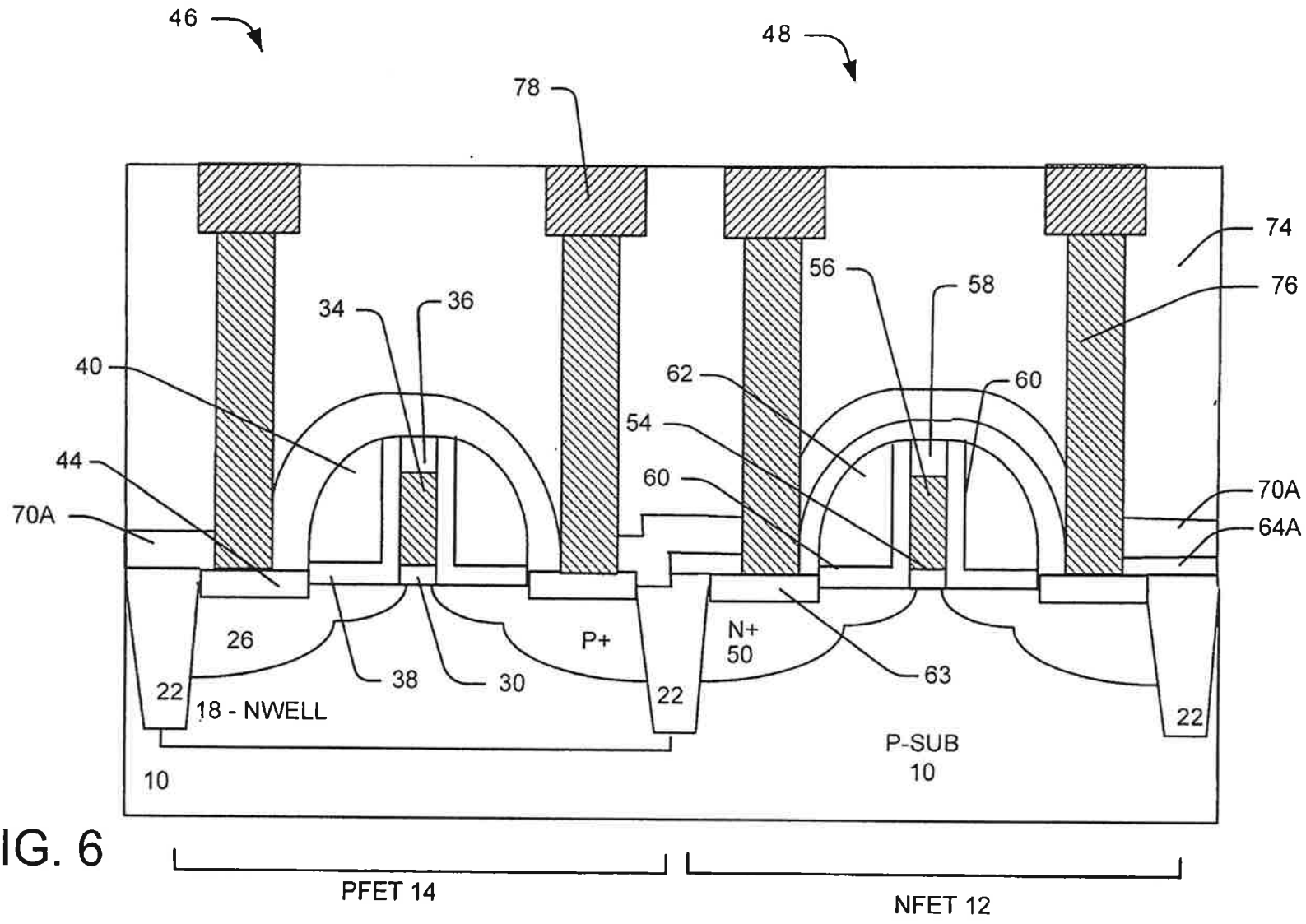

46
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36
40
62
60
54
44
60
70A
70A
64A
26
P+
N+
50
38
30
63
22
22
22
18 - NWELL
P-SUB
10
10
PFET 14
NFET 12

FIG. 6