

ABSTRACT

LOW VOLTAGE PROGRAMMABLE AND ERASABLE FLASH EEPROM

a new method of fabricating and programming and erasing a Flash EEPROM memory cell is achieved. A semiconductor substrate is provided. A tunneling oxide layer is formed overlying said semiconductor substrate. A first polysilicon layer is deposited overlying the tunneling oxide layer. An interpoly oxide layer is deposited overlying the first polysilicon layer. A second polysilicon layer is deposited overlying the interpoly oxide layer. The second polysilicon layer, the interpoly oxide layer, the first polysilicon layer, and the tunneling oxide layer are patterned to form control gates and floating gates for planned Flash EEPROM memory cells. Ions are implanted to form drain junctions for planned Flash EEPROM memory cells in the semiconductor substrate where the drain junctions are shallow and abrupt. Ions are implanted to form angled pocket junctions adjacent to the drain junctions. The angled pocket junctions are implanted at a non-perpendicular angle with respect to the semiconductor substrate and are counter-doped to the drain junctions. Ions are implanted to form source junctions where the junctions are deeper and less abrupt than the drain junctions to complete the Flash EEPROM memory cells in the integrated circuit device.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)