What is claimed is:

1. A method for processing a digital bit stream representative of a communication signal, the method comprising:

dividing, at one or more processors, the digital bit stream into a plurality of data packets, each of the data packets of the plurality of data packets including an overlap of data from an adjacent packet;

in a first processing block in the processor,

performing a timing recovery operation on a first portion of the plurality of data packets, and

performing a carrier recovery operation on the first portion of the plurality of data packets;

in a second processing block in the processor in parallel with the first portion of the plurality of packets,

performing the timing recovery error calculation on a second portion of the plurality of data packets; and

performing the carrier recovery error calculation on the second portion of the plurality of data packets; and

combining the first portion and the second portion based on timing and phase stitching.

2. The method of claim 1, wherein the adjacent packets overlap in time by one percent of the length of the packets.

3. The method of claim 1, wherein the plurality of data packets have varying lengths.

4. The method of claim 1, wherein the timing recovery operation comprises determining phase offset information associated with in-phase and quadrature (I/Q) data of the first portion and the second portion.

5. The method of claim 1, wherein the timing recovery operation comprises:

receiving overlapping packets as samples of the downlink signal, the samples having an unknown symbol rate and frequency;

determining a timing error of the samples based on an estimate of the symbol rate;

decimating the samples by a decimation filter; and

determining a phase, frequency, and Doppler rate of the samples;

synchronizing the samples as symbols, based on the phase, frequency, and Doppler rate; and

updating the estimate of the symbol rate.

6. The method of claim 5, wherein the carrier recovery operation comprises:

receiving the symbols associated with the synchronized samples of the downlink signal;

determining a carrier error of the symbols based on an estimate of a frequency of the downlink signal and a product of the symbols raised to a power of n, wherein n is an integer;

decimating the symbols by a decimation filter; and

determining a phase, frequency, and Doppler rate of the symbols; and

updating the estimate of the frequency.

7. The method of claim 1, wherein the carrier recovery is performed before timing recovery operation as a timing and carrier recovery error algorithm.

8. The method of claim 7, further comprising:

receiving overlapping packets as samples of the downlink signal, the samples having an unknown symbol rate and frequency;

determining a timing error of the samples based on an estimate of the symbol rate, an estimate of the frequency, and a square of the samples;

decimating the samples by a decimation filter; and

determining a phase, frequency, and Doppler rate of the samples;

synchronizing the samples in time and frequency, based on the phase, frequency, and Doppler rate; and

updating the estimate of the symbol rate.

9. The method of claim 1, wherein the first processing block and the second processing block are implemented by one or more central processing units having multiple cores and implementing single instruction, multiple data (SIMD) processing.

10. A non-transitory computer-readable medium for processing a digital bit stream representative of a communication signal comprising instructions that when executed by one or more processors, cause the one or more processors to:

divide the digital bit stream into a plurality of data packets, each of the data packets of the plurality of data packets including an overlap of data from an adjacent packet;

at a first processing block of the one or more processors,

perform a timing recovery operation on a first portion of the plurality of data packets, and

perform a carrier recovery operation on the first portion of the plurality of data packets;

at a second processing block of the one or more processors and in parallel with the first portion of the plurality of packets,

perform the timing recovery error calculation on a second portion of the plurality of data packets; and

perform the carrier recovery error calculation on the second portion of the plurality of data packets; and

combine the first portion and the second portion based on timing and phase stitching.

11. The non-transitory computer-readable medium of claim 10, wherein the adjacent packets overlap in time by one percent of the length of the packets.

12. The non-transitory computer-readable medium of claim 10, wherein the plurality of data packets have varying lengths.

13. The non-transitory computer-readable medium of claim 10, wherein the timing recovery operation comprises instructions that further cause the one or more processors to determine phase offset information associated with in-phase and quadrature (I/Q) data of the first portion and the second portion.

14. The non-transitory computer-readable medium of claim 10, wherein the timing recovery operation comprises instructions that further cause the one or more processors to:

receive overlapping packets as samples of the downlink signal, the samples having an unknown symbol rate and frequency;

determine a timing error of the samples based on an estimate of the symbol rate;

decimate the samples by a decimation filter; and

determine a phase, frequency, and Doppler rate of the samples;

synchronize the samples as symbols, based on the phase, frequency, and Doppler rate; and

update the estimate of the symbol rate.

15. The non-transitory computer-readable medium of claim 14, wherein the carrier recovery operation comprises instructions that further cause the one or more processors to:

receive the symbols associated with the synchronized samples of the downlink signal;

determine a carrier error of the symbols based on an estimate of a frequency of the downlink signal and a product of the symbols raised to a power of n, wherein n is an integer;

decimating the symbols by a decimation filter; and

determining a phase, frequency, and Doppler rate of the symbols; and

updating the estimate of the frequency.

16. The non-transitory computer-readable medium of claim 10, wherein the carrier recovery is performed before timing recovery operation as a timing and carrier recovery error algorithm.

17. The non-transitory computer-readable medium of claim 16 comprising instructions that further cause the one or more processors to:

receive overlapping packets as samples of the downlink signal, the samples having an unknown symbol rate and frequency;

determine a timing error of the samples based on an estimate of the symbol rate, an estimate of the frequency, and a square of the samples;

decimate the samples by a decimation filter; and

determine a phase, frequency, and Doppler rate of the samples;

synchronize the samples in time and frequency, based on the phase, frequency, and Doppler rate; and

update the estimate of the symbol rate.

18. The non-transitory computer-readable medium of claim 10, wherein the one or more processors are implemented by one or more central processing units having multiple cores and implementing single instruction, multiple data (SIMD) processing and the one or more central processing units implement the first processing block and the second processing block.

19. A system for processing a digital bit stream representative of a communication signal, the system comprising:

a digitizer configured to convert a received analog signal into the digital bitstream; and

one or more processors having a plurality of processing blocks and configured to

divide the digital bit stream into a plurality of data packets, each of the data packets of the plurality of data packets including an overlap of data from an adjacent packet,

in a first processing block of the plurality of processing blocks,

perform a timing recovery operation on a first portion of the plurality of data packets, and

perform a carrier recovery operation on the first portion of the plurality of data packets;

in a second processing block of the plurality of processing blocks and in parallel with the first portion of the plurality of packets,

perform the timing recovery error calculation on a second portion of the plurality of data packets, and

perform the carrier recovery error calculation on the second portion of the plurality of data packets; and

combine the first portion and the second portion based on timing and phase stitching.

20. The system of claim 19, wherein the timing recovery operation comprises determining phase offset information associated with in-phase and quadrature (I/Q) data of the first portion and the second portion.

21. The system of claim 19, wherein the timing recovery operation comprises:

receiving overlapping packets as samples of the downlink signal, the samples having an unknown symbol rate and frequency;

determining a timing error of the samples based on an estimate of the symbol rate;

decimating the samples by a decimation filter; and

determining a phase, frequency, and Doppler rate of the samples;

synchronizing the samples as symbols, based on the phase, frequency, and Doppler rate; and

updating the estimate of the symbol rate.

22. The system of claim 21, wherein the carrier recovery operation comprises:

receiving the symbols associated with the synchronized samples of the downlink signal;

determining a carrier error of the symbols based on an estimate of a frequency of the downlink signal and a product of the symbols raised to a power of n, wherein n is an integer;

decimating the symbols by a decimation filter; and

determining a phase, frequency, and Doppler rate of the symbols; and

updating the estimate of the frequency.

23. The system of claim 19, wherein the one or more processors comprise one or more central processing units having multiple cores and implementing single instruction, multiple data (SIMD) processing.