CLAIMS

What is claimed is:

1. A method of determining one or more candidate prediction modes, the method comprising:

deriving, by a processor, a first indicator by parsing a bitstream, wherein the first indicator specifies whether any affine model is allowed to be a candidate motion model for an image block in a preset area;

deriving, by the processor, a second indicator by parsing the bitstream when the first indicator is equal to a first value which indicates an affine model is allowed to be a candidate motion model, wherein the second indicator specifies whether a 6-parameter affine model is allowed to be a candidate motion model for the image block in the preset area; and

determining, by the processor, one or more candidate prediction modes for the image block based on the first indicator and the second indicator.

2. The method of claim 1, wherein deriving the first indicator comprises parsing a sequence parameter set (SPS) of a sequence of the bitstream, wherein the preset area comprises the sequence, and wherein the deriving the second indicator comprises parsing the SPS for deriving the second indicator.

3. The method of any of claims 1-2, wherein the first indicator and/or second indicator is carried in a SPS raw byte sequence payload (RBSP).

4. The method of any of claims 1-3, further comprising deriving, in response to an affine model being allowed to be the candidate motion model, a third indicator by parsing the bitstream, wherein the third indicator specifies whether a prediction mode of the image block is an affine merge mode.

5. The method of any of claims 1-4, wherein, in response to an affine model being allowed to be the candidate motion model, the method further comprises:

deriving a fourth indicator by parsing the bitstream;

determining, in response to the fourth indicator being a second value, that a prediction mode of the image block is not an affine inter mode; and

determining, in response to the fourth indicator being a first value, that the prediction mode is an affine inter mode,

wherein the affine inter mode is a 6-parameter affine model mode or a 4-parameter affine model mode in response to the second indicator being a first value, or the affine inter mode is a 4-parameter affine model mode in response to the second indicator being a second value.

6. The method of any of claims 1-5, in response to the prediction mode being the affine inter mode and the second indicator indicates that the 6-parameter affine model is allowed to be a candidate motion model for the image block, the method further comprises:

deriving a fifth indicator by parsing the bitstream;

determining, in response to the fifth indicator being a first value, that the prediction mode is the 6-parameter affine model mode; and

determining, in response to the fifth indicator being a second value, that the prediction mode is the 4-parameter affine model mode.

7. The method of claim 6, further comprising deriving, in response to a sum value being greater than 0, a first set of motion vector difference (MVD) information by parsing the bitstream, wherein the sum value is a sum of the value of the fourth indicator and the value of fifth indicator.

8. The method of claim 6, further comprising deriving, in response to the sum value being greater than 1, a second set of MVD information by parsing the bitstream, wherein the sum value is a sum of the value of the fourth indicator and the value of fifth indicator.

9. An apparatus for determining one or more candidate prediction modes, the apparatus comprising:

a memory; and

a processor coupled to the memory and configured to perform any of claims 1-8.

10. A method implemented by a video encoder and comprising:

determining a second value for an affine inter flag;

encoding the second value for the affine inter flag into a bitstream;

determining a third value for an affine type flag;

encoding the third value for the affine type flag into the bitstream; and

~~determining a first value for a motion model indicator variable that specifies a motion model used to generate prediction samples of a current coding unit, wherein the motion model is one of a translational model, a 4-parameter affine model, or a 6-parameter affine model, and the first value for the motion model indicator variable is determined by the sum of the second value for the affine inter flag and the third value for the affine type flag.~~

~~11. An encoding apparatus comprising:~~

~~a memory; and~~

~~a processor coupled to the memory and configured to perform claim 10.~~

~~12. A method implemented by a video decoder and comprising:~~

~~receiving a bitstream comprising an affine inter flag and an affine type flag;~~

~~determining, based on a first value of the affine inter flag and a second value of the affine type flag, a third value of a motion model indicator variable; and~~

~~determining, based on the third value, whether a motion model is a translational model, a 4-parameter affine model, or a 6-parameter affine model.~~

~~13. The method of claim 12, wherein the determining, based on a first value of the affine inter flag and a second value of the affine type flag, a third value of a motion model indicator variable comprises:~~

~~determining, based on the sum of the first value of the affine inter flag and the second value of the affine type flag, the third value of a motion model indicator variable.~~

~~14. A decoding apparatus comprising:~~

~~a memory; and~~

~~a processor coupled to the memory and configured to perform claim 12 or 13.~~

~~15. A computer program product comprising computer-executable instructions stored on a non-transitory medium that when executed by a processor cause an apparatus to perform any one of claims 1 to 8, 10, 12 and 13.~~

1. A method implemented by a video decoder and comprising:

receiving, by the video decoder, a video bitstream comprising a sequence parameter set (SPS) raw byte sequence payload (RBSP), wherein the SPS RBSP comprises a first SPS level flag, wherein the first SPS level flag equal to 1 specifies that an affine inter flag is present in coding unit syntax, wherein the first SPS level flag equal to 0 specifies that the affine inter flag is not present in the coding unit syntax, and wherein the affine inter flag equal to 1 specifies that for a current coding unit, when decoding a P or a B slice, affine model based motion compensation is used to generate prediction samples of the current coding unit; and

decoding, based on the first SPS level flag, a video sequence from the video bitstream.

2. The method of claim 1, wherein the SPS RBSP further comprises a second SPS level flag, wherein the second SPS level flag equal to 1 specifies that affine_type_flag is presented in the coding unit syntax, the second SPS level flag equal to 0 specifies that affine_type_flag is not presented in the coding unit syntax.

3. The method of claim 1 or 2, wherein the video bitstream further comprises the coding unit syntax.

4. The method of claim 3, wherein the coding unit syntax comprises the affine inter flag.

5. The method of any one of claims 1 to 4, wherein the affine inter flag equal to 0 specifies that the current coding unit is not predicted by affine model based motion compensation.

6. A method implemented by a video encoder and comprising:

generating, by the video encoder, a first sequence parameter set (SPS) level flag, wherein the first SPS level flag equal to 1 specifies that an affine inter flag is present in coding unit syntax, wherein the first SPS level flag equal to 0 specifies that the affine inter flag is not present in the coding unit syntax, and wherein the affine inter flag equal to the first value specifies that for a current coding unit, when decoding a P or a B slice, affine model based motion compensation is used to generate prediction samples of the current coding unit;

encoding the first SPS level flag into an SPS raw byte sequence payload (RBSP); and

encoding the SPS RBSP into a video bitstream.

7. The method of claim 6, wherein the affine inter flag equal to 0 specifies that the current coding unit is not predicted by affine model based motion compensation.

8. An encoding apparatus comprising:
a memory; and
a processor coupled to the memory and configured to perform the method of claim 6 or 7.

9. A decoding apparatus comprising:
a memory; and
a processor coupled to the memory and configured to perform the method of any one of claims 1 to 5.

10. A computer program product comprising computer-executable instructions stored on a non-transitory medium that when executed by a processor cause an apparatus to perform the method of any one of claims 1 to 7.