ABSTRACT

METHOD OF FORMING SHALLOW TRENCH ISOLATION

A new method of forming shallow trench isolations has been achieved. Trench oxide grooving due to etch stop layer etching is eliminated by the formation of a liner oxidation overlying a polysilicon layer. A semiconductor substrate is provided. A pad oxide layer is grown. A polysilicon layer is deposited. Optionally, the polysilicon layer may be ion implanted to increase the oxidation rate. A silicon nitride layer is deposited. The silicon nitride layer, the polysilicon layer, the pad oxide layer and the semiconductor substrate are patterned to form trenches for planned shallow trench isolations. A liner oxidation layer is grown overlying the semiconductor substrate, the pad oxide layer, and the polysilicon layer inside the trenches. A trench oxide layer is deposited overlying said silicon nitride layer and filling said trenches. The trench oxide layer is polished down to the silicon nitride layer. The silicon nitride layer, the polysilicon layer, the pad oxide layer are etched away. The presence of the liner oxidation layer and the oxidized polysilicon layer protect the trench oxide layer during the etching of the silicon nitride layer, the polysilicon layer, and the pad oxide layer. The integrated circuit is completed.

(FIGURE 4 IS SUGGESTED FOR PUBLICATION)