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Integrated Circuit and Method of Fabricating an Integrated Circuit That Includes a Frame Carrier Interposer

Technical Field

The present invention relates generally to an integrated circuit. More particularly, it pertains to an integrated circuit and method that include a frame carrier interposer.

Background

Integrated circuit technology relates to integrating numerous different types of electronic devices to formulate vast arrays of integrated circuits. The complexity of these circuits requires the use of an ever-increasing number of linked devices that are fabricated in ever smaller packages. One challenge is to develop improved methods for electrically connecting and packaging circuit devices which occupy less surface area on a chip/die or substrate.

Some computing systems are fabricated with many chips that perform different functions. The chips are packaged together to form a complete system.

One common type of integrated circuit uses a patterned conductive leadframe as an interposer. The leadframe interposer transfers currents among related devices. The thickness of a conventional leadframe is typically between 100 um and 200 um. The relatively large thickness of the leadframe typically generates a larger than desired inductance within the current paths of the leadframe when currents, such as I/O signals, travel through the leadframe. The thickness also causes fine pitch process limitations when the leadframe is fabricated. The design rule in conventional leadframes typically exceeds 200/200. In addition, integrated circuits that include conventional leadframes are generally larger (i.e., thicker) and slower because the electrical paths are typically longer in a leadframe interposer than other types of interposers.

Another type of integrated circuit uses a rigid substrate as part of an interposer. Interposers that include rigid substrates are relatively thick such that the integrated circuits which are produced with rigid substrate interposers have a

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larger than desired profile. An integrated circuit that includes an interposer with a rigid substrate is also generally more expensive to produce because it must be fabricated in batch form and requires relatively high fabrication costs. In addition, the cost of materials associated with fabricating rigid substrate interposers is relatively high.

The rigid substrate is typically made from a polymer resin with fiber, such as Bismaleimide Triazine (hereafter BT)/ epoxy resins, which tend to absorb moisture and negatively impact MST performance of the package. There are also typically outgassing problems with polymers such as BT. In addition, most of the resins that form rigid substrate interposers degrade at relatively low temperatures. The low degradation temperatures reduce the range of temperatures that an integrated circuit package, which includes a rigid substrate interposer, may be exposed to during fabrication and operation. Rigid substrate interposers are typically manufactured according to a 65/65 design rule.

Another type of integrated circuit uses a flexible substrate as part of an interposer. The flexible substrate will hereafter be referred to as flex. One advantage of flex interposers is that they are relatively thin so the current paths in the interposer generate less inductance during operation. In addition, the flex interposers can typically be manufactured with a better design rule, such as 30/30 or even lower.

One drawback with flex interposers is that they are relatively expensive to produce. Another drawback is that flex is typically formed of a polymer tape or film that tends to absorb a large amount of moisture thereby effecting package reliability. It is also typically difficult to adequately adhere anything, including copper foil, electronic devices and/or solder masks among others, to the flex during fabrication of an integrated circuit that includes a flex interposer. The inability to adequately adhere anything to the flex results in integrated circuits that have poor reliability. Another drawback with flex interposers is that they are difficult to handle during fabrication of integrated circuits due to their lack of thickness and rigidity and a higher than desired shrinkage factor.

Thus, what is needed are an improved integrated circuit and method which utilizes a relatively thin and low cost interposer that is fabricated

according to superior design rules. It would also be desirable if the interposer included little or no polymers to reduce moisture absorption and outgassing.

Summary

The above mentioned problems with integrated circuits are addressed by an integrated circuit and method that include a frame carrier interposer. The frame carrier interposer (hereafter FCI) may be produced in batch tape or reel form with a superior design rule. The FCI is relatively thin so that it can be used to produce low profile integrated circuits. The current paths in the FCI also generate low inductance during operation because the FCI is relatively thin.

In some embodiments, the FCI will include no polymers such that FCI has less moisture absorption and outgassing problems than other types electronics packages. The FCI is also easily configured with a die pad area such that I/O devices can be routed to an integrated circuit that includes the FCI.

In an illustrative embodiment, an integrated circuit includes an FCI and at least one electronic device mounted to the FCI. The FCI includes a conductive foil that is laminated to only a dry film and electrically connected to the at least one electronic device.

In another embodiment, an integrated circuit includes an FCI and a die mounted to the FCI. The FCI includes a copper foil that is laminated to only a dry photosensitive film and electrically connected to the die.

In another example embodiment, a method of fabricating an integrated circuit includes laminating a conductive foil to only a dry film to form an FCI and patterning the conductive foil. The method may also include punching a pattern into the dry film.

In still another embodiment, a method fabricating an integrated circuit includes laminating a copper foil to only a dry film to form an FCI, and patterning the copper foil after the copper foil has been laminated to the dry film. The method may also include patterning the dry film.

In yet another embodiment, a method of fabricating an integrated circuit includes laminating a conductive foil to only a dry film to form an FCI; patterning the conductive foil; and photo-imaging a pattern into the dry film.

The method may also include photo-imaging a pattern into the dry film after laminating the conductive foil to the dry film.

In another example embodiment, a method of fabricating an integrated circuit that includes laminating a conductive foil to only a dry film to form an FCI; patterning the conductive foil; and punching a pattern into the dry film. The method may also include punching a pattern into the dry film before laminating the conductive foil to the dry film.

In another example embodiment, an integrated circuit includes an FCI, a first die and at least one leadwire. The FCI includes a conductive foil laminated to only a dry film. The first die is mounted to the conductive foil on the FCI and the at least one leadwire electrically connects the conductive foil to the first die.

In another example embodiment, an integrated circuit includes an FCI and a die mounted to the FCI. The FCI includes a conductive foil laminated to only a dry film. The die includes solder balls that electrically connect the die to the conductive foil.

In another example embodiment, a method of fabricating an integrated circuit that includes laminating a conductive foil to only a dry film to form an FCI and patterning the conductive foil. The method further includes adhering an electronic device to the conductive foil in the frame carrier interposer and encapsulating the electronic device on the frame carrier interposer before removing the dry film.

In another example embodiment, an integrated circuit includes an FCI and a die mounted to the FCI. The FCI includes a conductive foil laminated to only a dry film and a soldermask adhered to the conductive foil. A die is mounted to the frame carrier interposer and electrically connected to the conductive foil.

These and other embodiments, aspects, advantages, and features of the present invention are set forth in part in the detailed description which follows. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 is a schematic cross-sectional view illustrating an example embodiment of an integrated circuit.

Figure 2 is a schematic cross-sectional view similar to Figure 1 illustrating another example embodiment of an integrated circuit.

Figure 3 is a schematic cross-sectional view similar to Figure 1 illustrating yet another example embodiment of an integrated circuit.

Figure 4 is a schematic cross-sectional view similar to Figure 1 illustrating still another example embodiment of an integrated circuit.

Figure 5 is a schematic cross-sectional view similar to Figure 1 illustrating another example embodiment of an integrated circuit.

Figure 6 is a schematic cross-sectional view similar to Figure 1 illustrating another example embodiment of an integrated circuit.

Figure 7 is a schematic cross-sectional view similar to Figure 1 illustrating another example embodiment of an integrated circuit.

Figures 8-12 illustrate one embodiment of a method of fabricating a FCI.

Figures 13-16 illustrate another embodiment of a method of fabricating a FCI.

Figures 17-19 illustrate one embodiment of a method of fabricating an integrated circuit.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which show specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The scope of the present invention is defined only by the claims and the full scope of equivalents to which the claims are entitled.

Figure 1 is a schematic cross-sectional view illustrating an example embodiment of an integrated circuit 10. Integrated circuit 10 includes an FCI 12

and at least one electronic device, such as die 14, mounted to FCI 12. FCI 12 includes a conductive foil 15 that is laminated to only a dry film 16 and is electrically connected to die 14. Conductive foil 15 is patterned to provide circuit paths to and from die 14 and/or other electronic devices. In some embodiments, FCI 12 has a thickness less than 150 microns.

Die 14 is secured to FCI 12 using an adhesive 17. Die 14 may be secured to conductive foil 15 and/or dry film 16. In the embodiment illustrated in Figure 1, die 14 is on the conductive foil 15 side of FCI 12, although in other embodiments, die 14 may be on the dry film 16 side of FCI 12. Die 14 may be over-molded with an encapsulate 18 according to conventional techniques. Encapsulate 18 may extend into the pattern of conductive foil 15 and/or dry film 16.

In some example embodiments, die 14 is electrically connected to conductive foil 15 using leadwires 19, while in other embodiments die 14 may alternatively (or in addition to) be electrically connected to conductive foil 15 where die 14 is mounted to FCI 12. In the sample embodiment illustrated in Figure 1, dry film 16 is patterned such that an array of solder balls 20 extends through portions of dry film 16 to engage at least one of the conductive foil 15, die 14 and leadwires 19.

As used herein conductive foil means any sheet of conductive material (e.g., copper) with a thickness less than 40 micron. In addition, as used herein dry film means protection coating material, such as solder-mask in film form. In some embodiments, dry film 16 is a photosensitive film.

Figure 2 illustrates an example embodiment of integrated circuit 10 that includes another die 24 that may be electrically connected to first die 14. Die 24 is mounted to conductive foil 15 adjacent to 14 on the same side of FCI 12. In some embodiments, FCI 12 may be folded over to stack die 24 onto die 14.

Figure 3 illustrates another example embodiment of integrated circuit 10. In the example embodiment illustrated in Figure 3, die 14 is a stacked die that includes a second die 34A stacked onto a first die 34B.

Each of dies shown in Figures 2 and 3 may or may not be connected to one another by any conventional technique, including one or more of the conductive foil 15 and leadwires 19.

Figure 4 illustrates a sample embodiment of integrated circuit 10 where dry film 16 is in a pattern and at least one leadwire 19B extends through FCI 12 into electrical connection with die 14. A first encapsulate 18A covers die 14 and a second encapsulate 18B covers the at least one leadwire 19B.

Figure 5 illustrates another sample embodiment of integrated circuit 10 which includes die 14 and FCI 12 arranged in a flip-chip configuration. Die 14 includes solder balls 40, or some other conventional connection, that electrically connects die 14 to conductive foil 15.

Figures 6 and 7 illustrate another example embodiment of integrated circuit 10. In the example embodiment illustrated in Figures 6 and 7, integrated circuit 10 includes an FCI 12 and a die 14 mounted to FCI 12. FCI 12 includes a conductive foil 15 that is laminated to only a dry film 16 and is electrically connected to die 14 using leadwires 19, or some other form of connection. Conductive foil 15 is patterned to provide circuit paths to and from die 14 and/or other electronic devices. A soldermask 21 is adhered to conductive foil 15 on the side of conductive foil 15 that opposes dry film 16. In some embodiments, soldermask 21 is a protection coating layer made of an acrylic and epoxy combination

In the embodiment illustrated in Figure 6, die 14 is secured to soldermask 21 using adhesive 17, while in the embodiment illustrated in Figure 7, die 14 is secured to dry film 16 using adhesive 17. Die 14 may be over-molded with an encapsulate 18 that may extend into a pattern on dry film 16 (Figure 6) or soldermask 21
(Figure7).

An example embodiment of a method of fabricating an FCI 52 to be used in an integrated circuit is shown in Figures 8-12. Figure 8 shows FCI 52 after a conductive foil 55 (e.g., copper foil) has been laminated to only a dry film 56 and before either conductive foil 55 or dry film 56 has been patterned. Figures 9 and 10 show FCI 52 after dry film 56 has been photo- imaged to create a pattern in

dry film 56. In some embodiments, dry film is made by Tayio of Japan under model nos. AUS402, PFR-800, TR6315. In other embodiments, dry film is DuPont Pyralux PC1020, or Sumilite CFP1123 and 1122. Figures 11 and 12 show FCI 52 after conductive foil 55 has been patterned.

Another example embodiment of a method of fabricating an FCI 52 to be used in an integrated circuit is shown in Figures 13-16. Figure 13 shows dry film 56 after dry film 56 has been punched into a pattern. In some embodiments, dry film 56 acts as a mechanical carrier for transportation and is made from PVC or PTFE among other polymeric materials. Figure 14 shows FCI 52 after dry film 56 has only been laminated to conductive foil 55. Figures 15 and 16 show FCI 52 after conductive foil 55 has been patterned.

An example embodiment of a method of fabricating an integrated circuit 70 is shown in Figures 17-19. Figure 17 shows integrated circuit 70 after a conductive foil 75 (e.g., copper foil) has been laminated to only a dry film 76 to form a frame carrier interposer 72 and conductive foil 75 has been patterned. A die 74 is adhered to a second side 82 of conductive foil 75 and encapsulated with an encapsulate 78. In this example embodiment, frame carrier interposer 72 acts as a carrier during fabrication of integrated circuit 70.

Figure 18 shows integrated circuit 70 after dry film 76 is removed from a first side 81 of conductive foil 75 and an array of solder balls 83 is added. Figure 19 shows integrated circuit 70 after a soldermask 84 is adhered to the first side 81 of conductive foil 75 to provide protection for conductive foil 75.

The example integrated circuits and methods described herein utilize a relatively thin and low cost FCI. The FCI is fabricated according to superior design rules that allow circuit designers to increase circuit density. In some embodiments, the FCI will include less polymers such that the FCI has less moisture absorption and outgassing problems as compared to other types electronics packages that include interposers with polymers.

The FCI may be produced in batch tape or reel form with a superior design rule. In addition, the FCI is relatively thin so that it can be used to produce low profile integrated circuits that generate low inductance during operation.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. An integrated circuit comprising:

a frame carrier interposer that includes a conductive foil laminated to only a dry film; and

at least one electronic device mounted to the frame carrier interposer and electrically connected to the conductive foil.

2. The integrated circuit of claim 1, wherein the frame carrier interposer has a thickness less than 150 micron.

3. The integrated circuit of claim 1, wherein the dry film is a photosensitive film.

4. The integrated circuit of claim 1, wherein the conductive foil is a copper foil.

5. The integrated circuit of claim 1, wherein the at least one electronic device includes a die.

6. An integrated circuit comprising:

a frame carrier interposer that includes a copper foil laminated to only a dry photosensitive film; and

a die mounted to the frame carrier interposer and electrically connected to the copper foil.

7. The integrated circuit of claim 1, wherein the frame carrier interposer has a thickness less than 150 micron.

8. A method of fabricating an integrated circuit, comprising:

laminating a conductive foil to only a dry film to form a frame carrier interposer; and

patterning the conductive foil.

9. The method of claim 8, wherein laminating the conductive foil to the dry film includes laminating a copper foil to the dry film.

10. The method of claim 8, wherein patterning the conductive foil includes patterning the conductive foil after laminating the conductive foil to the dry film.

11. The method of claim 8, further comprising patterning the dry film.

12. The method of claim 11, wherein patterning the dry film includes photo-imaging the dry film.

13. The method of claim 11, wherein patterning the dry film includes punching a pattern into the dry film.

14. A method of fabricating an integrated circuit, comprising:

laminating a copper foil to only a dry film to form a frame carrier interposer; and

patterning the copper foil after laminating the copper foil to the dry film.

15. The method of claim 14, further comprising patterning the dry film.

16. A method of fabricating an integrated circuit, comprising:

laminating a conductive foil to only a dry film to form a frame carrier interposer;

patterning the conductive foil; and

photo-imaging a pattern into the dry film.

17. The method of claim 16, wherein photo-imaging the pattern into the dry film includes photo-imaging the pattern into the dry film after laminating the conductive foil to the dry film.

18. A method of fabricating an integrated circuit, comprising:

laminating a conductive foil to only a dry film to form a frame carrier interposer;

patterning the conductive foil; and

punching a pattern into the dry film.

19. The method of claim 18, wherein punching a pattern into the dry film includes punching a pattern into the dry film before laminating the conductive foil to the dry film.

20. An integrated circuit comprising:

a frame carrier interposer that includes a conductive foil laminated to only a dry film;

a first die mounted to the conductive foil on the frame carrier interposer; and

at least one leadwire electrically connecting the conductive foil to the first die.

21. The integrated circuit of claim 20 further comprising an encapsulate covering the first die and the at least one leadwire.

22. The integrated circuit of claim 21, wherein the conductive foil is in a pattern and the encapsulate at least partially extends into at least a portion of the pattern.

23. The integrated circuit of claim 20, further comprising an adhesive that secures the first die the conductive foil.

24. The integrated circuit of claim 20, wherein the dry film is in a pattern, and further comprising an array of solder balls extending into the pattern in the dry film such that the solder balls are electrically connected to at least one of the conductive foil, the first die and the at least one leadwire.

25. The integrated circuit of claim 20 further comprising a second die electrically connected to the first die.

26. The integrated circuit of claim 25 wherein the second die is stacked onto the first die.

27. The integrated circuit of claim 25 wherein the second die is electrically connected to the first die by a leadwire.

28. The integrated circuit of claim 26 wherein the second die is mounted to the conductive foil in the frame carrier interposer.

29. The integrated circuit of claim 20 wherein the dry film is in a pattern and the at least one wire bond extends through the frame carrier interposer.

30. The integrated circuit of claim 29 further comprising a first encapsulate covering the first die and a second encapsulate covering the at least one leadwire.

31. An integrated circuit comprising:

a frame carrier interposer that includes a conductive foil laminated to only a dry film; and

a die mounted to the frame carrier interposer, the die including solder balls that electrically connect the die to the conductive foil.

32. The integrated circuit of claim 31 further comprising an encapsulate covering the die.

33. The integrated circuit of claim 31, wherein the dry film is in a pattern and further comprising a second array of solder balls extending into portions of the pattern in the dry film such that at least one of the solder balls is electrically connected to the conductive foil.

34. A method of fabricating an integrated circuit, comprising:

laminating a conductive foil to only a dry film to form a frame carrier interposer;

patterning the conductive foil;

adhering an electronic device to the conductive foil in the frame carrier interposer;

encapsulating the electronic device on the frame carrier interposer; and

removing the dry film.

35. The method of claim 34, further comprising adhering a soldermask to the conductive foil.

36. The method of claim 34, wherein laminating a conductive foil to only a dry film includes laminating the dry film to a first side of the conductive foil, and adhering a soldermask to the conductive foil includes adhering the soldermask to the first side of the conductive foil.

37. An integrated circuit comprising:

a frame carrier interposer that includes a conductive foil laminated to only a dry film and a soldermask adhered to the conductive foil; and

a die mounted to the frame carrier interposer and electrically connected to the conductive foil.

38. The integrated circuit of claim 37 wherein the soldermask is in a pattern and the die is mounted to the soldermask.

39. The integrated circuit of claim 37, wherein the dry film is in a pattern and the die is mounted to the dry film.