

"Circuit arrangement for a receiver comprising two phase control loops".

The invention relates to a circuit arrangement as claimed in the introductory part of Claim 1. A phase control loop is understood to mean a circuit comprising a frequency-controllable oscillator whose output signal is applied - optionally via a fixed or adjustable frequency divider - to a phase discriminator, which compares this signal with a reference signal and produces an output signal corresponding to the phase difference, which output signal is used - preferably via a low-pass filter - to control the frequency of the oscillator. Phase control loops of this type are now commonly denoted as "PLL-circuits".

"Pilot signal" must here and in the further course of the description be understood to mean a signal contained in the modulating signal of the received signal and having a constant frequency - preferably the 19 kHz pilot tone in the stereo multiplex signal of an FM stereo transmitter.

A circuit arrangement of the type described in the opening paragraph is known, for example, from the periodical "Grundig Technische Informationen", No. 1/2, 1980, page 12, Figure 12. Therein the first phase control loop comprises a frequency divider which is programmable for tuning purposes, whilst the second phase control loop is part of a stereo decoder. The two phase control loops require a total of two voltage-controlled oscillators - at least the oscillator included in the second phase control loop requiring adjustment - and a reference oscillator.

It is an object of the invention to reduce the cost and designing efforts for such a circuit.

Based on a circuit arrangement of the type described in the opening paragraph this object is accomplished by means of the measures described in the characterizing part of Claim 1.

On itself JP-A-5 705 7051 (corresponding to US-A-4,454,607 of 12-6-1984) discloses an FM-receiver with synthesizer tuning, which is tuned by means of tuning data supplied by a CPU (Central Processing Unit). The CPU employs as a clock pulse generator a

voltage-controlled oscillator included in a phase control loop, which is synchronized by the 19 kHz-stereo pilot of a stereo multiplex signal. As is known, the value of the tuning data depends on a value which is entered into the CPU and does not depend on the precise frequency of the clock pulse generator. Consequently, the tuning of this prior art FM-receiver is not synchronized with the 19 kHz stereo pilot and an additional and very stable reference oscillator must of necessity be used to stabilize the tuning frequency.

EP-A-0,088,467 describes a receiver comprising a stereo PLL which is synchronized by a pilot signal contained in the RF signal. The function of this PLL corresponds to that of the second PLL mentioned above in relation to Claim 1.

The reference oscillator of the circuit arrangement according to the invention has a dual function. In the first phase control loop it acts as a reference oscillator and in the second phase control loop it acts as a voltage-controlled oscillator which is in synchronism with the pilot signal. As a result thereof the voltage-controlled oscillator which would otherwise be additionally required for the second phase control loop can be omitted, and also the adjusting operation required for this oscillator is no longer necessary.

When signals are received which do not contain a pilot signal the reference oscillator is not synchronized, so it oscillates at its own natural frequency. When this frequency deviates from the frequency at which the oscillator oscillates when it is synchronized by the pilot signal, the frequency of the signal applied from the first phase control loop to the mixer stage also changes, that is to say the tuning is changed in dependence on the fact whether a pilot signal is received or not received. In order to keep this change as small as possible, the reference oscillator must have a highest possible frequency stability, which can, for example, be accomplished with the aid of a quartz oscillator. Particularly for this case a further embodiment of the invention provides that the frequency of the oscillator is at least approximately an integral multiple of the frequency of the pilot signal. However, the oscillator frequency may alternatively be a rational multiple of the pilot frequency.

When a tuning action to a transmitter transmitting a pilot signal is initiated, comparatively large phase differences between

the pilot signal and the signal derived from the reference oscillator may occur, which at the output of the phase discriminator results in a signal which effects a comparatively large detuning of the reference oscillator. Because of the presence of the frequency divider, this
5 detuning of the reference oscillator usually effects a still larger detuning of the oscillator comprised in the first phase control loop, so that also the tuning of the receiver is affected. The extent to which the receiver tuning is affected can be so large that correct tuning to the transmitter is not possible. In accordance with a further embodiment
10 of the invention this is prevented in that the output voltage of the phase discriminator is conveyed via a limiter. The limiter then limits the detuning of the reference oscillator and consequently the detuning of the oscillator in the first control loop.

However, because of this limitation, in the event of
15 significant phase deviations, the frequency of the reference oscillator can be synchronized with the pilot signal only relatively slowly, which is unwanted in many cases. A faster synchronization can be accomplished in accordance with a further embodiment of the invention in that a circuit for changing the frequency division ratio of the frequency
20 divider is provided which is controlled by the output signal of the phase discriminator via a threshold device. This construction is, however, independent of the invention. It can be used in all cases in which a fast synchronization of the phase control loop is important.

The invention will now be described in greater detail
25 with reference to the accompanying drawings, in which

Figure 1 shows an embodiment of the invention,

Figure 2 shows a further embodiment of the second control loop,

Figure 3 shows the structure of a counter having a
30 controllable frequency divider ratio and being suitable for use in the embodiment shown in Figure 2 and

Figure 4 is a Table showing the static behaviour of the logic processing circuit in the structure shown in Figure 3.

Figure 1 shows the block diagram of a VHF-receiver for
35 receiving stereo signals. The received signal is applied from the aerial 1 directly or via a preamplifier, not shown, to a mixer stage 2 in which it is mixed with an oscillator signal, so that the received signal

is converted to the intermediate frequency range, for example 10.7 MHz. The intermediate frequency signal is amplified and demodulated by an FM-demodulator 3. The modulating signal, a multiplex signal in the event of a stereo transmission, which contains in addition to the sum signal for the left (L) and the right (R) channel a 19 kHz pilot signal and a differential signal in the form of two sidebands around a suppressed 38 kHz subcarrier, appears at the output of the FM-demodulator. At the output of a first deemphasis means 4 the sum signal $L + R$ then appears, while the differential signal $L - R$ occurs at the output of a second deemphasis means 5, to which the output signal of a multiplier stage 6 is applied, which multiplies the multiplex signal by a 38 kHz signal. The sum and differential signals, respectively at the outputs of the deemphasis means 4 and 5 are then converted in the customary way, not shown further, into signals for the left and right channels, amplified and reproduced via a suitable acoustic transducer.

The oscillator signal for the mixer stage 2 is generated by the frequency-controllable oscillator 7 of a first phase control loop. In addition, the first phase control loop comprises an adjustable frequency divider 8, which reduces the oscillator frequency in accordance with an adjustable factor of n , and also a phase discriminator 9 which compares the phases of the frequency-reduced oscillator signal and a reference signal of a constant frequency and at its output produces a signal which corresponds to the phase difference between these two signals and is applied via a low-pass filter 10 to the control input of the frequency-controllable oscillator 7, which is controllable by the voltage applied to its control input. The frequency is then varied so long until the phase difference at the output of the phase discriminator 9 has substantially become equal to zero and the oscillator 7 is in synchronism with the reference signal.

The reference signal is produced with the aid of a reference oscillator 11 whose frequency is an integral multiple of the frequency of the pilot signal, that is to say, 4,56 MHz. The frequency of the output signal of the reference oscillator is reduced by a frequency divider 12 in the ratio $1/m$ and the reduced signal is applied as a reference signal to the phase discriminator 9. In the synchronized state, the frequency of the oscillator 7 is then n/m -times the frequency of the reference oscillator 11. Up to this point of the description the

stereo receiver as shown in Figure 1 is known in essence. According to the invention, in contrast with the prior art, the reference oscillator is, however, in the form of an electronic frequency-controllable oscillator and is included in a second phase control loop which produces
5 the (38 kHz) subcarrier signal.

In addition to the reference oscillator 11, this second phase control loop comprises a frequency divider 13, which reduces the frequency of the output signal of the reference oscillator 11 in the ratio $1/N$, where N is constant and is 240 for the above-mentioned value
10 of the oscillator frequency (4.56 MHz), so that the oscillator frequency is reduced to 38 kHz. The output signal of the frequency divider 13 is multiplied in the multiplier stage 6 by the multiplex signal from the output of the FM demodulator 3 and also reduced in frequency by means of a further frequency divider 14 in the ratio 1 : 2, so that a 19 kHz
15 signal is present at the output of this frequency divider. In a phase discriminator 15 this signal is compared with the pilot signal contained in the output signal of the FM-demodulator 3. The output voltage of the phase discriminator, whose amplitude or duty cycle corresponds to the phase difference, is applied via a switch 16, which is in the open
20 condition for mono reception and in the closed condition for stereo reception, to a low-pass filter 17 whose output is connected to the control input of the reference oscillator 11, so that the frequency of the oscillator 11 is controlled in accordance with the output signal of the phase discriminator 15.

The reference oscillator 11 is preferably a quartz
25 oscillator. The frequency of a quartz oscillator can then be controlled by, for example, a capacitance diode, which is connected relative to the quartz in the same way as variable capacitors are usually arranged, and thus operates e.g. in series with the quartz resonator. Such an
30 oscillator has indeed only a comparatively small, but still fully adequate detuning range when the oscillator frequency corresponds to an integral multiple of the frequency of the pilot signal. The switch 16 is operated by a pilot signal detector 18, which is required in stereo receivers anyway and which always closes the switch 16 when a pilot
35 signal is detected and in all other cases keeps the switch in the open condition. Such a pilot signal detector does not increase the cost since, as described above, it is required in a stereo receiver anyway.

The circuit operates as follows:

For mono reception, the switch 16 is opened and the oscillator 11 is not synchronized. The first phase control loop then receives a signal having a frequency of 4.56 MHz, whose stability is determined by the properties of the quartz. For stereo reception, the switch 16 is closed and the reference oscillator 11 is synchronized by the frequency of the pilot signal contained in the multiplex signal. The frequency stability of the reference oscillator depends in this case on the frequency stability of the pilot signal transmitted by the transmitter. As this frequency may fluctuate through ± 1 Hz, this corresponds in the VHF-range (100 MHz) to a possible frequency change of ± 5 kHz. Such slight frequency shifts do not interfere with the operation of the receiver shown in Figure 1.

When the phase discriminator 15 is in the form of a multiplier stage, its output signal contains an a.c. voltage component, which is produced by multiplying the 19 kHz output signal of the frequency divider 14 by the frequency components (for example 15 kHz) contained in the multiplex signal and is suppressed by the low-pass filter 17. In addition, the direct current operating point of such a phase discriminator is shifted in accordance with the phase difference between the output signal of the frequency divider 14 and the pilot signal contained in the multiplex signal, which causes a corresponding frequency shift of the oscillator 11. If the multiplex signal did not contain a pilot signal, no d.c. offset would occur at the output in the event of an ideal phase discriminator, so that also the reference oscillator frequency would not be shifted. Then the switch 16 in the connection between the phase discriminator 15 and the low-pass filter 17 could be dispensed with. However, in practice phase discriminators evidence a dc-offset at their output, so that the frequency of the oscillator 11 would still be shifted, even when no pilot signal were present. This shift might affect the tuning by the first phase control loop in an unacceptable manner, and switch 16 is provided to prevent this. A further possibility is, however, to limit the maximum possible frequency shift, that is to say the amplitude at the output of the low-pass filter 17, to a value which does not affect the function of the receiver. Switch 16 could then also be omitted.

Figure 2 shows the block diagram of the second phase

control loop thus modified, the same reference numerals having been used for identical components. The output signal of the phase discriminator 15 is then directly supplied to the low-pass filter 17, and the output of the low-pass filter 17 is connected to the control input of the oscillator 11 via a limiter 19. As a result thereof the maximum possible detuning of the reference oscillator is also limited, so that it cannot assume a value which would interfere with the tuning. On the other hand, this limiting operation has for its effect that the period of time required to synchronize the oscillator 11 with the pilot signal is extended. This disadvantage caused by the use of the limiter 19 can, however, be eliminated by using, instead of the frequency divider 13 with a fixed frequency divider ratio, a frequency divider 20 having an electronically controllable frequency division ratio, whose input 211 is connected to the output of the oscillator and whose output 212 is connected to the input of the 1:2 frequency divider 14. The frequency divider ratio is controlled with the aid of two comparators 22 and 23, whose inputs are connected to the output of the low-pass filter and whose outputs are connected to a control input 213 or 214 of the frequency divider 20.

20 If the output voltage of the low-pass filter 17 is located in a range between the limits U_1 and U_2 , the output signals s_m and s_p of the comparators 22 and 23, are equal to zero. In this case the frequency divider factor of the frequency divider 20 is exactly 120. The values U_1 and U_2 are preferably chosen such that that value of the output voltage of low-pass filter 17 at which absolutely no detuning of the oscillator 11 occurs is located halfway between these limits. They should be located between those values at which the limiter 19 produces a limitation. If the output voltage of the low-pass filter 17 is located above U_1 and U_2 , the signal s_m at the input 213 is equal to 1 and the signal s_p at the input 214 is equal to 0. In this case the frequency divider factor is reduced to the value 118. If in contrast therewith the output voltage of the low-pass filter 17 is less than U_1 and U_2 , then s_p is equal to 1 and s_m is equal to 0. In this case the frequency divider factor is increased to the value 122. In both cases the frequency of the output signal is changed by approximately 320 Hz. So even if in the worst case the phase shift were 180° , the phases of the output signal of the frequency divider 15 and

the pilot signal would be synchronized with each other in only a few ms; if however the frequency divider factor were not changed, approximately 500 ms would be required, provided that detuning of the oscillator were limited to approximately 5×10^{-5} .

5 Figure 3 shows an embodiment of the frequency divider
20. It comprises six series-arranged 1:2-frequency dividers, which are preferably constituted by so-called toggle-flipflops (Tietze/Schenck "Halbleiter/Schaltungstechnik", 4th edition 1978, page 166) and are triggered at their negative edges. The signal is not only applied to the
10 chain of frequency divider zones 1...206 but also to the input 211 of an inverter 215, whose output is connected to the reset input of an RS-flipflop whose output is connected to the clockpulse input of a further toggle flipflop 216. The output of this toggle-flipflop constitutes the output 212 of the frequency divider 20. The set input of the RS-flipflop
15 217 is connected to the output of a logic combining circuit 218, which combines the output signals $s_1...s_6$ of the frequency dividers 201...206 and also the output signals s_m , s_p of the comparators 22 and 23.

 The output of the RS-flipflop 217 is furthermore
20 connected to the reset inputs R of the frequency dividers 201 and also 203...206, and to the set input S of the frequency divider 202. For the case in which the output state of the logic combining circuit corresponds to the logic signal "1", the outputs of the frequency divider flipflops 201 and 203...206 are equal to "0" and the output of
25 the flipflop 202 is equal to "1". If the output signals $s_6...s_1$ of the frequency dividers 206...201 are combined to form a six-bit binary data word, in which the most significant binary bit precedes the least significant binary bit (s_6 is the most significant bit - s_1 is the least significant bit), then this switching condition corresponds to the
30 data word 000010. This corresponds to the number 2 in the decimal system.

 To explain the function of the circuit shown in Figure 3, let it be assumed that the second phase control loop is in the synchronized state, so that it holds that $s_m = s_p = 0$. Let it
35 further be assumed that at a predetermined instant the counter formed by the frequency divider flipflops 201...206 has reached a predetermined counting position. The counting position is then incremented by 1 at

each further period of the oscillator signal, until a counting position is reached which corresponds to the data word 111110 (decimal system : 62). As can be seen from the Table shown in Figure 4 which represents those combinations of $s_6 \dots s_1$, s_m , s_p on which the output signal of the logic combining circuit 218 becomes "1" (this output signal is "0" for all other combinations), the output signal of the logic combining circuit then becomes "1", so that the counter 201...206 is reset to 000010 (decimal system : 2), corresponding to the connection of the set or reset inputs. Then there are no longer the conditions at which the output signal of the logic combining circuit is "1", so that the counter then counts up again to 111110, starting from 000010, whereafter the above-described procedure is repeated. So the counter counts only 60 pulses and a 1 to 0 transition, that is to say a negative edge, appears at the output of the RS-flipflop 217 only once in every 60 pulses, so that the period of the signal at the output 212 corresponds accurately to 120 periods at the input 211.

When in the phase control loop shown in Figure 2 there is a large phase difference between the output signal of the frequency divider 14 and the pilot signal, the comparator 22, for example, responds ($s_m = 1$; $s_p = 0$). In this case the counter 201...206 also counts each pulse, however only until a counting position 111101 (decimal system: 61) has been reached. In this case the period duration at the output 212 is $2 \times (61-2) = 118$ periods of the signal at the input 211. If in contrast with the above-assumed case, the phase difference had the opposite sign, then s_m would be 0 and s_p would be 1. In that case the counter would count to 111111 (decimal system : 63) and the period of the signal at the output 212 would have a duration of 122 periods of the input signal 211.

CLAIMS:

1. A circuit arrangement for a receiver comprising a first phase control loop (7...10) which is synchronized with a reference oscillator and supplies a signal which is applied to a mixer stage which converts the received RF-signal to an intermediate frequency, and a
5 second phase control loop (13...17) which is synchronized by a pilot signal contained in the modulating signal of the received RF-signal, characterized in that the second phase control loop (13...17) incorporates an oscillator (11) whose frequency is electronically controllable and which can be synchronized on the pilot signal, said
10 oscillator constituting the reference oscillator of the first phase control loop (7...10).
2. A circuit arrangement as claimed in Claim 1, characterized in that the frequency of the oscillator (11) is at least substantially an integral multiple of the frequency of the pilot signal.
- 15 3. A circuit arrangement as claimed in any one of the preceding Claims, characterized in that the output of the reference oscillator (11) in the second control loop is connected via a frequency divider (13, 14) to one input of a phase discriminator (15), whose other input receives the pilot signal and whose output is connected via a low-
20 pass filter (17) to the control input of the reference oscillator (11) for controlling its frequency.
4. A circuit arrangement as claimed in Claim 3, characterized in that a switch (16) whose switching state is controlled by a pilot signal detector (18) is arranged between the output of the
25 phase discriminator (15) and the input of the low-pass filter (17).
5. A circuit arrangement as claimed in any one of the preceding Claims, characterized in that the output voltage of the phase discriminator (15) is supplied via a limiter (19).
6. A circuit arrangement as claimed in Claim 5,
30 characterized in that a circuit (20) for changing the frequency divider ratios of the frequency dividers is provided, which is controlled by the output signal of the phase discriminator (15) via a threshold

arrangement (22, 23).

7. A circuit arrangement as claimed in any one of the preceding Claims, characterized in that the reference oscillator (11) is connected to the first phase control loop (7...10) via a frequency
5 divider (12).

8. A circuit arrangement as claimed in any one of the preceding Claims, characterized in that the first phase control loop (7...10) comprises a frequency divider, (8) having an electronically controllable frequency divider ratio.

