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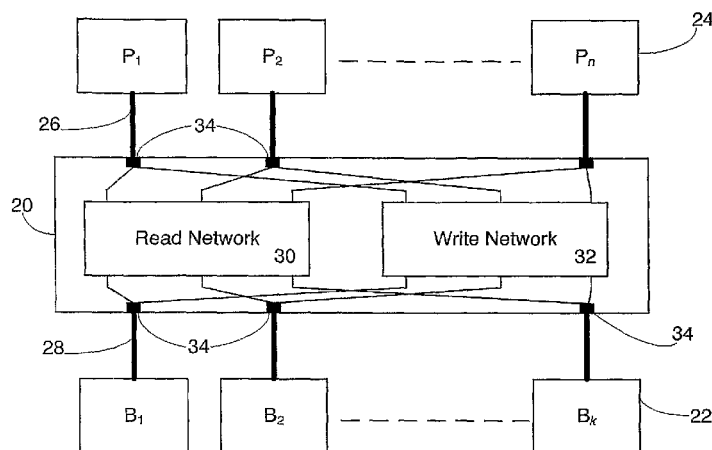


Fig. 2

(57) Abstract: A shared memory system for a multicore computer system utilizing an interconnection network that furnishes tens of processing cores or more with the ability to refer concurrently to random addresses in a shared memory space with efficiency comparable to the typical efficiency achieved when referring to private memories is disclosed. The interconnection network is generally composed of a sub-network for writing and a separate multicasting sub-network for reading. The shared memory system computes paths between processing cores and memory banks anew at every clock cycle, without rearrangement. It returns an approval reply to every core whose initiative of accessing memory leads to the successful establishment of a path and is fulfilled, or a rejection reply to every core whose initiative is not fulfilled.

