CLAIMS

What is claimed is:

1. A method of performing a process on a wafer, comprising:

(a) determining how wafer bow changes with temperature, wherein the wafer bow is at least partially caused by one or more processes performed on a front side of a wafer;

(b) using information about how the determined wafer bow changes with temperature to determine properties of a back side treatment of wafers, which back side treatment counteracts the wafer bow;

(c) applying the back side treatment identified in (b) to an incoming wafer; and

(d) performing the one or more processes on the front side of the incoming wafer, whereby the back side treatment applied in (c) at least partially prevents the incoming wafer from bowing in response to the one or more processes.

2. The method of claim 1, wherein the one or more processes performed on the front side of the wafer comprises a deposition process.

3. The method of claim 1, wherein the one or more processes performed on the front side of the wafer comprises multilayer stack deposition.

4. The method of claim 1, wherein the one or more processes performed on the front side of the wafer comprises oxide/nitride (ONON) deposition.

5. The method of claim 1, wherein the one or more processes performed on the front side of the wafer comprises an etching process.

6. The method of any one of claims 1-5, wherein determining how wafer bow changes with temperature comprises measuring wafer bow of a test wafer at multiple different temperatures while the temperature of the test wafer increases.

7. The method of any one of claims 1-5, wherein determining how wafer bow changes with temperature comprises measuring wafer bow of a test wafer at multiple different temperatures while the temperature of the test wafer decreases.

8. The method of any one of claims 1-5, wherein determining how wafer bow changes with temperature comprises determining a hysteresis of wafer bow in response to at least one cycle of increasing temperature and decreasing temperature.

9. The method of any one of claims 1-5, wherein determining how wafer bow changes with temperature comprises measuring wafer bow of a test wafer at multiple different temperatures within a range of temperatures experienced by the incoming wafer during the one or more processes on the front side of the incoming wafer.

10. The method of any one of claims 1-5, wherein the back side treatment comprises applying one or more layers to the back side of the incoming wafer.

11. The method of any one of claims 1-5, wherein using the information about how the determined wafer bow changes with temperature to determine properties of a back side treatment of the wafer comprises obtaining temperature versus bow information for test wafers having one or more deposited layers on the back sides of the test wafers.

12. The method of claim 11, wherein a first test wafer has a layer of a first material on its back side and a second test wafer has a deposited layer of a second material on its back side.

13. The method of claim 12, wherein using the information about how the determined wafer bow changes with temperature to determine properties of a back side treatment of the wafer further comprises determining a back side treatment that includes:

depositing a first layer of the first material to a first thickness on the wafer's back side, and

depositing a second layer of the second material to a second thickness on the wafer's back side.

14. An apparatus for controlling wafer bow during integrated circuit processing, comprising:

one or more process stations of a multi-station fabrication chamber,

the one or more process stations being configured to receive a corresponding

number of semiconductor wafers having undergone a fabrication process at a back side of each wafer,

the one or more process stations being additionally configured to perform a fabrication process to an active side of each wafer,

the one or more process stations being additionally configured to cooperate with each received semiconductor wafer to maintain wafer bow to a value below a threshold level during the fabrication process performed to the active side of each wafer.

15. The apparatus of claim 14, wherein the fabrication process performed to the active side of each wafer involves elevating the temperature of the wafer followed by reducing the temperature of the wafer.

16. The apparatus of claim 14, wherein the fabrication process performed to the active side of each wafer comprises material deposition.

17. The apparatus of claim 14, wherein the fabrication process performed to the active side of each wafer comprises removal of material from the wafer.

18. The apparatus of any one of claims 14-17, wherein the threshold level corresponds to about 100 μm and wherein each wafer has a diameter of about 300 mm.

19. The apparatus of any one of claims 14-17, wherein the threshold level corresponds to about 75 μm and wherein each wafer has a diameter of about 300 mm.

20. The apparatus of any one of claims 14-17, wherein the multi-station fabrication chamber comprises 4 process stations.

21. The apparatus of any one of claims 14-17, wherein the fabrication process at the back side of each wafer comprises depositing silicon oxide and/or silicon nitride layers.

22. A method of controlling wafer bow in an integrated circuit fabrication process, comprising:

characterizing the wafer bow in response to performing one or more active

fabrication processes to an active side of an integrated circuit wafer;

determining one or more second fabrication processes, to be applied to a back side of the integrated circuit wafer, to bring the wafer bow to below a predetermined threshold based on the one or more active fabrication processes; and

performing the one or more second fabrication processes on the back side of the integrated circuit wafer.

23. The method of claim 22, wherein the one or more active fabrication processes performed to the active side of the integrated circuit wafer comprises elevating the temperature of the integrated circuit wafer.

24. The method of one of claims 22 or 23, wherein the one or more active fabrication processes performed to the active side of the integrated circuit wafer comprises depositing a material on the active side of the integrated circuit wafer.

25. The method of claim 24, wherein the material deposited on the active side of the integrated circuit wafer comprises silicon nitride.

26. The method of claim 24, wherein the material deposited on the active side of the integrated circuit wafer comprises silicon oxide.

27. The method of one of claims 22 or 23, wherein the one or more active fabrication processes performed to the active side of the integrated circuit wafer comprises removing a material from the active side of the integrated circuit wafer.

28. The method of one of claims 22 or 23, wherein performing the one or more second fabrication processes on the back side of the integrated circuit wafer results in decreasing the wafer bow to an amount below 100 μm when the wafer has a diameter of about 300 mm.

29. The method of one of claims 22 or 23, wherein performing the one or more second fabrication processes on the back side of the integrated circuit wafer results in decreasing the wafer bow to an amount below about 75 μm when the wafer has a diameter of about 300 mm.

30. The method of one of claims 22 or 23, wherein performing the one or more second fabrication processes on the back side of the integrated circuit wafer comprises depositing a silicon oxide layer, a silicon nitride layer, or both a silicon oxide and a silicon nitride layer at the back side.