What is Claimed is:

1. A system for achieving correct-by-construction timing closure, the system comprising:

a first semiconductor device having a thin interface module, the thin interface module comprising:

an address register configured to register an address for address interconnects in accordance with an address clock from an address-clock interconnect;

a data register configured to register data for data interconnects in accordance with a data clock from a data-clock interconnect; and

a plurality of bonds disposed on a surface of the first semiconductor device, the plurality of bonds operatively coupled to the address interconnects and the data interconnects, the plurality of bonds configured to interface with a bonded second semiconductor device.

2. The system according to claim 1, wherein the system is configured for achieving correct-by-construction timing closure between the first and second semiconductor devices.

3. The system according to claim 1, wherein the first and second semiconductor devices are face-to-face bonded together or stacked together.

4. The system according to claim 1, wherein the address-clock interconnect and the data-clock interconnect are coupled together to thereby merge the address clock and the data clock.

5. The system according to claim 1, wherein the data register is

a read data register configured to receive read data via the data interconnects; or

a write data register configured to provide write data to the data interconnects.

6. The system according to claim 5, further comprising:

when the data register is a read data register configured to receive read data via the data interconnects, a write data register configured to register write data to provide the write data to a plurality of write data interconnects, wherein the plurality of bonds includes the write data interconnects; or

when the data register is a write data register configured to provide write data to the data interconnects, at least two read data registers configured to receive the read data from a plurality of read data interconnects, wherein the plurality of bonds includes the read data interconnects.

7. The system according to claim 1, the first semiconductor device further comprising:

a read-interface register, wherein the address register and the data register form the read-interface register, the read-interface register configured to register a read address from read interconnects and read data from the read interconnects in accordance with a read clock from a read-clock interconnect, wherein the read interconnects include the address interconnects and the data interconnects, the address clock and the data clock form the read clock, the address-clock interconnect and the data-clock interconnect form the read-clock interconnect;

a write-interface register configured to register a write address and write data from write interconnects in accordance with a write clock from a write-clock interconnect;

a plurality of read bonds disposed on a surface of the first semiconductor device, the plurality of read bonds operatively coupled to the read interconnects of the read-interface register, wherein the plurality of bonds includes the plurality of read bonds; and

a plurality of write bonds disposed on the surface of the first semiconductor device, the plurality of write bonds operatively coupled to the write interconnects of the write-interface register.

8. The system according to claim 7, the system further comprising:

the second semiconductor device comprising:

a read peripheral having a read-peripheral interconnects coupled to the surface of the second semiconductor device and configured to couple to the plurality of read bonds to thereby couple the read peripheral of the second semiconductor device to the read-interface register of the first semiconductor device; or

a write peripheral having a write-peripheral interconnects coupled to the surface of the second semiconductor device and configured to couple to the plurality of write bonds to thereby couple the write peripheral of the second semiconductor device to the write-interface register of the first semiconductor device.

9. The system according to claim 7, wherein the read interconnects comprise:

read-address interconnects; and

read-data interconnects.

10. The system according to claim 9, wherein the plurality of read bonds comprises:

a plurality of read-address bonds disposed on a surface of the first semiconductor device, the plurality of read-address bonds operatively coupled to the read-address interconnects of the read-interface register; and

a plurality of read-data bonds disposed on the surface of the first semiconductor device, the plurality of read-data bonds operatively coupled to the read-data interconnects of the read-interface register,

optionally,

wherein the plurality of bonds includes a read-clock bond, and wherein the read-clock interconnect couples the read-clock bond to the read-interface register.

11. The system according to claim 7, wherein the write interconnects comprise:

write-address interconnects; and

write-data interconnects.

12. The system according to claim 11, wherein the plurality of write bonds comprises:

a plurality of write-address bonds disposed on the surface of the first semiconductor device, the plurality of write-address bonds coupled to the write-address interconnects of the write-interface register; and

a plurality of write-data bonds disposed on the surface of the first semiconductor device, the plurality of write-data bonds coupled to the write-data interconnects of the write-interface register,

optionally,

wherein the plurality of bonds includes a write-clock bond, and wherein the write-clock interconnect couples the write-clock bond to the write-interface register.

13. A method for forming a first semiconductor device having correct-by-construction timing closure, the method comprising:

forming a thin interface module on a base die;

forming an address register in the thin interface module, the address register configured to register an address for address interconnects in accordance with an address clock from an address-clock interconnect;

forming a data register in the thin interface module, the data register configured to register data for data interconnects in accordance with a data clock from a data-clock interconnect;

forming a plurality of bonds disposed on a surface of the first semiconductor device, the plurality of bonds operatively coupled to the address interconnects and the data interconnects; and

bonding the plurality of bonds with a second semiconductor device.

14. The method according to claim 13, further comprising forming the thin interface module in spaced relation that is less than a predetermined distance to the plurality of bonds

thereby achieving correct-by-construction timing closure between the first and second semiconductor devices.

15. The method according to claim 13,

wherein the act of bonding the plurality of bonds with the second semiconductor device comprises face-to-face bonding or stacking the first semiconductor device to the second semiconductor device.

16. The method according to claim 13,

wherein the act of forming the thin interface module on the base die comprises forming the thin interface module under the plurality of bonds; or

wherein the act of forming the plurality of bonds comprises forming the plurality of bonds over the thin interface module; or

wherein the forming acts are implemented in accordance with a netlist.

17. The method according to claim 13, the method further comprising forming the plurality of bonds and the address register in spaced relation to each other such that communication between the plurality of bonds and the address register is less than a predetermined amount of time.

18. The method according to claim 13, further comprising vertically wiring the address interconnects and the data interconnects to the plurality of bonds.

19. The method according to claim 13, further comprising bonding or stacking the first and second semiconductor devices together, optionally wherein the bonding is face-to-face bonding.

20. The method according to claim 13, further comprising merging the address-clock interconnect and the data-clock interconnect together to thereby merge the address clock and the data clock.

21. The method according to claim 13, further comprising

receiving read data via the data interconnects, wherein the data register is a read data register; and

optionally,

registering write data into a write data register; and providing the write data to a plurality of write data interconnects, wherein the plurality of bonds includes the write data interconnects.

22. The method according to claim 13, further comprising

providing write data to the data interconnects, wherein the data register is a write data register; and

optionally,

receiving first read data in a first read data register from a first memory module on the second semiconductor device; and receiving second read data in a second read data register from a second memory module on the second semiconductor device.

23. The method according to claim 13, wherein the first semiconductor device further comprising:

a read-interface register, wherein the address register and the data register form the read-interface register, the read-interface register configured to register a read address from read-address interconnects and read data from the read interconnects in accordance with a read clock from a read-clock interconnect, wherein the read interconnects include the address interconnects and the data interconnects, the address clock and the data clock form the read clock, the address-clock interconnect and the data-clock interconnect form the read-clock interconnect;

a write-interface register configured to register a write address and write data from write interconnects in accordance with a write clock from a write-clock interconnect;

a plurality of read bonds disposed on a surface of the first semiconductor device, the plurality of read bonds operatively coupled to the read interconnects of the read-interface register, wherein the plurality of bonds includes the plurality of read bonds; and

a plurality of write bonds disposed on the surface of the first semiconductor device, the plurality of write bonds operatively coupled to the write interconnects of the write-interface register.

24. The method according to claim 23, wherein the second semiconductor device comprises

a read peripheral having read-peripheral interconnects coupled to the surface of the second semiconductor device and configured to couple to the plurality of read bonds to thereby couple the read peripheral of the second semiconductor device to the read-interface register of the first semiconductor device; or

a write peripheral having write-peripheral interconnects coupled to the surface of the second semiconductor device and configured to couple to the plurality of write bonds to thereby couple the write peripheral of the second semiconductor device to the write-interface register of the first semiconductor device.

25. The method according to claim 23, wherein the read interconnects comprise:

read-address interconnects; and

read-data interconnects.

26. The method according to claim 23, wherein the plurality of read bonds comprises:

a plurality of read-address bonds disposed on a surface of the first semiconductor device, the plurality of read-address bonds operatively coupled to the read-address interconnects of the read-interface register; and

a plurality of read-data bonds disposed on the surface of the first semiconductor device, the plurality of read-data bonds operatively coupled to the read-data interconnects of the read-interface register,

optionally,

wherein the plurality of bonds includes a read-clock bond, and wherein the read-clock interconnect couples the read-clock bond to the read-interface register.

27. The method according to claim 23, wherein the write interconnects comprise:

write-address interconnects; and

write-data interconnects.

28. The method according to claim 27, wherein the plurality of write bonds comprises:

a plurality of write-address bonds disposed on the surface of the first semiconductor device, the plurality of write-address bonds coupled to the write-address interconnects of the write-interface register; and

a plurality of write-data bonds disposed on the surface of the first semiconductor device, the plurality of write-data bonds coupled to the write-data interconnects of the write-interface register,

optionally,

wherein the plurality of bonds includes a write-clock bond, and wherein the write-clock interconnect couples the write-clock bond to the write-interface register.

29. A method of using the system according to one of claim 1-12, comprising:

providing the address to the address register; and clocking the address clock to thereby load the address register with the address,

or

providing the data to the data register; and clocking the data clock to thereby load the data register with the data.

30. A system for achieving correct-by-construction timing closure, the system comprising:

a first semiconductor means for providing a thin interface module on a base die, the thin interface module comprising:

an address means for registering an address for address interconnects in accordance with an address clock from an address-clock interconnect;

a data means for registering data for data interconnects in accordance with a data clock from a data-clock interconnect; and

a plurality of bonding means for communicating with a second semiconductor device via address interconnect means and the data interconnect means.