

A method of and apparatus for reducing priming and sweep-out losses in SCR switching circuits

Technical field of the invention

This invention relates to a method of and apparatus for reducing priming and carrier sweep-out losses in silicon-controlled rectifier switching circuits, hereinafter referred to as SCR switching circuits.

5 Background art

In conventional current pulse generators of the SCR type, the magnitude and pulse width of the generated current pulses are limited by the maximum di/dt rating, the electrical on-state conductivity, the thermal junction conductivity, the thermal junction capacitance, and the peak junction temperature.

For sinusoidal current pulses, the (di/dt) maximum is given by the relationship

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$$\left(\frac{di}{dt} \right)_{\max} = \pi \frac{I_{\text{peak}}}{T}$$

(1)

15 where T is the width of the current pulse and I_{peak} its peak current value.

In pulse applications, the SCR junction heats up during the pulse generation interval and then cools down in the interval between pulses. Thus, the junction temperature consists of a DC component and an AC ripple component. If the pulse width is much larger than the thermal time-constant, then the AC ripple component is much larger than the DC component, resulting in a considerable decrease in the
20 heat flow from the junction for a given maximum junction temperature, since the heat flow is proportional to the difference between the average junction temperature and the ambient. As a result, the RMS current rating of the device is reduced. If the pulse width is much smaller than the thermal time-constant, on the other hand, then the ripple component is small compared to the DC component and the junction operates at its maximum rated temperature continuously, with no decrease in heat
25 flow resulting. Thus, the maximum RMS current rating of the SCR can be realized. The maximum pulse repetition rate is determined by the allowable RMS current, such that the peak junction temperature is not exceeded.

This discussion, however, has ignored a significant source of heat dissipation in the junction that is associated with the reverse recovery characteristic of the SCR. At the end of the current pulse,
30 minority carriers are stored in the junction and these carriers conduct current in the reverse direction of the SCR. The minority carriers act like stored charge and are completely removed from the junction when the sum of the integral of the reverse current and the minority carrier recombination charge is equal to the initial minority carrier charge. The reverse current, in turn, generates a reverse voltage drop across the junction which can be appreciable during the recovery interval. Thus, considerable heat
35 dissipation may occur during the reverse recovery interval; and this loss increases with decreasing pulse width. The RMS current rating thus decreases with decreasing pulse width.

An object of the present invention is to provide a novel method of and apparatus for greatly decreasing these reverse recovery losses in the SCR.

The basic reason for the limited di/dt rating of an SCR is that, upon application of a gate signal,
40 only a small area of the junction is actually turned on. If the external circuit forces the SCR to conduct too much current through this small area, localized junction temperature rise burns it out. The mechanism of turn-on is characterized by a finite spreading velocity of the order of 30 to 80 m/second. In other words, initially, only the junction area near the gate structure is turned on; then the turned-on
45 area spreads out from the periphery of the gate structure with a speed referred to as the spreading velocity. If complicated gate structures are used, the total spreading distance can be made small such that total turn-on can be achieved in 10 to 20 μsec . This complicated gate structure, however, decreases the junction area thereby decreases the current capability of the device.

Because of the spreading effect in the turn-on mechanism, the junction area that is turned on increases with time. This, in turn, increases the di/dt capability of the device with time. Thus, one way of
50 increasing the di/dt rating of the SCR is to delay the anode current pulse, as by means of a network in series with the SCR, preferably of the saturable inductor type. This saturable inductor acts like a time delaying switch. When the SCR trigger signal is applied, the saturable inductor is in its unsaturated state, and thus represents a high impedance. Only a small amount of current can then flow in the circuit. During this initial time interval, the voltage applied to the saturable inductor drives it toward
55 saturation, at which time the inductor becomes a low impedance, and the full anode current can start to flow. The time of saturation is determined by the core cross-sectional area and the number of turns on the inductor.

Such use of a saturable inductor as a time-delaying switching means has been extensively used in the past to increase the di/dt rating of an SCR—this technique being referred to as "priming".

60 In United States Patent Specification No. 3 958 137 there is disclosed a thyristor circuit for generating a pulse current which has a bypass circuit of a predetermined impedance and which is placed in parallel to a saturable reactor. In this manner a small current is passed through the by-pass

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circuit during the unsaturated period of the saturable reactor so as to saturate the saturable reactor after enlarging the turn-on region of the thyristor to pass a pulse current having a high di/dt . As will later be made evident, however, the priming networks inherently introduce dissipation losses.

A further object of the invention, accordingly, is to provide a novel method and apparatus that greatly reduce, and indeed may substantially eliminate, such priming losses.

The before-mentioned reverse current generation of a reverse voltage drop across the SCR junction also may produce considerable heat dissipation during the reverse recovery interval. So-called "sweep-out" circuits, including inductors, for limiting the reverse current, still result in dissipation of energy associated with the minority carrier sweep-out process as later more fully explained.

An additional object of the invention is to provide a new and improved method of and apparatus for appreciably reducing and even substantially eliminating such dissipated minority carrier sweep-out losses, as well.

Other and further objects will be explained hereinafter and are more fully delineated in the appended claims.

Disclosure of the invention

In summary, from one of its important aspects, the invention embraces a method of reducing priming and carrier sweep-out losses in SCR switching circuits associated with power supplies in which energy is stored in response to such switching, the rise of SCR current upon such switching is delayed for a predetermined priming interval, thereby also generating additional minority carriers in the SCR, and the current is limited during the priming interval, said method comprising thereafter generating a reverse voltage to effect sweep-out of such minority carriers during a sweep-out interval, limiting the current during the sweep-out interval and transferring the energy resulting in priming and sweep-out apparatus in each of said priming and sweep-out intervals back to said power supplies to reduce heat dissipation of the said resulting energy.

Preferred details are hereinafter set forth.

The invention will now be described, by way of example, with reference to the accompanying drawings.

Brief description of the drawings

Figure 1 of which is an explanatory graph of the current vs. time characteristics of an SCR;

Figure 2 is a circuit diagram of circuit apparatus for an SCR priming and minority carrier sweep-out functions;

Figure 3 is a graph of SCR current waveforms resulting from the circuit of Figure 2;

Figure 4 is a circuit diagram of a preferred apparatus constructed in accordance with the invention and involving the novel method thereof;

Figures 5 and 6 are respectively SCR current and inductor voltage waveforms generated in the apparatus of Figure 4;

Figure 7 is a circuit diagram of a modification; and

Figures 8(a) and (b) are waveforms bearing upon the circuit of Figure 7.

Best mode for carrying out the invention

In order more fully to explain the principles underlying the invention, reference will first be made to the graphs of Figure 1 illustrating the turn-on characteristics of an SCR with and without priming; anode current being plotted along the ordinate, and time along the abscissa. The curve labeled A represents the maximum allowable rate-of-rise (di/dt) or anode current as a function of time. To compare the relative increase in anode current that can be achieved with and without priming, three additional current waveforms are sketched in Figure 1. Curve B represents a sinusoidal anode current, say, of 5 μ sec width with no priming. The peak magnitude of this current pulse is determined by the di/dt rating at time zero. Curve C, on the other hand, represents the anode current with a priming time ($o-t$), of 5 μ sec. It will be noted that a small amount of anode current flows during the priming interval. By increasing the anode current during such priming interval, further increase in the di/dt rating can be obtained; and this increase, in turn, increases the peak anode current, as is evident from Curve D. The anode current during the priming interval generates additional minority carriers in the turned-on junction area and thereby permits increased di/dt rating; though this anode current does not, however, increase the junction turned-on area. Such area is strictly a function of the time duration of the priming interval. Additional minority carriers in the turned-on area permit an increase in the anode current. Thus, the di/dt rating depends upon two parameters: the time duration of the priming interval, and the magnitude of the anode current during this interval.

A priming and minority carrier sweep-out circuit is shown in Figure 2, comprising a saturable inductor L1 with a square-loop core, a tapped primary winding P, a bias or reset winding B, and a secondary winding S shunted by a pair of diodes CR1 and CR2, respectively in series with adjustable resistors R1 and R2. For a fixed anode current, these adjustable components are set to the optimum values. This priming and sweep-out circuit is connected with the primary winding P of the saturable

inductor L1 in series between the +terminal of the power supply E_{DC} and the SCR, and a resonant charging inductor L2 then series-connects the SCR to the +terminal of a shunt storage capacitor C_1 .

The priming interval time duration is adjusted by selecting different taps on the primary winding P. During the priming interval, the voltage across the saturable inductor is positive and diode CR1 conducts. The amplitude of the priming current is adjusted by means of resistor R1. During the reverse recovery interval, the inductor voltage is negative so that diode CR2 conducts. The reverse recovery current is adjusted by means of resistor R2. In many applications, the resistance values of R1 and R2 are almost the same; and in these cases, the secondary circuit may consist only of one resistor. For high-frequency operation particularly, the priming loss dissipated in R1 is appreciable.

The before-mentioned reverse recovery characteristic of the SCR is shown in Figure 3. Without the priming and sweep-out circuit, the reverse current I_A builds up to a large peak value, as illustrated in Curve A of Figure 3. Since this reverse current flows through the charging inductor L2 of Figure 2 and the saturated inductance of L1, a considerable amount of energy is stored in these inductors and this energy dissipates in the SCR during reverse recovery. Such reverse current may cause two types of failures: one due to excess power dissipation; and the other due to reverse voltage breakdown. The sweep-out feature of this circuit, however, limits the reverse current to a value controlled by the resistor R2, as shown by Curve B in Figure 3. The optimum value of R2 is obtained when the current I_b is minimized. The square-loop core allows the SCR turnoff to be controlled by limiting the reverse-current pulse to a safe value. An additional bias current is generally applied to the square-loop core in the reset direction to insure core reset, in the event that the SCR's recombination process is completed prior to reverse saturation.

In the circuit of Figure 2, the resonant charging generates a voltage across C_1 that approaches twice the supply voltage E_{DC} in magnitude. The net voltage that sweeps out the minority carriers is therefore of the same magnitude as E_{DC} . The inductor L1 limits the reverse current to the value I_b shown in Figure 3. This low reverse current value generates a reverse voltage drop across the SCR junction of only a few volts, and the inductor L1 absorbs most of the reverse voltage. Thus, the energy associated with the minority carrier sweep-out process is dissipated in resistor R2 connected across the secondary windings of inductor L1. Again, for high-frequency operation, this energy loss is appreciable.

As before stated a primary objective of this invention is to substantially eliminate both the priming loss dissipated in resistor R1 and the minority carrier sweep-out loss dissipated in resistor R2. The illustrative circuit of Figure 4 is constructed in accordance with the invention to provide such low loss priming and minority carrier sweep-out. The circuit comprises a pair of successive saturable inductors L1 and L2 having respective primary, bias and secondary windings P—B—S and P'—B'—S', with diodes CR1 and CR2, linear inductor L3, resistor R1 and a DC bias supply; so-labelled. The primary windings P and P' are connected in series with SCR1. The bias windings B and B' are connected in series with L3, R1 and the DC bias supply. The secondary winding S of L1 is connected in series with diode CR1; and the secondary winding S' of L2 is connected in series with diode CR2. The operation of the circuit of Figure 4 will now be described with the aid of the waveforms of Figures 5 and 6.

Initially, the C_1 voltage is zero and L1 and L2 have been properly reset by the bias current, I_b . Such bias current drives L1 into negative saturation and L2 into positive saturation. Thus, when SCR1 is turned on at time t_0 , Figures 5 and 6, the inductor L1 is driven into its unsaturated region, thereby limiting the priming current to the value

$$(I_{SCR})_{\text{priming}} = \frac{n_{bl}}{n_{pl}} I_b + I_{ml}$$

where:

n_{bl} = number of bias winding turns B on L1,

n_{pl} = number of primary winding turns P on L1 and

I_{ml} = magnetizing current of L1.

This priming current flows during the time-interval t_0 to t_1 in Figure 5. During this time-interval, the L1 core is driven from negative to positive saturation by the voltage E_{DC} . The inductor L2, on the other hand, is driven further into positive saturation by the current I_{SCR} . At time t_1 , inductor L1 saturates positively, and a large sinusoidal charging current starts to flow. The frequency, or period, of this current pulse is determined by the saturated inductances of L1 and L2 and the capacitance C_1 .

At time t_2 , capacitor C_1 is fully charged and the SCR1 current (I_{SCR}) reverses polarity, thus initiating the minority carrier sweep-out process. When the SCR1 current reverses polarity, the bias current I_b starts to drive the L1 core into negative saturation. This generates a negative voltage across the L1 windings limited by the E_{DC} voltage and the number of secondary turns on S, through the clamping action of CR1. The number of secondary winding turns S is selected such that the clamping voltage appearing across the primary winding P of L1 is slightly less than the sweep-out voltage. That is,

$$E_{\text{sweep-out}} = (E_{C1})_{\text{peak}} - E_{DC} \quad (3)$$

Thus, the remaining part of the sweep-out voltage appears across L2.

The voltage waveforms across L1 and L2 are shown in Figure 6. Since the SCR1 sweep-out current is of the same polarity as the bias current for inductor L1, the sweep-out current aids the bias current in resetting L1. Further, since these two currents cause CR1 to conduct, there is no current-limiting function provided by L1 for the SCR1 sweep-out current. During this sweep-out process, however, inductor L2 provides the current-limiting function necessary to protect the SCR from failure. The SCR1 sweep-out current drives inductor L2 from positive toward negative saturation, with the sweep-out current being given by the expression:

$$(i_{SCR})_{\text{sweep-out}} = \frac{n_{b2}}{n_{p2}} i_b + i_{m2} \quad (4)$$

where:

n_{b2} = number of bias winding turns B' on L2,
 n_{p2} = number of primary winding turns P' on L2, and
 i_{m2} = magnetizing current of L2.

Thus, as seen from Equations (2) and (4) above, the priming current and the sweep-out current can be independently adjusted in magnitude by the number of turns on the two bias windings B and B'; namely, n_{b1} and n_{b2} .

At time t_3 , the sweep-out process is complete, and the reverse voltage is absorbed by SCR1. When the sweep-out current drops to a low value (time t_3 in Figure 5), the bias current drives the core of L2 back into positive saturation and by this action generates a positive voltage across the L2 primary winding P'. This voltage is clamped to the voltage E_{DC} by means of the secondary winding S' and the diode CR2. Without this clamping action, the bias current would generate a large voltage spike across L1, thereby exceeding the voltage rating of the SCR and causing SCR failure.

In the circuit of Figure 4, therefore, the energy associated with the priming and sweep-out processes is transferred back to the power supply by means of the L1 secondary winding S and CR1. During the priming time-interval, t_0 to t_1 , the energy absorbed by L1 is actually transferred into the bias circuit, thus eliminating the losses of prior art priming circuits. During this interval, the L1 voltage is positive, thereby increasing the bias current and the stored energy in L3. Since R1 has a small resistance value, the additional losses in R1 are negligible. During the sweep-out time-interval, this additional energy stored in L3 is transferred to the power supply together with the energy associated with the sweep-out process, providing for the elimination of the prior art losses attendant upon such sweep-out operation, also.

A modified circuit for attaining these novel results is shown in Figure 7, such circuit having novel advantages even apart from the priming and sweep-out features. This circuit generates both negative and positive sinusoidal current pulses, as shown in Figure 8(a). The circuit consists of capacitors C1 and C2; thyristor SCR1 in series with the first low loss priming and recovery circuit comprising inductors L1 and L2, diodes CR3 and CR5; thyristor SCR2 in series with a second low loss priming and recovery circuit comprising inductors L3 and L4, diodes CR4 and CR6; a DC bias supply with series elements R1 and L5; and a clamping circuit consisting of diodes CR1 and CR2, and transformer T1. The operation of the circuit is as follows. Initially, at time t_0 , Figure 8(b), capacitor C1 is charged positively and capacitor C2 negatively. At time t_0 , SCR1 is turned on, and a positive half sine-wave of current (i_1) is generated and delivered to the load during the time interval t_0 to t_1 . At time t_1 , both voltages on C1 and C2 have been reversed, such that the C2 voltage is positive (e_{c2}) and the C1 voltage is negative (e_{c1}). The next time interval, t_1 to t_2 , must be sufficiently long to insure that SCR1 recovers. At time t_2 , SCR2 is turned on, and a negative half-sine-wave of current (i_2) is generated and delivered to the load during the time interval t_2 to t_3 . At time t_3 , both voltages on C1 and C2 have been reversed, returning to the initial voltage polarities at time t_0 . In the time interval t_3 to t_4 , SCR2 recovers, and at time t_4 , a new cycle of operation is initiated.

The relation between the forward and reverse capacitor voltages depends on the load characteristic. For a resistive load, energy is delivered to the load. Thus, for this case, the reverse capacitor voltage is less than the forward voltage, and this difference in capacitor voltage reflects the energy delivered to the load. For a regenerative load in which energy is delivered from the load to the pulse generator, on the other hand, the reverse capacitor voltage is greater than the forward voltage. For this last case, dangerous high voltages may be generated in the pulse generator circuit that may exceed the SCR maximum voltage rating. The clamping circuit (transformer T1 and oppositely poled diodes CR1 and CR2) eliminates these high voltages and thereby permits safe operation into regenerative loads.

When the load is resistive, the voltage at this common point is a symmetrical flat-topped wave shown as e_1 in Figure 8(b). This voltage increases in magnitude when the load becomes reactive or regenerative. Even for a resistive load, the magnitude of the voltage e_1 exceeds the D.C. supply voltage E_{DC} . In order to clamp the e_1 voltage to a desired value, a secondary winding S is added to transformer

T1. The turns ratio between the primary and secondary windings P and S is selected such that the secondary winding voltage is equal to one half the D.C. supply voltage (E_{DC}) when e_1 is equal to the desired clamping voltage. If e_1 increases beyond this value, either of the diodes CR1 and CR2 (depending upon voltage polarity) conducts and thus transfers energy back to the power supply. Thus, the voltage e_1 cannot exceed the clamping voltage level.

Further modifications will also occur to those skilled in this art, and all such are considered to fall within the spirit and scope of the invention as defined in the appended claims.

Claims

1. A method of reducing priming and carrier sweep-out losses in SCR switching circuits associated with power supplies in which energy is stored in response to such switching, the rise of SCR current upon such switching is delayed for a predetermined priming interval, thereby also generating additional minority carriers in the SCR, and the current is limited during the priming interval, characterised by thereafter generating a reverse voltage to effect sweep-out of such minority carriers during a sweep-out interval, limiting the current during the sweep-out interval, and transferring the energy resulting in priming and sweep-out apparatus in each of said priming and sweep-out intervals back to said power supplies to reduce heat dissipation of the said resulting energy.

2. A method as claimed in Claim 1, characterised in that said delaying, generating and transferring are effected by saturable inductive field reversals.

3. An SCR switching-circuit priming and sweep-out apparatus having, in combination with power supply means adapted to store energy in response to SCR switching, saturable inductance means interposed between the power supply means and SCR means, characterised by part (B) of the saturable inductance means (L_1, L_2) being adjusted to provide limited priming current during a predetermined priming interval following switching of the SCR means (SCR1) and part (B') of said saturable inductance means (L_1, L_2) being adjusted upon reverse of said switching to provide a limited sweep-out current; and means (CR1) connected with said saturable inductance means for transferring back to said power supply means (E_{DC}) energy resulting from the providing of said priming and sweep-out currents to reduce heat dissipation of the same in said circuit.

4. Apparatus as claimed in Claim 3, characterized in that said saturable inductance means comprises a pair of successive saturable inductors (L_1, L_2) each having primary, bias and secondary windings and with the primary windings (P, P') connected in series with the SCR means (SCR1), the bias windings (B, B') connected in series to a bias part of said power supply means, and the secondary windings (S, S') connected in series with oppositely poled diode means (CR1, CR2).

5. Apparatus as claimed in Claim 4, characterized in that means is provided for adjusting one of the pair of saturable inductors (L_1, L_2) to limit the said priming current substantially in accordance with the expression

$$(i_{SCR})_{\text{priming}} = \frac{n_{b1}}{n_{p1}} i_b + i_{m1}$$

where n_{b1} represents the number of turns on its bias winding (B), n_{p1} represents the number of turns on its primary winding (P), i_{m1} represents the inductor magnetizing current and i_b represents the bias current; and in which said secondary winding (S) of said one of the pair of saturable inductors assists in limiting the said priming current.

6. Apparatus as claimed in Claim 5, characterized in that means is provided for adjusting the other of the pair of saturable inductors (L_1, L_2) to limit the said sweep-out current substantially in accordance with the expression

$$(i_{SCR})_{\text{sweep-out}} = \frac{n_{b2}}{n_{p2}} i_b + i_{m2}$$

where n_{b2} represents the number of turns on its bias winding (B'), n_{p2} represents the number of turns on its primary winding (P'), i_{m2} represents the inductor magnetizing current and i_b represents the bias current; and in which said secondary winding (S') of said other of the pair of saturable inductors assist in current limiting to protect the SCR means.

7. Apparatus as claimed in Claim 6, characterized in that means comprising the turns of the respective bias windings (B, B') of the pair of saturable inductors is provided for enabling independent adjustment of the magnitude of the priming and sweep-out currents, respectively.

8. Apparatus as claimed in Claim 6, characterized in that said bias windings (B, B') are connected in series with a resonant charging inductance with said bias part of the power supply means.

9. Apparatus as claimed in Claim 3, connected to feed a regenerative load wherein the energy transferred back to said power supply may exceed the SCR maximum voltage rating, characterized by



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T1. The turns ratio between the primary and secondary windings P and S is selected such that the secondary winding voltage is equal to one half the D.C. supply voltage (E_{DC}) when e_i is equal to the desired clamping voltage. If e_i increases beyond this value, either of the diodes CR1 and CR2 (depending upon voltage polarity) conducts and thus transfers energy back to the power supply. Thus, the voltage e_i cannot exceed the clamping voltage level.

Further modifications will also occur to those skilled in this art, and all such are considered to fall within the spirit and scope of the invention as defined in the appended claims.

Claims

1. A method of reducing priming and carrier sweep-out losses in SCR switching circuits associated with power supplies in which energy is stored in response to such switching, the rise of SCR current upon such switching is delayed for a predetermined priming interval, thereby also generating additional minority carriers in the SCR, and the current is limited during the priming interval, characterised by thereafter generating a reverse voltage to effect sweep-out of such minority carriers during a sweep-out interval, limiting the current during the sweep-out interval, and transferring the energy resulting in priming and sweep-out apparatus in each of said priming and sweep-out intervals back to said power supplies to reduce heat dissipation of the said resulting energy.

2. A method as claimed in Claim 1, characterised in that said delaying, generating and transferring are effected by saturable inductive field reversals.

3. An SCR switching-circuit priming and sweep-out apparatus having, in combination with power supply means adapted to store energy in response to SCR switching, saturable inductance means interposed between the power supply means and SCR means, characterised by part (B) of the saturable inductance means (L_1, L_2) being adjusted to provide limited priming current during a predetermined priming interval following switching of the SCR means (SCR1) and part (B') of said saturable inductance means (L_1, L_2) being adjusted upon reverse of said switching to provide a limited sweep-out current; and means (CR1) connected with said saturable inductance means for transferring back to said power supply means (E_{DC}) energy resulting from the providing of said priming and sweep-out currents to reduce heat dissipation of the same in said circuit.

4. Apparatus as claimed in Claim 3, characterized in that said saturable inductance means comprises a pair of successive saturable inductors (L_1, L_2) each having primary, bias and secondary windings and with the primary windings (P, P') connected in series with the SCR means (SCR1), the bias windings (B, B') connected in series to a bias part of said power supply means, and the secondary windings (S, S') connected in series with oppositely poled diode means (CR1, CR2).

5. Apparatus as claimed in Claim 4, characterized in that means is provided for adjusting one of the pair of saturable inductors (L_1, L_2) to limit the said priming current substantially in accordance with the expression

$$(i_{SCR})_{\text{priming}} = \frac{n_{b1}}{n_{p1}} i_b + i_{m1}$$

where n_{m1} represents the number of turns on its bias winding (B), n_{p1} represents the number of turns on its primary winding (P), i_{m1} represents the inductor magnetizing current and i_b represents the bias current; and in which said secondary winding (S) of said one of the pair of saturable inductors assists in limiting the said priming current.

6. Apparatus as claimed in Claim 5, characterized in that means is provided for adjusting the other of the pair of saturable inductors (L_1, L_2) to limit the said sweep-out current substantially in accordance with the expression

$$(i_{SCR})_{\text{sweep-out}} = \frac{n_{b2}}{n_{p2}} i_b + i_{m2}$$

where n_{b2} represents the number of turns on its bias winding (B'), n_{p2} represents the number of turns on its primary winding (P'), i_{m2} represents the inductor magnetizing current and i_b represents the bias current; and in which said secondary winding (S') of said other of the pair of saturable inductors assist in current limiting to protect the SCR means.

7. Apparatus as claimed in Claim 6, characterized in that means comprising the turns of the respective bias windings (B, B') of the pair of saturable inductors is provided for enabling independent adjustment of the magnitude of the priming and sweep-out currents, respectively.

8. Apparatus as claimed in Claim 6, characterized in that said bias windings (B, B') are connected in series with a resonant charging inductance with said bias part of the power supply means.

9. Apparatus as claimed in Claim 3, connected to feed a regenerative load wherein the energy transferred back to said power supply may exceed the SCR maximum voltage rating, characterized by



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said apparatus being further provided with transformer means (T1) the primary winding (P) of which connects to the load and the secondary winding (S) to oppositely poled diode means (CR1, CR2) connected to the power supply means E_{DC} to clamp such excessive energy and permit safe operation into the regenerative load.

5 10. Apparatus as claimed in Claim 9, characterized in that said power supply means comprises a pair of oppositely poled power supplies (E_{DC}) having a pair of series connected capacitors (C1, C2) connected therebetween, and said primary winding (P) connects to the point of series connection of the capacitors, and said diode means (CR1, CR2) are series-connected across said capacitors with the point of series connection of the diode means being connected to said secondary winding (S).

10 11. An SCR switching-circuit comprising an SCR switching-circuit priming and sweep-out apparatus according to Claim 3, characterized by a pair of oppositely poled power supplies (E_{DC}) provided with a pair of series-connected capacitors (C1, C2) connected therebetween for storing energy in response to SCR switching, a regenerative load connected to receive the stored energy and wherein the energy may exceed the SCR maximum voltage rating, and means for clamping excess
15 energy to permit safe operation comprising transformer means (T1) the primary winding (P) of which connects to the point of series connection of the capacitors and to the load, and series connected across said capacitors with the point of series connection of the diode means being connected to a secondary winding (S) of the transformer means.

20 Patentansprüche

1. Verfahren zur Verringerung der Vorspann- und Trägerabastverluste in siliziumgesteuerten Gleichrichter-Schaltstromkreisen, die mit Netzteilen verbunden sind, in welchen in Abhängigkeit von
25 einer Schaltung Energie gespeichert wird, wobei der Gleichrichterstrom bei einer Schaltung über ein vorbestimmtes Vorspannintervall verzögert wird und dadurch in den Gleichrichter auch zusätzliche Minoritätsträger erzeugt werden, und wobei der Strom während dieses Vorspannintervalls begrenzt wird, dadurch gekennzeichnet, daß anschließend eine Umkehrspannung erzeugt wird, um die Minoritätsträger während eines Abastintervalls abzutasten, wobei der Strom während dieses Abastintervalls begrenzt wird, und daß die während der Vorspann- und Abastintervalle in den Vorspann- und Abastereinrichtungen resultierende Energie zurück an die Netzteile übertragen wird, um eine Wärmeableitung der resultierenden Energie zu verringern.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Verzögerung, die Erzeugung und die Rückübertragung durch sättigungsfähige induktive Feldumkehrungen bewirkt werden.

35 3. Einrichtung zum Vorspannen und Abtasten eines siliziumgesteuerten Gleichrichter-Schaltstromkreises, der mit Netzteilen verbunden ist, in welchen in Abhängigkeit von einer Schaltung des Gleichrichters Energie gespeichert wird, mit einer zwischen die Netzteile und den Gleichrichter geschalteten sättigungsfähigen Induktivitätseinrichtung, dadurch gekennzeichnet, daß ein erster Teil (B) der sättigungsfähigen Induktivitätseinrichtung (L_1 , L_2) für die Bereitstellung eines begrenzten
40 Vorspannstromes während eines auf die Schaltung des Gleichrichters (SCR1) folgenden vorbestimmten Vorspannintervalls und ein zweiter Teil (B') der sättigungsfähigen Induktivitätseinrichtung (L_1 , L_2) für die Bereitstellung eines begrenzten Abtaststromes nach der Umkehrung der Schaltung eingestellt ist, und daß mit der sättigungsfähigen Induktivitätseinrichtung eine Einrichtung (CR1) verbunden ist, durch welche die aus der Bereitstellung der Vorspann- und Abtastströme resultierende Energie an die Netz-
45 teile (E_{DC}) rückübertragen wird, um die Wärmeableitung der Energie in dem Schaltstromkreis zu verringern.

4. Einrichtung nach Anspruch 3, dadurch gekennzeichnet, daß die sättigungsfähige Induktivitätseinrichtung zwei aufeinanderfolgend sättigungsfähige Induktoren (L_1 , L_2) umfaßt, von denen jeder Primär-, Vorspannungs- und Sekundärwicklungen aufweist, von denen die Primärwicklungen (P, P') in
50 Reihe mit dem Gleichrichter (SCR1), die Vorspannungswicklungen (B, B') in Reihe mit einem Vorspannungsteil der Netzteile und die Sekundärwicklungen (S, S') in Reihe mit entgegengesetzt gepolten Dioden (CR1, CR2) verbunden sind.

5. Einrichtung nach Anspruch 4, gekennzeichnet durch eine Einrichtung zum Einstellen eines der beiden sättigungsfähigen Induktoren (L_1 , L_2) für eine Begrenzung des Vorspannstromes im wesentlichen entsprechend der Gleichung
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$$(I_{SCR})_{Vorspann} = \frac{n_{bl}}{n_{pl}} I_b + i_{ml}$$

60 wobei n_{bl} die Anzahl der Windungen seiner Vorspannungswicklung (B), n_{pl} die Anzahl der Windungen seiner Primärwicklung (P), i_{ml} der Magnetisierungsstrom des Induktors und I_b der Vorspannungsstrom ist, und wobei die Sekundärwicklung (S) dieses einen sättigungsfähigen Induktors die Begrenzung des Vorspannstromes unterstützt.

65 6. Einrichtung nach Anspruch 5, gekennzeichnet durch eine Einrichtung zum Einstellen des



anderen der beiden sättigungsfähigen Induktoren (L_1 , L_2) für eine Begrenzung des Abtaststromes in wesentlichen entsprechend der Gleichung

$$(i_{SCR})_{Abtast} = \frac{n_{b2}}{n_{p2}} I_b + i_{m2}$$

wobei n_{b2} die Anzahl der Windungen seiner Vorspannungswicklung (B'), n_{p2} die Anzahl der Windungen seiner Primärwicklung (P'), i_{m2} der Magnetisierungsstrom des Induktors und I_b der Vorspannungsstrom ist, und wobei die Sekundärwicklung (S') dieses anderen sättigungsfähigen Induktors eine Strombegrenzung für einen Schutz des Gleichrichters unterstützt.

7. Einrichtung nach Anspruch 6, dadurch gekennzeichnet, daß eine die Windungen der Vorspannungswicklungen (B , B') der beiden sättigungsfähigen Induktoren umfassende Einrichtung zur Ermöglichung einer unabhängigen Einstellung der Größe der Vorspann- und Abtastströme vorgesehen ist.

8. Einrichtung nach Anspruch 6, dadurch gekennzeichnet, daß die Vorspannungswicklungen (B , B') in Reihe mit einer Resonanz-Ladeinduktivität mit dem Vorspannungsteil der Netzteile verbunden sind.

9. Einrichtung nach Anspruch 3, die einen Anschluß zur Speisung eines regenerativen Verbrauchers aufweist, wobei die an die Netzteile rückübertragene Energie den maximalen Spannungsnennwert des Gleichrichters übersteigen kann, gekennzeichnet durch eine Transformatoreinrichtung ($T1$), über deren Primärwicklung (P) der Anschluß mit dem Verbraucher hergestellt wird und deren Sekundärwicklung (S) mit einer mit den Netzteilen (E_{DC}) verbundenen, entgegengesetzt gepolten Diodeneinrichtung ($CR1$, $CR2$) verbunden ist, um die übersteigende Energie abzuklemmen und eine sichere Betriebsweise des regenerativen Verbrauchers sicherzustellen.

10. Einrichtung nach Anspruch 9, dadurch gekennzeichnet, daß die Netzteile zwei entgegengesetzt gepolte Netzteil (E_{DC}) mit zwei dazwischen geschalteten, in Reihe verbundenen Kondensatoren ($C1$, $C2$) umfassen, daß die Primärwicklung (P) an den Reihenanschluß der Kondensatoren angeschlossen ist und daß die Diodeneinrichtung ($CR1$, $CR2$) parallel zu den Kondensatoren in Reihe geschaltet ist, wobei der Reihenanschluß der Diodeneinrichtung mit der Sekundärwicklung (S) verbunden ist.

11. Siliziumgesteuerter Gleichrichter-Schaltstromkreis, der eine Einrichtung zum Vorspannen und Abtasten nach Anspruch 3 umfaßt, gekennzeichnet durch zwei entgegengesetzt gepolte Netzteile (E_{DC}), die über zwei in Reihe geschaltete Kondensatoren ($C1$, $C2$) für eine Speicherung von Energie in Abhängigkeit von einer Schaltung des Gleichrichters verbunden sind, wobei die gespeicherte Energie den maximalen Spannungsnennwert des Gleichrichters übersteigen kann und zur Übergabe an einen angeschlossenen regenerativen Verbraucher bestimmt ist, und durch eine Einrichtung zum Abklemmen einer solchen übermäßigen Energie zu Ermöglichung einer sicheren Betriebsweise, die eine Transformatoreinrichtung ($T1$) umfaßt, deren Primärwicklung (P) mit dem Reihenanschluß der Kondensatoren und mit dem Verbraucher und deren Sekundärwicklung (S) mit dem Reihenanschluß einer parallel zu den Kondensatoren in Reihe geschalteten Diodeneinrichtung verbunden ist.

Revendications

1. Méthode de réduction des pertes à l'amorçage et lors de la suppression des porteurs dans les circuits de commutation à thyristors associés à des alimentations, dans lesquelles de l'énergie est emmagasinée lors de ladite commutation, l'augmentation du courant des les thyristors lors de ladite commutation est retardée pendant une période prédéterminée d'amorçage des porteurs minoritaires supplémentaires étant ainsi engendrés dans le thyristor, et le courant est limité durant la période d'amorçage, caractérisée par le fait qu'elle consiste en outre à engendrer une tension inverse destinée à effectuer la suppression desdits porteurs minoritaires pendant une période de suppression des porteurs, limiter le courant durant la période de suppression des porteurs et restituer l'énergie résultant de l'amorçage et de la suppression des porteurs pendant chacune des périodes d'amorçage et de suppression des porteurs auxdites alimentations afin de réduire la dissipation thermique de ladite énergie résultante.

2. Méthode selon la revendication 1, caractérisé par le fait que le retard, la génération et la restitution sont accomplis par l'inversion de champs inductifs saturables.

3. Appareil pour l'amorçage et la suppression des porteurs dans des circuits de commutation à thyristors comportant, en combinaison avec des moyens d'alimentation agencés pour emmagasiner de l'énergie lors de la commutation des thyristors, des moyens inductifs saturables intercalés entre les moyens d'alimentation et le thyristor, caractérisé par le fait qu'une partie (B) des moyens inductifs saturables ($L1$; $L2$) est ajustée de façon à provoquer une limitation du courant d'amorçage pendant une période d'amorçage prédéterminée faisant suite à la commutation du thyristor ($SCR1$), et qu'une partie (B') desdits moyens inductifs saturables ($L1$, $L2$) soit ajustée de façon à ce qu'un courant de



suppression des porteurs limité soit engendré, et qu'il comprend des moyens (CR1) connectés auxdits moyens inductifs saturables destinés à restituer auxdits moyens d'alimentation (E_{dc}) l'énergie provenant de la génération desdits courants d'amorçage et de suppression des porteurs, afin de réduire la dissipation thermique de cette énergie dans le circuit.

- 5 4. Appareil selon la revendication 3, caractérisé par le fait que les moyens inductifs saturables comprennent deux inducteurs saturables successifs (L1, L2) chacun comportant un enroulement primaire, un enroulement de polarisation et un enroulement secondaire, les enroulements primaires (P, P') étant connectés en série avec le thyristor (SCR1), les enroulements de polarisation (B, B') étant connectés en série avec une partie de polarisation desdits moyens d'alimentation et les enroulements
10 secondaires (S, S') étant connectés en série avec des diodes à pôles opposés (CR1, CR2).

5. Appareil selon la revendication 4, caractérisé par le fait qu'il comprend des moyens pour ajuster l'un de la paire d'inducteurs saturables (L1, L2) afin de limiter sensiblement ledit courant d'amorçage selon la relation.

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$$(i_{SCR})_{\text{amorçage}} = \frac{n_{b1}}{n_{p1}} i_b + i_{m1}$$

- 20 dans laquelle n_{b1} représente le nombre de spires de son enroulement de polarisation (B) n_{p1} représente le nombre de spires de son enroulement primaire (P), i_{m1} représente le courant de magnétisation de l'induction et i_b représente le courant de polarisation; et que ledit enroulement secondaire (S) d'une des parties d'inducteurs saturables aide à la limitation dudit courant d'amorçage.

6. Appareil selon la revendication 5, caractérisé par le fait qu'il comprend des moyens pour ajuster l'autre de la paire d'inducteurs saturables (L1, L2) afin de limiter sensiblement ledit courant de
25 suppression des porteurs selon la relation.

$$(i_{SCR})_{\text{suppression des porteurs}} = \frac{n_{b2}}{n_{p2}} i_b + i_{m2}$$

30

dans laquelle n_{b2} représente le nombre de spires de son enroulement de polarisation (B'), n_{p2} représente le nombre de spires de son enroulement primaire (P'), i_{m2} représente le courant de magnétisation de l'inducteur et i_b représente le courant de polarisation; et que ledit enroulement secondaire (S') de l'autre paire d'inducteurs saturables aide à la limitation du courant pour protéger le thyristor.

- 35 7. Appareil selon la revendication 6, caractérisé par le fait qu'il comprend des moyens concernant les nombres de spires respectifs de chacun des enroulements (B, B') de la paire d'inducteurs saturables, afin de procurer un réglage indépendant des amplitudes respectives du courant d'amorçage et du courant de suppression des porteurs.

8. Appareil selon la revendication 6, caractérisé par le fait que lesdits enroulements de
40 polarisation (B, B') sont connectés en série par une induction de charge en résonance avec ladite partie de polarisation des moyens d'alimentation.

9. Appareil selon la revendication 3, relié à une charge restitutive d'énergie, qui peut restituer à ladite alimentation une énergie correspondant à une tension dépassant la tension admissible maximale du thyristor, caractérisé par le fait que ledit appareil comporte en outre un transformateur (T1) dont
45 l'enroulement primaire (P) est relié à la charge et dont l'enroulement secondaire (S) est relié à deux diodes à pôles opposés (CR1, CR2) connectées aux moyens d'alimentation (E_{dc}) afin de limiter ladite énergie en excès et d'assurer un fonctionnement sûr avec une charge restitutive d'énergie.

10. Appareil selon la revendication 9, caractérisé par le fait que lesdits moyens d'alimentation comprennent deux alimentations de polarités opposées (E_{dc}) reliées l'une à l'autre par l'intermédiaire de
50 deux condensateurs en série (C1, C2), ledit enroulement primaire (P) est connecté au point de jonction des deux condensateurs en série et des diodes (CR1, CR2), en série, sont reliées aux bornes des condensateurs, le point de jonction des diodes étant connecté audit enroulement secondaire (S).

11. Circuit de commutation à thyristors comprenant un appareil pour l'amorçage et la suppression des porteurs dans les circuits de commutation à thyristors selon la revendication 3, caractérisé par le
55 fait qu'il comprend deux alimentations de polarités opposées (E_{dc}) reliées l'une à l'autre par l'intermédiaire d'une paire de condensateurs en série (C1, C2) destinés à emmagasiner l'énergie lors de la commutation des thyristors, une charge restitutive d'énergie reliée de façon à recevoir l'énergie emmagasinée, et dans laquelle l'énergie supérieure à celle correspondant à la tension maximale admissible des thyristors, et des moyens de limitation de l'énergie en excès destinés à permettre un
60 fonctionnement sûr, comprenant un transformateur (T1) dont l'enroulement primaire (P) est relié au point de jonction des condensateurs en série et à la charge, et dont l'enroulement secondaire (S) est relié au point de jonction des diodes, en série, et connecté aux bornes des condensateurs.