CLAIMS

Claim 1: A resistive random access memory, comprising:

a first electrode;

a dielectric layer formed on the first electrode, wherein the dielectric layer has an opening exposing a portion of the first electrode;

a protection layer disposed on a sidewall of the opening;

at least one switching layer disposed on the exposed portion of the first electrode and exposing a portion of a sidewall of the protection layer; and

at least one conductive layer disposed on the at least one switching layer in the opening, wherein the at least one conductive layer is a second electrode, and

a top surface of the at least one conductive layer is not higher than a top surface of the protection layer.

Claim 2: The resistive random access memory according to claim 1, wherein the at least one switching layer comprises an extension portion extending on the sidewall of the protection layer.

Claim 3: The resistive random access memory according to claim 1, wherein the at least one switching layer is a single-layer structure or a multi-layer structure.

Claim 4: The resistive random access memory according to claim 1, wherein the at least one conductive layer is a single-layer structure or a multi-layer structure.

Claim 5: The resistive random access memory according to claim 1, further comprising a stop layer located on a surface of the dielectric layer.

Claim 6: The resistive random access memory according to claim 1, wherein the at least one conductive layer is in direct contact with the exposed portion of the sidewall of the protection layer.

Claim 7: A method of manufacturing a resistive random access memory, comprising:

forming a first electrode;

forming a dielectric layer on the first electrode;

forming an opening in the dielectric layer to expose a portion of the first electrode;

forming a protection layer on a sidewall of the opening;

forming at least one switching layer on the exposed portion of the first electrode and exposing a portion of a sidewall of the protection layer; and

forming at least one conductive layer on the at least one switching layer in the opening, wherein the at least one conductive layer is a second electrode, and

a top surface of the at least one conductive layer is not higher than a top surface of the protection layer.

Claim 8: The method of manufacturing the resistive random access memory according to claim 7, wherein forming the protection layer comprises:

depositing a protection material on the dielectric layer and the sidewall and a bottom of the opening; and

anisotropically etching the protection material until the first electrode is exposed.

Claim 9: The method of manufacturing the resistive random access memory according to claim 7, wherein forming the at least one switching layer comprises:

conformally depositing at least one switching material on the sidewall of the protection layer and a bottom of the opening; and

removing a portion of the at least one switching material on the sidewall of the protection layer.

Claim 10: The method of manufacturing the resistive random access memory according to claim 7, wherein forming the at least one conductive layer comprises:

depositing at least one conductive material to fill the opening; and

performing a planarization process to remove the at least one conductive material other than the opening.

Claim 11: The method of manufacturing the resistive random access memory according to claim 10, wherein the planarization process is a chemical mechanical polishing (CMP) process.

Claim 12: The method of manufacturing the resistive random access memory according to claim 7, wherein forming the opening in the dielectric layer comprises:

forming a stop layer on a surface of the dielectric layer, wherein the stop layer has a hole exposing a portion of the surface of the dielectric layer; and

etching the dielectric layer using the stop layer as an etching mask.

Claim 13: The method of manufacturing the resistive random access memory according to claim 12, wherein forming the at least one conductive layer comprises:

depositing at least one conductive material to fill the opening; and

using the stop layer as a polishing stop layer and performing a chemical mechanical polishing process to remove the at least one conductive material other than the opening.