C L A I M S

1. A storage device comprising:

a stage on which a semiconductor wafer can be mounted, wherein data is capable of being read from the semiconductor wafer or data is capable of being written to the semiconductor wafer;

a plurality of probe pins for reading or writing data; and

a controller connected the probe pins, and configured to write user data from a host computer to the semiconductor wafer in response to receiving a write request from the host computer and read user data from the semiconductor wafer in response to receiving a read request from the host computer, and,

the semiconductor wafer comprising:

electrodes connectable to the probe pins;

a first memory area that can store user data; and

a second memory area that can store identification information for identification of the semiconductor wafer and a check code for checking integrity of the identification information, and

the controller being capable of reading the identification information and the check code from the second memory area.

2. The storage device according to claim 1, wherein

the controller writes first identification information for identifying the semiconductor wafer and a first check code for checking integrity of the first identification information to the second memory area when a set of identification information and a check code having a

correct correspondence is not stored in the second memory area.

3. The storage device according to claim 1, wherein

the controller acquires a first logical-to-physical address translation table associated with identification information stored in the second memory area from outside or the first memory area when the set of the identification information and the check code having the correct correspondence is stored in the second memory area.

4. The storage device according to any one of claims 1 to 3, wherein

the semiconductor wafer further comprises a plurality of memory dies, and

the electrodes, the first memory area and the second memory area are included in the memory dies.

5. The storage device according to claim 1, further comprising:

a probe card, wherein

the probe pins and the controller are included in the probe card.

6. The storage device according to claim 5, further comprising;

a driver, wherein

the driver moves the probe card or the stage to bring the electrodes of the semiconductor wafer mounted on the stage into contact with the probe pins.

7. The storage device according to claim 1, further comprising:

a stocker capable of storing a plurality of semiconductor wafers.

8. The storage device according to claim 7, further comprising:

a conveyance mechanism which conveys a semiconductor wafer to the stage from the stocker, wherein

the conveyance mechanism can replace the semiconductor wafer mounted on the stage with any one of the plurality of semiconductor wafers in the stocker.

9. The storage device according to claim 7 or 8, wherein

the controller writes identification information different from each other to the plurality of semiconductor wafers, respectively.

10. The storage device according to claim 9, wherein

the controller checks, by the check code, each semiconductor wafer as to whether the identification information written is correct, and writes to or reads from the memory die of the semiconductor wafer only when and the identification information written is correct.

11. The storage device according to claim 1, wherein

the controller is configured to:

when the set of the identification information and the check code having the correct correspondence is stored in the second memory area,

acquire the first logical-to-physical address translation table associated with the identification information from outside or the first memory area;

in response to receiving a write request, write data to a physical storage location in the first memory area, and update the first logical-to-physical address translation table such that a physical address indicating the physical storage location is associated with a logical address designated by the write request; and

in response to receiving the read request, acquire a physical address corresponding to a logical address designated by the read request by referring to the first logical-to-physical address translation table, and read data from the first memory area based on the acquired physical address.

12. The storage device according to claim 1, wherein

when the set of the identification information and the check code having the correct correspondence is stored in the second memory area, the controller is configured to acquire the first logical-to-physical address translation table associated with the identification information of the first semiconductor wafer and first defect information associated with the identification information of the semiconductor wafer from outside or the first memory area, and

the first defect information indicates a defective block included in a plurality of nonvolatile memories in the first semiconductor wafer.

13. The storage device according to claim 1, wherein

the controller is configured to erase both contents of the first memory area and contents of the second memory area when erasing all data in the first semiconductor wafer.

14. A storage system comprising a host computer and a storage device,

the storage device comprising:

a reader & writer in which a probe card can be mounted; and

a stocker capable of storing a plurality of semiconductor wafers,

the reader & writer comprising:

a stage on which one semiconductor wafer of the plurality of semiconductor wafers can be mounted; and

a driver,

the probe card comprising:

a plurality of probe pins; and

a controller connected to the probe pins, and configured to write user data from the host computer to the semiconductor wafer in response to receiving a write request from the host computer and read user data from the semiconductor wafer in response to receiving a read request from the host computer,

each of the plurality of semiconductor wafers comprising:

electrodes connectable to the probe pins;

a first memory area capable of storing user data; and

a second memory area capable of storing identification information for identifying the semiconductor wafer and a check code for checking integrity of the identification information,

the driver moving the probe card or the stage to bring electrodes of a first semiconductor wafer mounted on the stage into contact with the probe pin,

the controller being configured to:

execute write or read of data with respect to the first semiconductor wafer in response to a write request or read request from the host computer;

when a set of identification information and a check code having a correct correspondence is not stored in the second memory area of the first semiconductor wafer, write first identification information for identifying the first semiconductor wafer and a first check code for checking integrity of the first identification information to the second memory area of the first semiconductor wafer based on a request from the host computer; and

when the set of the identification information and the check code having the correct correspondence is stored in the second memory area of the first semiconductor wafer, acquire a first logical-to-physical address translation table associated with the identification information of the first semiconductor wafer from the host computer or the first memory area of the first semiconductor wafer.

15. The storage system according to claim 14, wherein

when the set of the identification information and the check code having the correct correspondence is not stored in the second memory area of the first semiconductor wafer, the controller writes data to the first memory area of the first semiconductor wafer after the controller writes the first identification information and the first check code to the second memory area of the first semiconductor wafer.

16. The storage system according to claim 14, wherein

the controller is configured to:

when the set of the identification information and the check code having the correct correspondence is stored in the second memory area of the first semiconductor wafer,

acquire the first logical-to-physical address translation table from the host computer or the first memory area of the first semiconductor wafer;

in response to receiving a write request from the host computer, write data to a physical storage location in the first memory area of the first semiconductor wafer, and update the first logical-to-physical address translation table such that a physical address indicating the physical storage location is associated with a logical address designated by the write request; and

in response to receiving a read request from the host computer, acquire a physical address corresponding to a logical address designated by the read request by referring to the first logical-to-physical address translation table, and read data from the first memory area of the first semiconductor wafer based on the acquired physical address.

17. The storage system according to claim 14, wherein

the host computer is configured to manage a plurality of logical-to-physical address translation tables and a plurality of pieces of defect information, each of the plurality of logical-to-physical address translation tables and each of the plurality of pieces of defect information corresponding to each of the semiconductor wafers to which identification information and a check code for checking integrity of the identification information are written,

each of the plurality of pieces of defect information indicates a defective block included in a plurality of nonvolatile memories in a corresponding semiconductor wafer,

when the set of the identification information and the check code having the correct correspondence is stored in the second memory area of the first semiconductor wafer, the controller is configured to acquire the first logical-to-physical address translation table associated with the identification information of the first semiconductor wafer and first defect information associated with the identification information of the first semiconductor wafer from the host computer or the first memory area of the first semiconductor wafer, and

the first defect information indicates a defective block included in a plurality of nonvolatile memories in the first semiconductor wafer.

18. The storage system according to claim 14, wherein

the host computer is configured to cause the controller to erase both contents of the first memory area of the first semiconductor wafer and contents of the second memory area of the first semiconductor wafer when erasing all data in the first memory area of the first semiconductor wafer.

19. The storage system according to claim 14, wherein

the host computer is configured to manage a plurality of pieces of identification information corresponding to the plurality of semiconductor wafers to each of which identification information and a check code for checking

integrity of the identification information are written, and

the host computer is allowed to write data to the first memory area of the first semiconductor wafer and read data from the first memory area of the first semiconductor wafer when the set of the identification information and the check code having the correct correspondence is stored in the second memory area of the first semiconductor wafer and the identification information stored in the second memory area matches identification information of a semiconductor wafer to be accessed which is designated by the host computer.

20. The storage system according to claim 14, wherein

the host computer is configured to determine whether the set of the identification information and the check code having the correct correspondence is stored in the second memory area of the first semiconductor wafer by executing verification processing of determining whether correspondence between identification information and a check code which are read from the second memory area of the first semiconductor wafer is correct.

21. The storage system according to claim 14, wherein

the host computer is configured to manage location information indicating physical locations where the plurality of semiconductor wafers exists, and

the physical locations each indicate whether the respective wafer is stocked on the stage, or stored in the stocker, or when stored in the stocker, what location in the stocker, the wafer is stored.