What is claimed is:

1. A semiconductor structure comprising:

a semiconductor substrate including a first active region and a second active region;

a shallow trench isolation region between the first active region and the second active region;

a plurality of gate structures on the first active region;

a first field-effect transistor on the first active region, the first field-effect transistor comprising one of the gate structures on the first active region, a channel region, and a pair of epitaxial source/drain regions on opposite sides of the channel region, each epitaxial source/drain region being located between a pair of the gate structures on the first active region;

a wrap-around metal silicide liner adjoining each epitaxial source/drain region of the first field-effect transistor;

a dielectric layer extending over the semiconductor substrate and the first field-effect transistor;

metal liner portions contiguous, respectively, with each metal silicide liner, each metal liner portion including:

a vertically extending portion located between a pair of the gate structures on the first active region and extending above the source/drain regions; and

a horizontally extending portion below the source/drain regions of the first field-effect transistor and positioned between the shallow trench isolation region and the dielectric layer, the horizontally extending portion of each metal liner portion extending laterally beyond one of the source/drain regions of the first field-effect transistor.

2. The semiconductor structure of claim 1, further including:

a plurality of gate structures on the second active region;

a second field-effect transistor on the second active region, the second field-effect transistor comprising one of the gate structures on the second active region, a channel region, and a pair of epitaxial source/drain regions on opposite sides of the channel region, each epitaxial source/drain region being located between a pair of the gate structures, the dielectric layer extending over the second field-effect transistor;

a wrap-around metal silicide liner adjoining each epitaxial source/drain region of the second field-effect transistor;

metal liner portions contiguous, respectively, with each metal silicide liner of the second field-effect transistor, each metal liner portion including:

a vertically extending portion located between a pair of the gate structures on the second active region and extending above the source/drain regions of the second field-effect transistor, the gate structures on the second active region extending vertically above the vertically extending portion; and

a horizontally extending portion below the source/drain regions of the second field-effect transistor and positioned between the shallow trench isolation region and the dielectric layer, the horizontally extending portion of each metal liner portion extending laterally beyond one of the source/drain regions of the second field-effect transistor.

3. The semiconductor structure of claim 2, further including:

a plurality of vertically extending trenches within the dielectric layer; and

contact metal within the trenches and contacting the metal silicide liners adjoining the epitaxial source/drain regions of the first and second field-effect transistors.

4. The semiconductor structure of claim 3, wherein the first field-effect transistor and the second field-effect transistor are nanosheet transistors and the epitaxial source/drain regions comprise doped, faceted structures.

5. The semiconductor structure of claim 3, wherein the active regions comprise semiconductor fins.

6. The semiconductor structure of claim 5, further including a bottom dielectric isolation layer beneath the first field-effect transistor and the second field-effect transistor, each metal liner portion extending over an edge portion of the bottom dielectric isolation layer.

7. The semiconductor structure of claim 1, further including gate sidewall spacers on sidewalls of the gate structures, the vertically extending portions of the metal liner portions adjoining, respectively, the gate sidewall spacers, the gate structures on the first active region extending vertically above the vertically extending portions of the metal liner portions.

8. The semiconductor structure of claim 7, wherein the metal liner portions comprise titanium and the first field-effect transistor is a nanosheet transistor or a FinFET transistor.

9. A semiconductor structure comprising:

a semiconductor substrate including a first active region and a second active region;

a plurality of parallel gate structures extending across the semiconductor substrate;

a first field-effect transistor on the first active region, the first field-effect transistor comprising one of the gate structures, a channel region, and a first pair of epitaxial source/drain regions on opposite sides of the channel region, each epitaxial source/drain region being located between a first pair of the gate structures;

a second field-effect transistor on the second active region, the second field-effect transistor comprising one of the gate structures, a channel region, and a second pair of epitaxial source/drain regions on opposite sides of the channel region, each epitaxial source/drain region being located between a second pair of the gate structures;

a dielectric layer encasing the first field-effect transistor and the second field-effect transistor;

a metal silicide liner wrapped around each of the source/drain regions;

a conformal metal liner extending from and contiguous with each metal silicide liner, each conformal metal liner including a vertically extending portion confined between one of the first and second pairs of the gate structures and extending vertically above one of the source/drain regions, the first and second pairs of the gate structures extending vertically above the vertically extending portion of each conformal metal liner; and

source/drain contact metal extending vertically through the dielectric layer and contacting the metal silicide liner.

10. The semiconductor structure of claim 9, wherein the channel region of each of the first transistor and the second transistor includes a plurality of vertically stacked channel layers.

11. The semiconductor structure of claim 9, wherein each of the gate structures includes gate sidewall spacers, and further wherein the vertically extending portion of each conformal metal liner includes a pair of vertical segments, each vertical segment adjoining one of the

gate sidewall spacers, the gate sidewall spacers extending vertically above the pairs of vertical segments.

12. A semiconductor structure comprising:

a semiconductor substrate including a first active region and a second active region;

a plurality of parallel gate structures extending across the semiconductor substrate;

a first field-effect transistor on the first active region, the first field-effect transistor comprising one of the gate structures, a channel region, and a first pair of epitaxial source/drain regions on opposite sides of the channel region, each epitaxial source/drain region being located between a first pair of the gate structures;

a second field-effect transistor on the second active region, the second field-effect transistor comprising one of the gate structures, a channel region, and a second pair of epitaxial source/drain regions on opposite sides of the channel region, each epitaxial source/drain region being located between a second pair of the gate structures;

a dielectric layer encasing the first field-effect transistor and the second field-effect transistor;

a metal silicide liner wrapped around each of the source/drain regions;

a conformal metal liner extending from and contiguous with each metal silicide liner, each conformal metal liner including a vertically extending portion confined between one of the first and second pairs of the gate structures and extending vertically above one of the source/drain regions, the first and second pairs of the gate structures extending vertically above the vertically extending portion of each conformal metal liner; and

source/drain contact metal extending vertically through the dielectric layer and contacting the metal silicide liner;

wherein each of the gate structures includes gate sidewall spacers, and further wherein the vertically extending portion of each conformal metal liner includes a pair of vertical segments, each vertical segment adjoining one of the gate sidewall spacers; and

wherein each conformal metal liner includes a horizontal segment extending beneath the dielectric layer and laterally beyond one of the source/drain regions.

13. The semiconductor structure of claim 12, further including a shallow trench isolation region beneath the dielectric layer and laterally between the first active region and the second active region, the horizontal segment of each conformal metal liner extending between the dielectric layer and the shallow trench isolation region.

14. A method of forming a semiconductor structure including wrap-around contacts, comprising:

conformally depositing a metal liner on a monolithic structure, the monolithic structure including:

first and second active regions; and

field-effect transistors on the first and second active regions including gate structures and epitaxial source/drain regions;

forming a metal silicide liner on and wrapping around the epitaxial source/drain regions from the metal liner;

protecting the first and second active regions with a patterned block mask;

selectively removing the metal liner from a region exposed by the patterned block mask between the first and second active regions;

removing the patterned block mask;

forming a protective mask on the monolithic structure such that the epitaxial source/drain regions are entirely beneath the top surface of the protective mask and portions of the metal liner above the first and second active regions are exposed;

selectively removing the exposed portions of the metal liner above the first and second active regions; and

removing the protective mask.

15. The method of claim 14, wherein the forming the protective mask includes:

depositing an organic planarization layer on the monolithic structure; and

etching back the organic planarization layer such that portions of the gate structures extend above the top surface of the protective mask.

16. The method of claim 15, further including:

forming an interlevel dielectric layer over the active regions;

patterning the interlevel dielectric layer, thereby exposing the metal silicide liner on the epitaxial source/drain regions;

forming metal contacts within the interlevel dielectric layer and directly contacting the metal silicide liner on the epitaxial source/drain regions.

17. The method of claim 16, wherein the monolithic structure further includes gate caps and gate sidewall spacers adjoining the gate structures, further wherein selectively removing the exposed portions of the metal liner above the first and second active regions includes removing the metal liner from the gate caps and top portions of the gate sidewall spacers.

18. The method of claim 17, wherein the monolithic structure includes a shallow trench isolation region between the first and second active regions, further wherein selectively removing the metal liner from a region between the first and second active regions includes removing the metal liner from a top surface of the shallow trench isolation region.

19. The method of claim 18, wherein the monolithic structure further includes a contact etch stop liner extending over the first and second active regions and the shallow trench isolation region, further including:

removing the contact etch stop liner and replacing the contact etch stop liner with the metal liner.

20. The method of claim 18, wherein the field-effect transistors include nanosheet transistors or FinFET transistors.

21. The method of claim 14, wherein the field-effect transistors include nanosheet transistors or FinFET transistors and the epitaxial source/drain regions comprise doped, faceted semiconductor regions, further wherein conformally depositing the metal liner causes the metal liner to wrap around the doped, faceted semiconductor regions.

22. The method of claim 21, wherein the patterned block mask completely covers and extends laterally beyond the epitaxial source/drain regions.

23. The method of claim 22, wherein:

the monolithic structure further includes gate caps and gate sidewall spacers adjoining the gate structures;

forming the protective mask includes depositing an organic planarization layer on the monolithic structure and etching back the organic planarization layer, thereby exposing the gate caps and top portions of the gate sidewall spacers; and

selectively removing the exposed portions of the metal liner above the first and second active regions includes removing the metal liner from the gate caps and the top portions of the gate sidewall spacers.

24. A method of forming a semiconductor structure including wrap-around contacts, comprising:

obtaining a monolithic structure including:

first and second active regions;

field-effect transistors on the first and second active regions including gate structures, gate caps above the gate structures, gate sidewall spacers on sidewalls of the gate structures, and epitaxial source/drain regions between pairs of gate structures; and

a contiguous liner including first liner portions on and wrapping around the epitaxial source/drain regions and a metal liner extending between the first and second active regions and over the gate caps and gate sidewall spacers;

protecting the first and second active regions with a patterned block mask;

selectively removing the metal liner from a region exposed by the patterned block mask between the first and second active regions;

removing the patterned block mask;

forming a protective mask on the monolithic structure such that the gate caps and top portions of the gate sidewall spacers extend above a top surface of the protective mask and the epitaxial source/drain regions are beneath the top surface of the protective mask;

selectively removing the metal liner from the top portions of the gate sidewall spacers and the gate caps; and

removing the protective mask.

25. The method of claim 24, wherein the field-effect transistors comprise nanosheet transistors or FinFET transistors, further including:

forming metal silicide liners from the first liner portions;

forming an interlevel dielectric layer over the first and second active regions;

patterning the interlevel dielectric layer, thereby exposing the metal silicide liners on the epitaxial source/drain regions; and

forming metal contacts within the interlevel dielectric layer and directly contacting the metal silicide liners on the epitaxial source/drain regions.