

A SEMICONDUCTOR DEVICE HAVING A PRESSURE SENSOR
AND A METHOD OF MANUFACTURING SUCH A DEVICE

The present invention relates to a semiconductor device having a pressure sensor, and to a method of manufacturing such a device.

It can be expected that a semiconductor pressure
5 sensor will have the advantages of a small size, a low-cost
and a high performance, when compared to other known
pressure sensors such as a Bourdon tube or a mechanical
pressure sensor employing a bellows. One example of
a semiconductor pressure sensor is a silicon diaphragm
10 type pressure sensor.

As shown in Figure 1 of the accompanying drawings,
a silicon diaphragm type pressure sensor is formed by a
single crystal Si substrate (silicon chip) 1 having a
relatively thin or membrane portion 3 which is sufficiently
15 thin to be deformed sensitively by differences in pressure
between the spaces over and under this membrane portion 3. A
depressed portion 2 is provided in a part of the rear
surface of the single crystal Si substrate 1, and four
diffused resistors 4 are formed as piezoresistive elements
20 in the front surface of the membrane portion 3. The
diffused resistors are connected together to form a
bridge network, and the electrical resistances of the
resistors change when the membrane portion 3 is deformed
by mechanical motion or stress. Thus, the semiconductor
25 pressure sensor detects pressure electrically.

Such a silicon diaphragm type pressure sensor can

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be manufactured by the following steps. First of all, boron (B) is diffused into parts of one surface (hereinafter referred to as the front surface) of a single crystal Si substrate 1 having a thickness of approximately 5 280 μm , thereby to form the diffused resistors 4. The other surface (hereinafter referred to as the rear surface) of the Si substrate 1 is ground to a mirror-like finish. Thereafter, as shown in Figure 2, the rear surface of the single crystal Si substrate 1 is subjected to 10 anisotropic etching with an alkali etchant such as potassium hydroxide (KOH), whereby a depressed portion 2 is formed and a membrane portion 3, which is desirably approximately 25 μm in thickness, is left in the substrate 1.

15 The following problems, however, have been recognized by the inventors of the present invention.

When the depressed portion 2 is etched:

(i) it is difficult to form the membrane portion 3 uniformly and accurately to a thickness of approximately 20 25 μm , and

(ii) as shown in Figure 2 of the accompanying drawings the etched Si surface, which corresponds to the membrane portion 3, is not flat due to such drawbacks as foreign matter, contamination, and crystal defects 25 in the substrate 1. The etched surface has corrugations 5 which may have an unevenness of approximately $\pm 5 \mu\text{m}$. The corrugations 5 are likely to cause strain during deformation due to pressure variations, and it has thus been difficult to manufacture pressure sensors of high

sensitivity, with good reproducibility.

A method of forming the membrane portion 3 to an accurate thickness is apparently disclosed in U.S. Patent Specification No. 3,893,228. According to that specification, the thickness of the membrane portion is controlled by utilizing a p^+ -type epitaxial layer as an etching stopper. Other prior art literature, however, does not disclose the flattening of the membrane portion at all or does not contain any statement suggestive of ways of achieving such flattening. It is believed that the method of forming a semiconductor pressure sensor taught in US 3,893,228 will have problems in satisfactorily flattening the membrane portion for the reason stated below.

As is well known, where a semiconductor layer has been formed on a semiconductor substrate by epitaxial growth, it has a uniform impurity concentration in the thickness direction thereof. In the case of the technique disclosed in US 3,893,228, therefore, there will be an abrupt change between the impurity concentration of the substrate and that of the epitaxial semiconductor layer. As shown in Figure 3a of the accompanying drawings, when the rear surface of the substrate 1 has been etched causing an uneven surface (indicated by a dotted line) until the epitaxial semiconductor layer EP is reached, parts of the substrate 1 are left as protuberances 5 on the epitaxial layer EP. In order to remove the protuberances 5 completely, the substrate 1 must be exposed to an etchant for a predetermined time. During this time

the epitaxial semiconductor layer EP is also etched, though at a rate lower than the etching rate of the protuberances 5. After the protuberances 5 have been completely removed, the epitaxial semiconductor layer EP is found to have a ruggedness as shown in Figure 3b of the accompanying drawings. It is difficult to remove the ruggedness completely, because the epitaxial semiconductor layer EP has a uniform impurity concentration as stated before.

The present invention seeks to overcome or at least ameliorate the problem of non-uniformity of the membrane portion. It does this by providing in a first aspect of the invention, a semiconductor device having a pressure sensor comprising a semiconductor body having a membrane portion therein, wherein a plurality of semiconductor resistor layers connected together in a bridge network are provided in a first surface of the membrane portion, and a heavily doped semiconductor layer is provided in a second surface of the membrane portion opposite to the first surface, the heavily doped semiconductor layer having a concentration gradient in a direction substantially perpendicular to the second surface such that the impurity concentration increases in a direction away from the second surface.

The use of a heavily doped layer with such an impurity gradient means that when the etchant (e.g. an alkali etchant) reaches the heavily doped layer, the impurity gradient of the heavily doped layer causes

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preferential etching of raised parts of the surface being etched, thereby smoothing out unevenness in the etched surface and permitting a membrane portion of uniform thickness to be achieved.

5 Preferably the surface in which the resistor layers are formed, and the surface which is etched are each parallel to the (100) crystal plane. The resistor layers are desirably formed in the direction of the $\langle 110 \rangle$ axis and are connected together to form a bridge network. Deform-
10 ation of the membrane portion due to pressure difference across it causes changes in resistance of the resistor layers hence enabling the pressure to be sensed.

 The semiconductor body (including the substrate) may be an n-type silicon single crystal, and each resistor
15 layer is a p-type diffused layer. The heavily doped layer may be an n-type diffused layer.

 A semiconductor active element (e.g. a part of an integrated circuit) may be formed in the semiconductor substrate adjacent the pressure sensor. It has been found
20 that such an active element can co-exist with the pressure sensor, although it is preferable to isolate the active element from the sensor by forming isolation layers between the two.

 According to a second aspect of the invention there
25 is provided a method of manufacturing a semiconductor device having a pressure sensor, the method comprising forming in a semiconductor body a heavily doped buried

layer; forming semiconductor resistor layers in a first surface of the semiconductor body; and etching the semiconductor body from the opposite side to that in which the resistor layers are formed, to a depth extending
5 partially into the buried layer, so as to form a membrane layer containing the resistor layers and a part of the heavily doped layer, to expose the buried layer at a second surface, wherein the buried layer has a concentration gradient in a direction substantially perpendicular to the
10 second surface such that the impurity concentration increases in a direction away from the second surface.

Embodiments of the present invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

15 Figure 1 is a sectional view through an example of a prior art silicon diaphragm type pressure sensor, and has already been discussed;

Figure 2 is a sectional view showing a problem

associated with the pressure sensor shown in Figure 1, and has already been discussed;

Figures 3a and 3b are sectional views showing a problem associated with a silicon pressure sensor 5 which is disclosed in the U.S. Patent Specification No. 3,893,228, and has already been discussed;

Figures 4 to 8 are sectional diagrams showing the stages of a process for manufacturing one embodiment of a pressure sensor according to the present invention;

10 Figure 9a is a graph showing the relationship between the impurity concentration in a semiconductor and the rate of etching by an alkali etchant;

Figure 9b is a diagram showing the impurity profile of the part of a semiconductor device taken 15 along line X - X' in Figure 7;

Figure 9c is a partly enlarged sectional view of the semiconductor device shown in Figure 7;

Figure 10 is a plan view showing another embodiment of a pressure sensor according to the present 20 invention;

Figure 11 is a sectional view taken along line A - A' in Figure 10;

Figure 12 is a sectional view showing another embodiment of a pressure sensor according to the present 25 invention;

Figures 13 to 19 are sectional views showing the stages in a process for manufacturing an IC which includes a pressure sensor being another embodiment of the present invention;



Figure 20 is a plan view showing parts of an IC which includes a pressure sensor being another embodiment of the present invention; and.

Figure 21 is a sectional view taken along line 5 B - B' in Figure 20.

Embodiment 1

Figures 4 to 8 illustrate a process for manufacturing

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a silicon diaphragm type pressure sensor to which the present invention is applied.

(1) As shown in Figure 4, a lightly-doped p-type single crystal Si substrate (wafer) 6 having thickness of approximately 400 μm is prepared. The one (front) surface of this Si substrate is formed with an oxide film (SiO_2 film) 7 having thickness of 8000 $\text{\AA}$ - 9000 $\text{\AA}$. This oxide film 7 is produced by the thermal oxidation of the Si substrate 6, for example, by heating the substrate at 1100°C in wet O_2 for 110 minutes. Next, an important step for attaining a precise thickness for the membrane portion (or the relatively thin portion) of the pressure sensor is performed. In order to form a heavily-doped semiconductor region serving as an etching stopper, as illustrated in Figure 4, an n-type impurity such as Sb (antimony) is introduced into the front surface of the substrate by predeposition or ion implantation by employing the oxide film (SiO_2 film) 7 as a mask for introducing the impurity. More specifically, first, the oxide film 7 is selectively etched by the well-known photoetching process in order to expose the selected area of the substrate surface into which the n-type impurity is to be introduced. Subsequently, using the remaining oxide film 7 as the mask, the n-type impurity is introduced into the exposed

front surface of the substrate. The layer of the introduced n-type impurity is as shallow as $0.1\ \mu\text{m} - 0.2\ \mu\text{m}$. Regarding the introduction of the n-type impurity, in a case where the introducing method is the predeposition, Sb_2O_3 can be deposited on the front surfaces of Si wafers in such a way that a solid impurity source such as of the Sb_2O_3 is placed in a quartz diffusion tube together with the Si wafers, that Ar gas and O_2 gas are used as carrier gases, and that a furnace in which the tube is inserted is held at a temperature of 900°C . On the other hand, in case of the ion implantation, when ions are introduced at a high density by at once, unfavorably the substrate surface suffers ion damage. Therefore, ion implanting operations each of which is set at the implantation energy level of $75\ \text{keV} - 125\ \text{keV}$ and the dosage of $1 \times 10^{14}\ \text{atoms}/\text{cm}^2$ are repeated several times.

(2) The oxide film 7 is removed using fluoric acid as an etchant. As shown in Figure 5, a lightly-doped n-type Si layer 8 having $25 - 30\ \mu\text{m}$ thickness is formed on the front surface of the substrate 6 by epitaxial growth. This epitaxial growth is carried out by the thermodecomposition of silane (SiH_4), and a preferable temperature at that time is approximately 1100°C . During the epitaxial growth, the predeposited or

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ion-implanted Sb is diffused into the substrate 6 and the Si layer 8 by drive-in diffusion, to form a heavily-doped n-type buried layer 9 (thickness: 2 μm) which has an impurity concentration gradient (peak value: about 10^{19} atoms/cm²).

An insulator film 7a is formed on the surface of the Si layer 8. The formation of the insulator film 7a can be achieved by a method similar to the method of forming the oxide film 7. That is, the Si substrate 6 formed with the Si layer 8 is heated at 1100°C in wet O₂ for 110 minutes, whereby the surface of the Si layer 8 is oxidized to be formed with the oxide film (SiO₂ film) 7a. Subsequently, in order to form four semiconductor resistor regions, i.e., four piezoresistive elements, in the selected areas of that part of the Si layer 8 which overlies the n-type buried layer 9, the oxide film 7a is selectively removed by the well-known photoetching process so as to expose the part of the n-type Si layer 8. A p-type impurity, for example, B (boron) is introduced into the exposed surface of the Si layer 8 by predeposition or ion implantation. The p-type impurity introduced in the Si layer 8 is subjected to drive-in diffusion, thereby to form p-type diffused resistor regions 10 which are 2 - 3 μm thick and which have the sheet resistance of 100 ohm per square. In

case of the predeposition, a solid impurity source such as of B_2O_3 is placed in a quartz diffusion tube together with Si wafers, and the B_2O_3 is deposited on the surfaces of the Si wafers at the temperature of about $900^{\circ}C$ while the interior of the silica tube is held in a reduced pressure condition. On the other hand, in case of the ion implantation, boron ions are implanted into Si wafers. At this time, the implantation energy level is 75 keV, and the dosage is 1×10^{13} atoms/cm².

In the case of the predeposition method, after performing the drive-in diffusion, boron glass deposited on the surfaces of the diffused resistor regions 10 and the surface of the oxide film 7a is removed. Thereafter, the exposed surfaces of the diffused resistor regions 10 are oxidized, whereby thin oxide films (SiO_2 films having a thickness of approximately 500 Å) 7b are formed on the diffused resistor regions 10.

In the case of the ion implantation method, preferably oxide films 7b (thickness: 100 Å) are formed before the execution of the ion implantation in order to prevent the ion damage of the surface of the Si layer 8, whereupon the boron ions are introduced into the Si layer 8 through the oxide films 7b.

(3) As shown in Figure 6, in order to lead out

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electrodes from the diffused resistor regions 10, the SiO_2 films 7b are selectively etched to form contact holes CH. Thereafter, Al (aluminum) layer (1 - 1.75 μm thickness) are formed on the surfaces of the SiO_2 films 7a and 7b by evaporation. Further, terminal portions 11, and the electrodes 12 ohmically connected to the respective diffused resistor regions 10 are formed by the photoetching process. Subsequently, a final passivation film 13 (thickness: 1.2 μm) made of plasma nitride or PSG (phosphosilicate glass) is formed. This final passivation film 13 serves to protect the SiO_2 films 7a, 7b and the electrode 12. In particular, since the plasma nitride has a stable film property, the use thereof is desirable. A stacked film in which a PSG film (thickness: 0.2 μm) and a plasma nitride film (thickness: 1.1 μm) are successively formed on the SiO_2 films 7a, 7b may well be employed as the final passivation film. For some purposes or in some applications, the passivation film 13 on the diffused resistors 10 of the pressure sensor portion is especially removed to leave only the thin oxide films (SiO_2 films) 7b thereon, whereby nonuniformity in the strains of the resistors attributed to dispersions in the quality and thickness of the passivation film is prevented.

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(4) As shown in Figure 7, a photoresist mask 14 is provided on the rear surface ((100) crystallographic plane) of the p-type substrate 6, and anisotropic etching is performed with an alkali etchant such as KOH, whereby a deep depressed portion 15 is formed. The depressed portion is etched so as to reach the n^+ -type buried layer 9. During the etching, the etched surface of the substrate does not become flat but becomes rugged as shown in Figure 7.

In case of alkali-etching a silicon crystal substrate doped with an impurity, the relationship between the impurity concentration and the etching rate is as shown in Figure 9a. While the impurity concentration is low, the etching rate does not change, whereas when the former reaches the concentration of 10^{19} atoms/cm³, the etching rate is decreasing rapidly.

On the other hand, the impurity profile taken along line X - X' of the semiconductor shown in Figure 7 is depicted in Figure 9b. As apparent from this figure, the n^+ -type buried layer 9 has the gradient of the impurity concentration because it has been formed by the drive-in diffusion. For this reason, when the etching has reached the heavily-doped buried layer, the etching rate is decelerated, so that a flat etched surface is gradually formed as shown in Figure 9c. More specifically,

referring to Figure 9c, when the n^+ -type buried layer 9 has been reached the step or ruggedness of the etched surface is somewhat great as indicated by a dotted line A. However, as the etching proceeds in the direction of an arrow, the impurity concentration of the n^+ -type buried layer 9 becomes high, so that a recess A_1 is etched at a low rate, while a protuberance A_2 is efficiently etched owing to an etching rate somewhat higher than that of the recess A_1 . Therefore, the step of the etched surface decreases as indicated by a dotted line B. In this way, the etching rate is controlled of itself, and a flat etched surface is achieved as shown in Figure 8.

Figure 10 shows the layout of the four diffused resistors 10 and the configuration of the bridge-connected electrodes 12 in the silicon diaphragm type sensor. These electrodes 12 are to be connected to a detector circuit (not shown) through the terminals (bonding pads) 11. Figure 11 is a sectional view of the sensor taken along line A - A' in Figure 10.

In the foregoing embodiment, the n^+ -type buried layer has been utilized for the flattening etching. However, a p^+ -type buried layer may well be utilized instead of the n^+ -type buried layer. Figure 12 shows a case where, in the step (2) described before, a

p^+ -type buried layer 16 is formed in place of the n^+ -type buried layer 9, whereupon the depressed portion 15 is formed so as to reach this layer 16. In order to form the p^+ -type buried layer 16, a p-type impurity such as boron is used, and it is introduced into the Si substrate 6 by predeposition or ion implantation as in the case of forming the n^+ -type buried layer 9. After the impurity introduction for forming the p^+ -type buried layer 16 has been completed, the steps (3) and (4) are carried out. The p^+ -type buried layer 16 has the gradient of the impurity concentration.

Embodiment 2:

Figures 13 to 19 show a process for manufacturing an embodiment in which a pressure sensor and other active elements coexist in a single semiconductor body.

(1) A lightly-doped p-type single crystal Si substrate 6 having a thickness of approximately 400 μm is prepared. As illustrated in Figure 13, using as a mask an oxide film (SiO_2 film having a thickness of 8000 $\text{\AA}$ - 9000 $\text{\AA}$) 17, boron ions (B^+) are implanted into the part of the front surface of the substrate to form the pressure sensor and the part thereof to form an isolation region. The implantation energy of the boron ions is preferably 75 keV - 125 keV, and

the implantation dosage is 10^{14} atoms/cm² - 10^{16} atoms/cm².

The implanted boron ions are subjected to drive-in diffusion by a heat treatment, whereby p⁺-type layers 18a and 18b are simultaneously formed, respectively, as shown in Figure 14. The p⁺-type buried layer 18a is used as an etching stopper in forming the depressed portion of the pressure sensor, and the p⁺-type buried layer 18b as a part of the isolation region.

(2) After removing the oxide film 17, a new oxide film (SiO₂ film having a thickness of 8000 Å - 9000 Å) 19 is formed by thermal oxidation. The p-type impurity (boron) is subjected to the drive-in diffusion during the formation of the oxide film 19, whereby the p⁺-type buried layers 18a and 18b shown in Figure 14 are formed as stated above.

Subsequently, the step for forming n⁺-type buried layer is carried out in order to prevent the occurrence of a substrate parasitic transistor operation in the pressure sensor portion and to reduce a collector resistance in the active element portion such as a vertical transistor or to prevent the occurrence of a substrate parasitic transistor operation in the active element portion such as a lateral transistor. Namely, first of all, the oxide film 19 is selectively

etched thereby to form a mask for introducing an impurity into selected areas. Using this mask, the n-type impurity such as antimony is introduced into the exposed surface areas of the Si substrate 6 by predeposition or ion implantation.

Figure 14 shows the case of the ion implantation. In this case, the antimony ions (Sb^+) are implanted into the front surface of the Si substrate 6 at an implantation energy level of 75 keV - 125 keV. The dosage of the implantation is 10^{14} atoms/cm² - 10^{16} atoms/cm².

On the other hand, in case of the predeposition, as in the foregoing embodiment 1, a solid impurity source such as Sb_2O_3 is placed in a quartz diffusion tube together with Si wafers, Ar gas and O_2 gas are used as carrier gases, and a furnace in which the tube is inserted is held at a temperature of 900°C, whereby the Sb_2O_3 is deposited on the front surfaces of the Si wafers.

In order to prevent of the occurrence of a parasitic p-n-p transistor, the antimony is introduced into the pressure sensor forming portion so as to overlie the p⁺-type buried layer 18a and to be broader than it, as shown in Figure 14.

(3) After removing the oxide film (SiO_2 film) 19,

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a lightly-doped n-type epitaxial Si layer (impurity concentration: 10^{15} atoms/cm³, thickness: 30 μ m) 21 is formed on the entire surface as shown in Figure 15. At this time, the p⁺-type buried layers 18a, 18b and n⁺-type buried layers 20a, 20b are respectively formed by the boron ions (B⁺) and antimony ions (Sb⁺) introduced by the preceding steps. The impurity concentrations of the p⁺-type buried layers 18a, 18b and the n⁺-type buried layers 20a, 20b exhibit peak values of about 10^{19} atoms/cm³. The formation of the epitaxial Si layer 21 is achieved by the thermodecomposition of silane, and a preferable temperature at that time is about 1100°C. Next, an oxide film (SiO₂ film having a thickness of 8000 Å - 9000 Å) 22 is formed on the surface of the epitaxial Si layer 21. The oxide film 22 is formed by thermally oxidizing the surface of the Si layer 21. Also, the oxide film 22 may be formed by the well-known CVD (chemical vapor deposition) process. Further, an insulator film such as of Si₃N₄ (silicon nitride) may be deposited on the surface of the Si layer 21 instead of the oxide film.

(4) Subsequently, an isolation layer is formed as shown in Figure 16. First of all, the oxide film 22 is selectively removed by photoresist processing. Using the resultant oxide film (SiO₂ film) 22 as a

mask for selectively introducing an impurity, the p-type impurity such as boron is introduced into the exposed surface part of the n-type epitaxial Si layer 21, thereby to form the p-type diffused layer (isolation layer) 23 for isolating the elements. Since, at this time, the p-type impurity is diffused into the epitaxial Si layer 21 by drive-in diffusion also from the p⁺-type buried layer 18b, the isolation can be achieved in a short diffusion time owing to the diffusions in both the directions. Accordingly, lateral diffusion is reduced. Therefore, the occupying area of the isolation layer 23 becomes small, and a higher density of integration can be accomplished.

(5) In order to form diffused resistors to constitute the pressure sensor, the SiO₂ film 22 is selectively removed with the well-known photoresist processing as shown in Figure 17. A p-type impurity, e.g., boron is ion-implanted into the exposed surface areas of the Si layer 21, and is thereafter subjected to drive-in diffusion, whereby the p-type diffused resistors 24 are formed. The p-type diffused resistors 24 have the sheet resistance of 100 ohm per square, and are approximately 2 - 3 μm deep.

(6) After forming the diffused resistors 24, a p⁺-type emitter region 28a and a p⁺-type collector region

28b which constitute a lateral transistor are formed in an island region 21a as shown in Figure 18, by selective diffusion utilizing the oxide film 22 as a mask. The island region 21a acts as the base region of this transistor. Subsequently, the base region 29 of a vertical transistor is formed in an island region 21b by selective diffusion, and an emitter region 30e is formed in the base region 29. The lateral transistor and the vertical transistor are used for the temperature compensation circuit of the pressure sensor. Next, the SiO_2 film 22 is selectively etched to form contact holes in predetermined positions. Thereafter, an Al (aluminum) layer which is $1\text{ }\mu\text{m} - 1.75\text{ }\mu\text{m}$ thick is formed on the surface of the SiO_2 film by evaporation. This Al layer is selectively removed by photoetching so as to form electrodes (conductive layer) 25 which are connected to the respectively element regions. Next, a final passivation film (thickness: $1.3\text{ }\mu\text{m}$) 26 made of plasma nitride or PSG (phosphosilicate glass) is formed. This final passivation film 26 serves to prevent the SiO_2 film 22 from coming into touch with the open air to get stained. In particular, since the plasma nitride has a stable film property, the use thereof is desirable. A stacked film in which a PSG film (thickness: $0.2\text{ }\mu\text{m}$) and a plasma nitride film (thickness:



1.1 μm) are successively formed on the SiO_2 22 may well be employed as the final passivation film.

As in the foregoing embodiment 1, the passivation film may be removed to leave only the thin oxide film on the pressure sensor portion, whereby nonuniformity in the strain of the resistors attributed to dispersions in the quality and thickness of the passivation film is decreased.

The rear surface of the p-type substrate 6 is anisotropically etched by the alkali etchant such as KOH, to form a depressed portion 27 as shown in Figure 19. For the same reason as explained in Embodiment 1, the etching for forming the depressed portion has its etching rate controlled after the p^+ -type buried layer has been reached. Therefore, a flat etched surface is achieved as the surface of the membrane portion 18a.

Figures 20 and 21 are a plan view and a sectional view, respectively, concretely showing the embodiment of the semiconductor device which is provided by the aforementioned process and in which the other active elements are formed around the pressure sensor.

Figure 20 principally shows the diffused layers, which are indicated by solid lines. The sectional view of Figure 21 is taken along line B - B' in Figure 20.

Referring to Figure 20, the depressed portion 27

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or diaphragm is formed on the rear side of substantially the central part of a Si semiconductor body (Si epitaxial layer 21, Si substrate 6) having the (100) crystallographic plane. The p^+ -type isolation layer 23 for isolating the pressure sensor portion from the other elements (active elements) is formed so as to surround the diaphragm. The sides of the diaphragm (27) surrounded with the isolation layer 23 are respectively formed with the resistors (diffused resistors) for use as the pressure sensor. As can be seen from Figure 20, these resistors have the same structure and are connected by the wiring layers 25 as the bridge network. The structure of the resistor will be explained as follows.

Each of resistors ($R_1 - R_4$) is composed of p-type diffused resistor layers 24 (sheet resistance: 100 ohm per square) which are formed in the direction of the $\langle 110 \rangle$ axis; p^+ -type diffused layers for contacts, 28a (sheet resistance: 30 ohm per square) which are formed in the direction of the $\langle 100 \rangle$ axis, inclining by 45 degrees to the $\langle 110 \rangle$ axis; and a p^+ -type diffused layer 28b (sheet resistance: 30 ohm per square) which connects the p-type diffused resistor layers 24 extending in parallel with each other. The p-type diffused resistor layer 24 extending in the direction of the

$\langle 110 \rangle$ axis (or an axis equivalent thereto) is sensitivity in the piezo-resistive effect, so a resistance changes sensitively to the strain of the diaphragm. This is especially remarkable in the case of the resistor layer which has the p-conductivity type. On the other hand, the p^+ -type diffused layer 28a is in the direction of a low piezo-resistive effect (the direction of the $\langle 100 \rangle$ axis or an axis equivalent thereto) and is heavily doped, so that the change of its resistance relative to the strain of the diaphragm is small and negligible. Further, the p^+ -type diffused layer 28b is heavily doped and is formed so as to form a square, so that the influence thereof on the strain of the diaphragm is negligible. The p^+ -type diffused layers 28a and 28b are formed simultaneously with the emitter and collector regions 28 of the P-N-P transistor (indicated as PNP TRS in Figure 20). In order to prevent the leakage current between the resistors within the diaphragm, an n^+ -type diffused layer 30' is formed so as to surround the p-type diffused resistor layers 24 and the p^+ -type diffused layers 28a, 28b. This n^+ -type diffused layer 30' is formed simultaneously with the emitter region 30a and collector contact region 30b of the N-P-N transistor (indicated as NPN TRS in Figure 20) and the base contact region 30c of the

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P-N-P transistor by the use of an n-type impurity such as arsenic (As) or phosphorus (P). The P-N-P transistor and N-P-N transistor which are sited around the diaphragm constitute a temperature compensation circuit, an amplifier circuit. In addition, external lead-out terminals (bonding pads) 35 are sited on the peripheral edges of the semiconductor body. As can be seen from Figure 21, the bottom of the diaphragm 27 is formed with the heavily-doped p^+ -type buried layer 18a which has the gradient of the impurity concentration and which serves as the etching stopper. The p^+ -type buried layer 18a is overlaid with the n^+ -type buried layer 20a, which prevents the operation of a parasitic p-n-p transistor (p-type diffused resistor layer 24 - n^- -type epitaxial Si layer 21a - p^+ -type buried layer 18a). That is, the carriers are recombined by the heavily-doped n^+ -type buried layer 20a, thereby to prevent the transportation of the carriers from the p-type diffused resistor layer 24 to the p^+ -type buried layer 18a.

According to the constructions described above in conjunction with the embodiments, the objects of the invention may be accomplished and many other effects may be brought forth as follows.

- (1) A buried layer which is heavily doped and which



has the gradient of the impurity concentration is formed in a pressure sensor region (at the etched side of a diaphragm), whereby a flat surface is obtained at the etched side of a membrane portion when a depressed portion is etched.

(2) A heavily-doped p^+ -type layer is disposed under an n^+ -type buried layer, whereby the exposure of the p-n junction between the n^+ -type buried layer and the p^- -type substrate can be avoided after the formation of the depressed portion, and protectiveness is enhanced. In addition, the operation of a parasitic transistor can be prevented.

(3) A p^+ -type buried layer formed around the sensor portion can finish up an isolation region of small width when coupled with a p^+ -type diffused layer which extends from the front surface of an epitaxial n-type Si layer. Therefore, the occupying area of the isolation region can be reduced, and a semiconductor device having a high density of integration can be produced.

(4) n^+ -type buried layers can be utilized as parts of active elements (the collector of the N-P-N transistor, the base of the lateral P-N-P transistor) in peripheral portions.

(5) A Si membrane portion can be sufficiently thickened by rendering the epitaxial n-type Si layer

thick, whereby even a sensor applicable to a high pressure (100 Torr or above) can be manufactured at high precision.

(6) An IC in which active elements of high withstand voltage and a pressure sensor applicable to a high pressure are integrally combined can be realized by the use of a thick n-type Si layer.

(7) In case of using an n^+ -type buried layer as an etching stopper as in Embodiment 1, no parasitic transistor is formed directly below p-type diffused resistor layers.

(8) In case of Embodiment 2, before the step of anisotropic etching, active element portions and a pressure sensor portion can be formed by the standard process of a bipolar IC, and no increase in processing steps is involved. More specifically, the p^+ -type buried layer 18a as the etching stopper can be formed simultaneously with the p^+ -type buried layer 18b which forms the part of the isolation region. In addition, the n^+ -type buried layer 20a for preventing the parasitic transistor can be formed simultaneously with the n^+ -type buried layers 20b of the active element portions.

**CLAIMS:**

1. A semiconductor device having a pressure sensor comprising a semiconductor body having a membrane portion therein, wherein a plurality of semiconductor resistor
5 layers connected together in a bridge network are provided in a first surface of the membrane portion, and a heavily doped semiconductor layer is provided in a second surface of the membrane portion opposite to the first surface, the heavily doped semiconductor layer having a concentration
10 gradient in a direction substantially perpendicular to the second surface such that the impurity concentration increases in a direction away from the second surface.
2. A device according to claim 1, wherein the semiconductor body includes the (100) plane, and the resistor
15 layers are formed in the direction of the $\langle 110 \rangle$ axis or an axis equivalent thereto.
3. A device according to claim 1 or claim 2, having an active element in a part of the semiconductor body adjacent the membrane portion.
- 20 4. A device according to any one of the preceding claims, wherein the heavily doped layer is of n^+ type, p^+ type or p^+-n^+ type.
5. A device according to any one of the preceding claims, wherein the semiconductor body comprises a semi-
25 conductor substrate having an opening therein at the membrane portion, and a further semiconductor layer on the substrate and extending across that opening.



6. A device according to claim 5, wherein the substrate and the further semiconductor layer are of opposite conductivity types.
7. A device according to claim 5 or claim 6, wherein the
5 heavily doped semiconductor layer is of the same conductivity type as the further semiconductor layer.
8. A device according to claim 5 or claim 6, wherein the heavily doped semiconductor layer is of opposite conductivity type to the further semiconductor layer.
- 10 9. A device according to any one of claims 5 to 8, wherein the heavily doped layer is a first heavily doped layer, and there is a second heavily doped layer of opposite conductivity type to the first heavily doped layer between the first heavily doped layer and the further semiconductor layer.
15
10. A device according to any one of claims 5 to 9, wherein the second heavily doped layer is of n-type.
11. A device according to any one of the preceding claims, having semiconductor isolation regions of the same
20 conductivity type as the heavily doped layer surrounding the resistor layers, each isolation region having a first part extending from a surface of the body which (in the continuation of that surface in the membrane portion) forms the first surface, and a second part being a buried layer,
25 the buried layer being heavily doped and having a concentration gradient the same as the heavily doped layer.
12. A device according to claim 11, having at least two

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semiconductor regions constituting at least one active element in the body, at least one of the isolation regions separating the active element from the resistor layers.

13. A device according to claim 12, having additional
5 buried layers in the body below the active element(s), the additional buried layers being of opposite conductivity type to the isolation regions.

14. A semiconductor device having a pressure sensor substantially as herein described with reference to and as
10 illustrated in Figs. 4 to 8, or Figs. 10 and 11, or Fig. 12, or Figs. 13 to 19, or Figs. 20 and 21 of the accompanying drawings.

15. A method of manufacturing a semiconductor device having a pressure sensor, the method comprising forming in
15 a semiconductor body a heavily doped buried layer; forming semiconductor resistor layers in a first surface of the semiconductor body; and etching the semiconductor body from the opposite side to that in which the resistor layers are formed, to a depth extending partially into the buried
20 layer, so as to form a membrane layer containing the resistor layers and a part of the heavily doped layer, to expose the buried layer at a second surface, wherein the buried layer has a concentration gradient in a direction substantially perpendicular to the second surface such that
25 the impurity concentration increases in a direction away from the second surface.

16. A method of manufacturing a semiconductor device



according to claim 14, wherein said semiconductor body includes the (100) plane.

17. A method of manufacturing a semiconductor device according to claim 15 or claim 16, wherein the etching step
5 is performed by anisotropic etching with an alkali etchant.

18. A method of manufacturing a semiconductor device according to any one of claims 15 to 17, wherein the semiconductor body consists of a p-type silicon substrate on which an n-type silicon layer is grown epitaxially, and
10 the heavily doped layer is an n⁺-type layer which is formed in a selected part of the silicon substrate before the growth of the epitaxial silicon layer.

19. A method of manufacturing a semiconductor device according to claim 18, wherein the impurity concentration
15 of the n⁺-type heavily doped layer has a peak value of at least 10¹⁹ atoms/cm³.

20. A method according to any one of the preceding claims, wherein the heavily doped layer is produced by forming a heavily doped region in a surface of a semiconductor substrate, and forming an epitaxial layer over
20 the surface of the substrate, the resistor layers being formed in the epitaxial layer.

21. A method according to claim 20, wherein further heavily doped buried layers are formed simultaneously with
25 the said buried layer.

22. A method according to claim 21, wherein impurity is introduced into parts of the epitaxial layer to form doped

(51)



regions of the same conductivity type as the further buried layers, the doped regions and the further buried layers forming isolation regions.

23. A method according to claim 22 wherein layers of
5 opposite conductivity type to the said buried layer are formed in the substrate prior to the formation of the epitaxial layer, those layers including a first layer overlying the heavily doped layer, and second layers, such that the second layers are subsequently isolated from the
10 heavily doped layer by the isolation regions.

24. A method according to claim 23, wherein semiconductor regions forming at least one active element are formed in the epitaxial layer above the second layers, and metal wiring layers are formed connecting the resistor layers and
15 the active element(s).

25. A method of manufacturing a semiconductor device having a pressure sensor substantially as herein described with reference to Figs. 4 to 8, or Figs. 10 and 11, or Fig. 12, or Figs. 13 to 19, or Figs. 20 and 21 of the accomp-
20 anying drawings.
