

Description

This invention relates to a sawtooth generator that produces S-corrected signal for a television deflection system. In particular, it relates to such generator that may be used in, for example, a deflection system, arranged for reducing the visibility of flicker.

The threshold of perception of field flicker in a television display system is a function of the flicker frequency and the brightness of the display. Over the years, displays have increased in brightness to the point where flicker is noticeable even in relatively high field rate systems (e.g., the NTSC 60 Hz system) and clearly objectionable in lower field rate systems (e.g., the PAL 50 Hz system). A solution to this problem is to double the field rate of displayed images. In one prior art system, a video input signal is stored in a field memory. Each stored field is recovered or "read" twice from the memory and displayed at double the line rate and double the field rate of the incoming video signal, thereby doubling the flicker frequency of displayed images and thus reducing the visibility of flicker.

In U.S. Patent US-A-4701793 entitled, TELEVISION DISPLAY SYSTEM WITH FLICKER REDUCTION PROCESSOR, issued to W. den Hollander, et al on 20 October 1987, a television display arrangement that provides flicker reduction is described. In the den Hollander arrangement, an interlaced baseband television input signal having a given field rate is provided. A timing unit, responsive to the video input signal, supplies a vertical synchronizing signal having a pulse waveform that repeats on a four-field basis. The pulses of the pulse waveform cause a corresponding phase modulation of the deflection current such that the durations of corresponding vertical scanning cycles vary on a field basis and repeat on a four field basis.

A conventional vertical deflection circuit may include a sawtooth generator, synchronized to a synchronizing signal having a constant phase that generates a drive signal having a sawtooth waveform. In the sawtooth generator, a capacitor is discharged during retrace by a switch, and charged during trace by a current source. The drive signal is coupled to a switching circuit that produces a deflection current having a corresponding sawtooth waveform. The drive signal includes a ramping portion that corresponds with vertical trace such that the beginning time of the ramping portion corresponds with a deflection current that causes scanning at the top of the raster of the display.

Because of the phase modulation of the pulse waveform of the vertical synchronizing signal that is required in, for example, the den Hollander, et al. arrangement, the peak amplitude of the drive signal

at the end of vertical trace may also change on a field basis in accordance with the pulse waveform pattern.

Different peak amplitudes of the drive signal may cause the beginning time of the ramping portion to be different relative to the corresponding pulse of the vertical synchronizing signal that causes such ramping portion. This is so because the discharge time of the capacitor of the sawtooth generator may vary in accordance with the peak amplitude of the drive signal that may be different in different fields. The result is that the phase of the trace portion of the deflection current may, disadvantageously, vary from that established by the phase modulated vertical synchronizing signal. Consequently, the requirement that even field should overlap even field, odd field should overlay odd field and even and odd field pairs should interlace, disadvantageously may not be fulfilled.

Therefore, it may be desirable in each deflection cycle to prevent, for example, the beginning time of the ramping portion of the drive signal from being substantially affected by variations in an amplitude, such as the peak amplitude, of the drive signal.

It may also be desirable to generate the drive signal such that a nonlinearity type distortion, that is discussed below, is corrected by S-shaping of the sawtooth waveform of the drive signal. Nonlinearity distortion may be attributable to the fact that the effective center of deflection of the electron beam is not coincident with the center of radius of curvature of the screen of the kinescope. A common method of compensating for such nonlinearity is to form a deflection current that, rather than being a substantially linear ramp during the recurrent scanning intervals, becomes a segment of a sinewave having a reduction in the rate of change of deflection current at the positive and negative extremes of the deflection current relative to that at the center. This S-shaping in turn creates a slight reduction in the rate of scanning of the electron beam near the top and bottom edges of the raster relative to the center and a reduction in such nonlinearity.

In some prior art vertical deflection circuits, the S-shaping of the deflection current that corresponds with, for example, the one extreme of vertical trace is done by S-shaping the drive signal that is generated in the sawtooth generator. S-shaping of the deflection current that corresponds with the other extreme of vertical trace is controlled by, for example, a voltage that is developed in a capacitor that couples the drive signal of the sawtooth generator to a vertical amplifier.

As explained in the patent to Den Hollander, et al., it may be desirable to DC-couple the drive signal to the deflection winding. Therefore, the

above-mentioned way of S-shaping that utilizes capacitive coupling may not be suitable.

FR-A-1467113 discloses a television deflection apparatus responsive to a synchronizing input signal at a frequency that is related to a deflection frequency, comprising: a controllable switch responsive to said input signal that operates at a frequency that is related to that of said input signal; first and second capacitors forming a series arrangement that is coupled to said switch; a current source coupled to said capacitors for charging said capacitors to generate a sawtooth signal having a ramping first portion that changes in a first direction when said switch is nonconductive such that when said switch becomes conductive said switch discharges said capacitors to form a ramping second portion of said sawtooth signal that changes in an opposite direction; and a source of a ramping voltage related to the generated sawtooth signal. The disclosure of this document corresponds to the introductory portions of the independent claims.

In accordance with a first aspect of the present invention there is provided a television deflection apparatus responsive to a synchronizing input signal at a frequency that is related to a deflection frequency, comprising: a controllable switch responsive to said input signal that operates at a frequency that is related to that of said input signal; first and second capacitors forming a series arrangement that is coupled to said switch; a current source coupled to said capacitors for charging said capacitors to generate a sawtooth signal having a ramping first portion that changes in a first direction when said switch is nonconductive such that when said switch becomes conductive said switch discharges said capacitors to form a ramping second portion of said sawtooth signal that changes in an opposite direction; and a source of a ramping voltage related to the generated sawtooth signal; characterized by a first impedance coupled to said source of said ramping voltage and to a first junction terminal that is coupled between said first and second capacitors for generating a first current that flows in said first impedance that controls S-shaping of said sawtooth signal by reducing the rate of change of said sawtooth signal at one of the beginning and end of one of said first and second portions of said sawtooth signal in accordance with said first current that flows in said first impedance; a second impedance coupled to a terminal of said first impedance that is remote from said first junction terminal for bypassing a portion of a current that flows in a current path between said source of said ramping voltage and said first junction terminal for reducing said first current in said first impedance and that reduces the rate of change of said sawtooth signal at the other of the beginning, and end of said one of said first and second portions of

said sawtooth signal to control S-shaping at said other of the beginning and end; a deflection winding; and means responsive to said sawtooth signal for generating a deflection current in said deflection winding that is S-corrected.

In accordance with a second aspect of the present invention there is provided a television deflection apparatus responsive to a synchronizing input signal at a frequency that is related to a deflection frequency, comprising: a controllable switch responsive to said input signal for operating said switch at a frequency that is related to that of said input signal; first and second capacitors forming a series arrangement that is coupled to a terminal of said switch; a source of DC voltage coupled through a first resistor to said capacitors for generating a sawtooth signal at said terminal having a ramping trace portion that changes in a first direction when said switch is nonconductive and a ramping retrace portion that changes in an opposite direction, when said switch is conductive; characterized by an impedance having a first terminal that is coupled to a junction terminal of said first and second capacitors for generating a first current that is coupled to said junction terminal to control S-shaping of said sawtooth signal; means coupled to said first and second capacitors for clamping each corresponding voltage across each of said first and second capacitors, causing each to be at a corresponding predetermined level prior to a beginning time of said trace portion such that each of said corresponding predetermined levels across each of said capacitors is substantially unaffected by an amplitude of said sawtooth signal at an end of said trace portion; a deflection winding; and means responsive to said sawtooth signal that is S-corrected for generating a deflection current in said deflection winding that is S-corrected.

In accordance with a third aspect of the present invention there is provided a television deflection apparatus responsive to a synchronizing input signal at a frequency that is related to a deflection frequency, comprising: a source of said synchronizing input signal; first and second capacitors forming a series arrangement; a source of a first current coupled to said capacitors for charging said capacitors to generate a sawtooth signal having a ramping trace portion that changes in a first direction during trace and a ramping retrace portion of said sawtooth signal that changes in an opposite direction during retrace; and a source of a first voltage at a frequency that is related to that of said input signal; characterized by a first impedance coupled between said source of said first voltage and a junction terminal of said first and second capacitors for generating a second current that is coupled to said junction terminal that provides S-correction to said sawtooth signal; switching means

coupled to said first and second capacitors for establishing prior to a beginning of said trace portion of said sawtooth signal, respective voltages that are developed across the two capacitors at corresponding levels that are substantially unaffected by an amplitude of said sawtooth signal; a deflection winding; and means responsive to said sawtooth signal that is S-corrected for generating a deflection current in said deflection winding that is S-corrected.

A preferred embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawings, of which:

Figure 1 illustrates a vertical scan generator that includes a sawtooth generator embodying an aspect of the invention;

Figures 2a and 2b illustrates waveforms useful for explaining the operation of the circuit of Figure 1;

Figure 3 illustrates a block diagram of a television receiver that includes the generator of Figure 1;

Figures 4A-4D are waveform diagrams illustrating the operation of the receiver that utilizes the generator of Figure 1; and

Figure 5 illustrates waveforms useful for explaining the operation of the arrangement of Figure 1.

Referring to Figure 1, a sync pulse $2V'$ is coupled to a vertical oscillator circuit 501 of a vertical scan generator 64, embodying an aspect of the invention, that may be used in conjunction with a 110° 45AX type picture tube. Pulse $2V'$, that is phase modulated, is generated in a manner that is described later on. Pulse $2V'$ has a nominal frequency of $2f_v$, where f_v is the frequency of the vertical sync in a baseband television signal such as of the NTSC or the PAL standard. Pulses $2V'$ are separated by corresponding intervals of slightly different durations, with the nominal duration being equal to $1/2V$. V represents the vertical scanning interval of 20 milliseconds, in, for example, the PAL standard.

A ramp generator 500 that is controlled by oscillator circuit 501 includes a charging current generating resistor R2 that is coupled to a terminal 500a of series coupled capacitors C_1 and C_2 . Resistor R2 charges capacitors C_1 and C_2 to form a trace portion of a voltage V_0' at terminal 500a. Terminal 500a is driven by an open-collector switching transistor U6a of a comparator U6 for discharging capacitors C_1 and C_2 to form a vertical retrace portion of voltage V_0' . Voltage V_0' is coupled to an inverting input terminal of a comparator U5. A noninverting input terminal of comparator U5 is DC biased by an arrangement that includes a variable hold control resistor R20. Pulse $2V'$ is inverted by OR-gate 1000 and differentiated by a

differentiating network that includes a capacitor C_4 and a resistor R18 to form pulse $2V''$, which is coupled via a capacitor C_5 to the noninverting terminal of comparator U5. An output terminal of comparator U5 forms a voltage V_{U4} on a conductor U4a and is coupled to a noninverting input terminal of comparator U6. An inverting input terminal of comparator U6 is DC biased by a voltage across a resistor R24.

During vertical trace, the voltage at the noninverting input terminal of comparator U5 is more positive than the voltage at the corresponding inverting input terminal. Consequently, voltage V_{U4} is more positive than the voltage at the inverting input terminal of comparator U6. Therefore, output transistor U6a of comparator U6 remains nonconductive.

At the end of trace, when voltage V_0' is at its peak, as illustrated at time t_0 in FIGURE 2b, a leading edge 900 of pulse $2V'$ of FIGURE 1 occurs. As a result of the inversion and differentiation of its leading edge 900, the voltage at the non-inverting input terminal of comparator U5 becomes smaller than at the corresponding inverting input terminal. The result is that voltage V_{U4} changes to a level that is smaller than that at the inverting input terminal of comparator U6, causing switching transistor U6a of comparator U6 to become conductive. Conduction of transistor U6a discharges capacitors C_1 and C_2 , causing voltage V_0' to be at the saturation level of transistor U6a that is approximately zero volts.

When, as a result of leading edge 900 of pulse $2V'$, voltage U4a changes, a time-out capacitor C_6 causes a corresponding voltage change at a noninverting input terminal of a comparator U4, operating as a one-shot, to a level that is below that at the inverting input terminal of comparator U4. Consequently, comparator U4 sustains voltage V_{U4} at the low level for a predetermined interval that is determined by capacitor C_6 and resistors R25 and R26. As long as voltage V_{U4} is at the low level, voltage V_0' remains approximately zero, because output switching transistor U6a of comparator U6 is conductive. Transistor U6a is conductive in intervals that are illustrated schematically in FIGURE 2a such as, for example, between times t_0 and t_2 . Thus, the conduction time of transistor U6a is independent of the duration of input pulse $2V'$. When voltage V_{U4} of FIGURE 1 changes to a high level, the trace portion of voltage V_0' of FIGURE 2b, such as, for example, between times t_2 and t_3 of FIGURE 2b, begins. Thus, when leading edge 900 of pulse $2V'$ occurs, capacitors C_1 and C_2 of FIGURE 1 begin discharging to the saturation voltage level of switching transistor U6a. In the event that pulses $2V'$ of FIGURE 1 are missing, comparators U4, U5 and U6, that form vertical oscillator 501, produce

the required pulses of voltage V_{U4} .

Each pulse of voltage V_{U4} of FIGURE 1 causes output transistor U6a to clamp voltage V_0' to its saturation voltage level for the predetermined duration of voltage pulse V_{U4} , such as until time t_2 of FIGURE 2b, thus preventing voltage V_0' from upramping. Voltage V_0' of FIGURE 1 is coupled via a transistor Q2, operating as an emitter follower, to produce a voltage V_0 of FIGURE 2b having a controllable average value that, like voltage V_0' , is also of a sawtooth waveform.

An upramping, first, or trace portion of voltage V_0' or V_0 , occurs during an interval such as interval t_2 - t_3 . The first portion begins upramping from a predetermined constant level that is equal to the saturation voltage of output switching transistor U6a of comparator U6 of FIGURE 1 in a way that is not affected by phase modulation of pulse $2V'$. Thus, the upramping first portion begins upramping at an instant, such as time t_2 of FIGURE 2b. A downramping second portion of voltage V_0 occurs, for example, during interval t_0 - t_1 . A flat third portion occurs during interval t_1 - t_2 . The phase modulation of the pulses of voltage V_{U4} , shown in FIGURE 2a, that are separated by intervals having correspondingly different lengths, causes correspondingly different peak values of ramp voltage V_0 , to occur such as at times t_0 , t_3 , t_6 and t_9 , respectively, of FIGURE 2b.

The sum of the intervals that correspond with the second and third portions is a predetermined constant that is not affected by the peak value of voltage V_0 of FIGURE 1. The interval between the beginning of the downramping portion and the beginning time of the upramping portion of voltage V_0 , such as interval t_0 - t_2 of FIGURE 2b, may be maintained, illustratively, constant so as to be unaffected by the phase modulation of pulses $2V'$ of FIGURE 1.

Ramp generator 500 includes an S-correction arrangement 700, embodying aspects of the invention. A capacitor C_3 of arrangement 700 is coupled between the emitter electrode of emitter follower transistor Q2 and a terminal 701. Terminal 701 is coupled, via a series arrangement of a variable, linearity control resistor R4 and a resistor R5, to a junction terminal 703. Terminal 703 is coupled between capacitors C_1 and C_2 . A diode D_1 that, during retrace, clamps voltage V_2 , at the junction of capacitors C_1 and C_2 , to a predetermined positive level is coupled between terminal 703 and the emitter of transistor Q2. A diode D_2 that discharges capacitor C_3 , during retrace, is coupled in parallel with a resistor R8 and between ground and terminal 701.

FIGURE 5 illustrates waveforms useful in explaining the operation of the circuit of FIGURE 1.

At the beginning of vertical trace, voltage V_0' of FIGURE 1 is approximately zero, as described before. A positive voltage V_2 at terminal 703, is equal to the sum of saturation voltage V_0' , the emitter-base forward voltage of transistor Q2, and the forward voltage of diode D_1 . Also, voltage V_4 at terminal 701 is slightly negative as a result of the clamping operation of diode D_2 . Because voltage V_2 is more positive than voltage V_4 , capacitor C_2 begins discharging through resistors R5 and R4, and through diode D_1 and capacitor C_3 , at a rate of change that initially is, substantially unaffected by the value of resistor R8, so as to reduce the value of voltage V_2 . Later on, during trace, when an emitter voltage V_3 , shown in FIGURE 5, of transistor Q2 of FIGURE 1 attains a sufficiently high voltage level, capacitor C_2 of FIGURE 1 is charged through capacitor C_3 . The initial decrease in voltage V_2 causes the rate of change of voltage V_0' to be higher at, for example, the center of trace than at its beginning. As described before, the difference between voltages V_2 and V_4 causes a partial discharge of capacitor C_2 , at the beginning of trace. The discharge of capacitor C_2 causes a slower rate of increase of voltage V_3 , as shown in FIGURE 5, that is developed at the emitter of transistor Q2 of FIGURE 1, than at the center of trace. Thus the slower rate of increase provides S-shaping at a first half of trace that occurs between the beginning and the center of trace, as shown in FIGURE 5.

In accordance with an aspect of the invention, during a second half of vertical trace, S-shaping becomes increasingly affected by resistor R8 which increasingly loads capacitor C_2 as voltages V_2 and V_4 increase. Resistor R8 reduces, at the end of trace, the current supplied through capacitor C_3 that is available for charging capacitor C_2 .

Voltage V_4 is higher toward the end of trace than, for example, at the center of trace. Therefore, the current that is supplied through capacitor C_3 that is bypassed by resistor R8 and that is prevented by resistor R8 from flowing in capacitor C_2 becomes increasingly larger toward the end of trace. The result is that voltage V_3 is S-corrected at the second half of trace. It follows that an increase, for example, in the value of resistor R8 changes the rate of change of voltage V_0' at the end of trace in an opposite manner to that caused by an increase of, for example, resistor R4.

In accordance with another aspect of the invention, S-corrected ramp generator 500 produces voltage V_0' in which the rate of change, in a given vertical trace, is independent of vertical frequency variations or of the trace time of a preceding vertical trace. Such result is obtained because of the clamping operation of transistor U6a, diode D_1 and diode D_2 that clamp voltages V_0 , V_4 and V_2 during

retrace.

FIGURE 1, advantageously, also includes a switched vertical deflection circuit 100 of generator 64 that is controlled by a vertical control circuit 120 of generator 64. The operation of deflection circuit 100 and of control circuit 120 is described in detail in U.S. Patent No. 4,544,864 in the name of P.E. Haferl, entitled SWITCHED VERTICAL DEFLECTION CIRCUIT WITH BIDIRECTIONAL POWER SUPPLY. It should be understood that ramp generator circuit 500 may be employed as the sawtooth generator for other types of DC coupled vertical deflection output stages to obtain proper registration of the displayed image.

Control circuit 120 provides, in accordance with voltage V_0 , width modulated horizontal, or line rate, switching signals to a switching element 21, illustratively shown as comprising a field effect transistor 118 and an integrated antiparallel diode 19. Transistor 118 may comprise a MOS power field effect transistor. Using such power field effect transistor is particularly advantageous when the horizontal rate is substantially higher than the horizontal frequency in, for example, the PAL standard. High rate horizontal frequency may be used in computer monitors, video display terminals or in television receivers, operating with deflection currents at, for example, twice the horizontal and vertical deflection frequencies, respectively, for reducing the visibility of flicker. Switching element 21 is coupled to a terminal 126' of a storage capacitor 126 via a winding 23 of a flyback transformer 125 that is series coupled with an energy storage coil 25. Terminal 126' of capacitor 126 is coupled to a vertical deflection winding 27. The other terminal of vertical deflection winding 27 is coupled to a voltage supply designated +V1.

A horizontal output stage 33 is switched at the horizontal deflection rate by signals applied from a horizontal oscillator and driver circuit 134. The switching operation of output stage 33 generates a horizontal deflection current i_{2H} at twice the horizontal frequency, f_H , of the sync signal of a baseband video signal V_{BB} that is mentioned later on. Output stage 33 produces a retrace voltage at the horizontal rate of $2f_H$ across each winding of flyback transformer 125.

Ramping voltage V_0 is fed to a noninverting input terminal of a comparator 66 of FIGURE 1 to control the switching operation of switching element 21. Horizontal retrace pulses from winding 124, applied via a resistor 74, charge a capacitor 75 to obtain a horizontal ramp which is compared with the vertical sawtooth of voltage V_0 . Comparator 66 serves as a pulse width modulator. An output terminal of comparator 66 that generated pulses at the horizontal rate $2f_H$, having variable duty cycle that vary in a vertical manner, provides gate drive

to MOS power field effect transistor 118.

The operation of deflection circuit 100 consists of the horizontal rate charge and discharge of storage capacitor 126 which supplies a vertical deflection current i_{27} that flows in winding 27. Horizontal rate switching is performed by switching element 21.

At the beginning of vertical trace, during each horizontal period, transistor 118 of switching element 21 is conductive for a negligible short interval that occurs immediately prior to each horizontal retrace. Consequently, the large retrace pulse in winding 23 is clamped by diode 19 and generates a current i_{23} that is large in winding 23 flowing in a direction opposite to that of the arrow that causes capacitor 126 to be charged to a voltage that is more positive than voltage +V1. The resulting voltage at terminal 126' that is more positive than voltage +V1 causes negative deflection current i_{27} to flow in deflection winding 27, in a direction opposite to that of the arrow. As a result, deflection current i_{27} charges capacitor C_{12} positively. Control circuit 120 progressively increases, during the vertical scanning trace, the conduction interval of transistor 118 that occurs in each horizontal trace. This causes the negative portion of current i_{23} , flowing through diode 19, to decrease progressively and the positive portion of current i_{23} , flowing through transistor 118, to increase progressively. As a result, the average voltage across capacitor 126 at terminal 126' decreases and causes, in turn, a decrease of deflection current i_{27} .

At the center of vertical trace, equal portions of current i_{23} that are at opposite polarities flow through diode 19 and transistor 118, respectively. Consequently, no charge is added to capacitor 126. Also, the voltage at terminal 126' is equal to voltage +V1; therefore, deflection current i_{27} , at the center of vertical trace, is zero.

During the second half of the vertical trace, control circuit 120 further increases progressively the conduction time of transistor 118. The sum of the portions of current i_{23} at the opposite polarity, flowing through diode 19 and transistor 118, respectively, increases progressively in the positive direction from zero, causing capacitor 126 to discharge. The voltage at terminal 126' decreases progressively and causes deflection current i_{27} that flows in the direction of the arrow to increase. As a result, deflection current i_{27} discharges capacitor C_{12} . At the end of trace, the conduction time of diode 19 is small compared with that of transistor 118. The conduction of diode 19 is controlled by transistor 118 and by energy storage coil 25 which determines the rate di/dt of current i_{23} that is substantially constant during each horizontal retrace period. It follows that from the beginning to the end of vertical trace deflection current i_{27}

changes in an upramping manner and reverses polarity at approximately the center of vertical trace.

During vertical retrace, transistor 118 is non-conductive and diode 19 conducts a large amount of negative current i_{27} ; consequently, deflection winding 27 and capacitor 126 cause a half cycle of oscillation. A resulting vertical retrace voltage charges capacitor 126 to a voltage that is larger than voltage $+V_1$ that causes deflection current i_{27} to reverse its polarity.

It can be seen that the current through resistor 122 is equal to the deflection current i_{27} . Therefore, the voltage developed across resistor 122 is proportional to current i_{27} , the vertical deflection current. The voltage developed across deflection current sampling resistor 122 is produced by deflection current i_{27} and provides negative feedback to vertical control circuit 120. This feedback provides information to vertical control circuit 120 to enable the driving of transistor 118 into conduction for the appropriate duration each horizontal interval to generate vertical deflection current i_{27} . Current i_{27} , during vertical trace, is linearly proportional to sawtooth ramp voltage V_0' or V_0 .

When the leading edge 900 of pulse $2V'$ occurs, such as, for example, immediately prior to time t_0 of FIGURE 2b, the downramping, second portion of voltage V_0 begins. The beginning of the downramping portion of voltage V_0 causes deflection current i_{27} in winding 27 of FIGURE 1 to begin its corresponding downramping retrace portion. When a trailing edge of the pulse of voltage V_{U4} occurs, the upramping trace portion of deflection current i_{27} of FIGURE 1 begins. Voltage V_0 controls the instantaneous level of deflection current i_{27} during the vertical trace portion of deflection current i_{27} .

In each vertical scanning cycle, each of the voltages V_0 , V_2 , V_3 and V_4 is at the same corresponding predetermined voltage level when the trailing edge of the pulse of voltage V_{U4} occurs, because of the clamping operation as described before. Consequently, as described later on, proper image registration is obtained. The phase modulation of pulse $2V'$ results in a modulation of the vertical trace time. Capacitors C_1 , C_2 and C_3 provide "S" shaping, as described before. Clamping the voltage across each of capacitors C_1 , C_2 and C_3 during pulse V_{U4} establishes in each such capacitor the corresponding predetermined charge or voltage level at the beginning of each trace interval in a way that is unaffected by the duration of the trace interval of any previous field. Without the clamping action of diodes D_1 and D_2 , each of capacitors C_1 , C_2 , and C_3 would have carried slightly modulated charge from previous fields which may upset proper image registration. Be-

cause of the clamping action in capacitors C_1 , C_2 and C_3 , the ramping trace portion in each deflection cycle of both voltage V_0 and of deflection current i_{27} of FIGURE 1 is in phase with, and follows phase variations of, the corresponding leading edge 900 of pulse $2V'$.

As described later on, the phase modulation of pulse $2V'$ provides the precise timing that is required to provide a displayed image in which proper image registration occurs such that even fields overlay even fields, odd fields overlay odd fields and such that even and odd field pairs are interlaced.

It should be understood that as a result of the way the waveform of voltage V_0 or V_0' of FIGURE 2b is generated, the interval from the end of vertical trace of a given deflection cycle of deflection current i_{27} of FIGURE 1 to the beginning of vertical trace of the following deflection cycle is also constant.

The DC component of the vertical sawtooth of voltage V_0 or V_0' of FIGURE 2b should be, preferably, preserved and transmitted to deflection winding 27 of FIGURE 1. DC coupling may, preferably, be used between sawtooth generator circuit 500 and vertical deflection circuit 100 as well as to deflection winding 27. DC coupling is preferred so that the phase modulation of pulse $2V'$ does not change the level of deflection current i_{27} that corresponds with a given level of voltage V_0 such as at the beginning of trace.

Height control is provided by a variable resistor R_6 that controls, by control of a source voltage V_5 , the rate by which capacitors C_1 and C_2 are charged, during trace. Centering is provided by a variable resistor R_{10} that is responsive to voltage V_5 for controlling the average value of voltage V_0 . Voltage V_5 , at a terminal 999 of resistor R_2 , is proportional to both the sawtooth AC portion of voltage V_0 and also to its DC average level. Therefore, voltage V_5 forms a DC reference for deflection circuit 100 that maintains picture centering while picture height is being adjusted by varying resistor R_6 .

The features of deflection current i_{27} , that were mentioned before, may be useful, for example, in a television receiver circuit of FIGURE 3, that is similar to that described in the aforementioned den Hollander patent, where the vertical deflection current is phase and amplitude modulated in accordance with a phase modulated vertical sync signal.

The receiver of FIGURE 3, that generates pulse $2V'$ of FIGURE 1, includes a tuner 10 having an input terminal 12 for connection to an antenna or other source of video input signal and having an output for supplying baseband video output signal V_{BB} , that was mentioned before, to a video processing unit 14. For purposes of illustration, it will

be assumed that the baseband video output signal is of the PAL standard. It will be appreciated, however, that the principles of the invention also apply to other standard interlaced video signal formats. Video processor 14 includes a PAL decoder that converts the input signal to Y, R-Y and B-Y component signals. The signal could be processed, if desired, in R, G, B component form. R, G, B components each have full video bandwidth while the color difference signals (R-Y, B-Y) have a lower bandwidth. Accordingly, a field store for color difference signals can be realized with fewer memory elements than would be the case if processing were done using R, G, B components.

The Y, R-Y and B-Y component signals are low pass filtered by filters 16, 18 and 20 and converted to digital form by analog-to-digital (A/D) converters 22, 24 and 26 for storage in a memory 40. Filters 16-20 minimize aliasing and have cutoff frequencies of 7.5 MHz for Y and 2.8 MHz for the color difference signals R-Y and B-Y for the assumed PAL input signal. Lower cut off frequencies would be appropriate for NTSC signals.

Converters 22-26 digitize the low pass filtered components to an 8-bit resolution using a sample clock CL that is phase locked to a multiple of horizontal sync in order to obtain a constant number of samples per horizontal line. After A/D conversion, the digitized components are applied to memory 40 via respective delay units 28, 30 and 32. The delay units may be variable and are included to equalize the delay times of the three input signal paths. The color difference components R-Y and B-Y are applied to memory 40 via a multiplex switch (MUX) 34 controlled by a horizontal line rate signal H. Switch 34 combines the two 8-bit wide color difference signals into a single 8-bit wide signal to minimizing storage requirements in memory 40.

As one field of the multiplexed 8-bit signal and the 8-bit luma signal are stored in memory 40, a field previously stored is read out twice using a read clock signal 2 CL of double the write clock CL frequency. This doubles the field rate (100 Hz for PAL, 120 Hz for NTSC) and so reduces the perception of flicker where the signal is displayed on display unit 60. A multiplex switch 42 demultiplexes the color difference signals which, with the double field rate luma signal, are converted back to analog form by digital to analog converters 44-48. Low pass filters 50-54 suppress the repeat spectra after D/A conversion, suitable cut-off frequencies being 13.5 MHz for luma and 6.75 MHz for chroma. The double field rate analog signals are then converted to R G B form for application to display unit 60 which is synchronized by means of double speed horizontal deflection current i_{2H} and vertical deflection current i_{2V} provided by horizontal and

vertical scan generators 62 and 64, respectively. Generator 62 generates deflection current i_{2H} at twice the frequency f_H of the horizontal sync of baseband video output signal V_{BB} .

A field consists of 312.5 lines in the PAL standard. At double speed read-out, this field together with its repetition must consist of 625 lines. This can be realized when one of the two fields consists of 312 lines and the other consists of 313 lines. Memory 40 of FIGURE 3 is supplied with timing signals from timing unit 70 to provide the field sequence shown in FIGURE 4A in which 312 lines are produced in the first read cycle (fields A or B) and 313 lines are produced during the second memory read cycle (field A' or B') with the 313th line being blank.

The double field rate vertical sync pulse $2V'$ required for generator 64 has the pulse pattern illustrated in solid line in FIGURE 4B. For comparison purposes, pulses in dashed-line are provided, which represent a situation of equidistant double rate vertical sync pulses having a period of 312.5 line. The solid line pulses represent pulse signal $2V'$ of FIGURES 1 and 3, which is periodic on a four-field basis. As shown, there are 312 lines in field A, 312.5 lines in the repeat field A', 312 lines in field B and 313.5 lines in repeat field B'. Pulse $2V'$ controls vertical deflection generator 100, as described before, to produce the vertical scan waveforms of vertical deflection current i_{2V} . The vertical trace portions of current i_{2V} are shown schematically in FIGURE 4C. The scanning current waveform sequence of FIGURE 4c results in the interlace pattern shown in FIGURE 4D in which the first fields (A, A') overlay first fields, the second fields overlay second fields (B, B') and in which the first and second field pairs (AA', BB') are interlaced. For purpose of comparison, the dashed lines in FIG. 4D illustrate scan lines which would result if sync pulses $2V'$ of FIGURE 4B were equidistant rather than being shifted or phase modulated. To ensure proper registration of displayed fields, the sawtooth voltage of FIG. 4C, provided by generator circuit 500, that was described before, always starts at the same value; all retrace times (T_0-T_0' , T_1-T_1' , T_2-T_2' , etc.) are equal.

Timing signals for controlling the digital converters, memory, switches and scan generators are provided by timing unit 70 of FIGURE 3. Unit 70 generates, as described in the den Hollander patent, two-field and four-field pulse sequences for memory control and for scan generation of pulse $2V'$ for ensuring that even fields overlay even fields, odd fields overlay odd fields, and that even and odd pairs of fields are interlaced when the double field rate signal is displayed.

Ramp generator circuit 500 and vertical oscillator circuit 501 of FIGURE 1, embodying aspects of

the invention, reduce or eliminate any tendency for variation in the phase of the trace portion of deflection current i_{27} relative to the irregularly spaced double field rate vertical sync pulse $2V'$ over the four field sequence.

Claims

1. A television deflection apparatus responsive to a synchronizing input signal ($2V'$) at a frequency that is related to a deflection frequency, comprising:

a controllable switch (U_{6a}) responsive to said input signal that operates at a frequency that is related to that of said input signal ($2V'$);

first (C_1) and second (C_2) capacitors forming a series arrangement that is coupled to said switch (U_{6a});

a current source (R_2) coupled to said capacitors (C_1, C_2) for charging said capacitors to generate a sawtooth signal (V_o') having a ramping first portion that changes in a first direction when said switch (U_{6a}) is nonconductive such that when said switch becomes conductive said switch (U_{6a}) discharges said capacitors (C_1, C_2) to form a ramping second portion of said sawtooth signal (V_o') that changes in an opposite direction; and

a source (500) of a ramping voltage (V_3) related to the generated sawtooth signal; characterized by;

a first impedance (R_4, R_5) coupled to said source (500) of said ramping voltage (V_3) and to a first junction terminal (703) that is coupled between said first (C_1) and second (C_2) capacitors for generating a first current that flows in said first impedance (R_4, R_5) that controls S-shaping of said sawtooth signal (V_o') by reducing the rate of change of said sawtooth signal (V_o') at one of the beginning and end of one of said first and second portions of said sawtooth signal in accordance with said first current that flows in said first impedance (R_4, R_5);

a second impedance (R_6) coupled to a terminal (701) of said first impedance (R_4, R_5) that is remote from said first junction terminal (703) for bypassing a portion of a current that flows in a current path between said source (500) of said ramping voltage (V_3) and said first junction terminal (703) for reducing said first current in said first impedance (R_4, R_5) and that reduces the rate of change of said sawtooth signal (V_o') at the other of the beginning and end of said one of said first and second portions of said sawtooth signal (V_o') to control S-shaping at said other of the beginning and end;

a deflection winding (27); and

means (100) responsive to said sawtooth signal (V_o') for generating a deflection current in said deflection winding (27) that is S-corrected.

2. An apparatus according to Claim 1 characterized by a third capacitor (C_3) for capacitively coupling said ramping voltage (V_3) to said first junction terminal (703).
3. An apparatus according to Claim 2 characterized in that said source of ramping voltage (500) comprises a voltage follower (Q_2) having an input terminal (500a) that is responsive to said sawtooth signal (V_o') and wherein said third capacitor (C_3) is coupled between an output terminal (emitter) of said voltage follower (Q_2) and a terminal (701) of said first impedance (R_4, R_5) that is remote from said first junction terminal (703).
4. An apparatus according to Claim 2 characterized in that said first (R_4, R_5) and second (R_6) impedances comprise corresponding first and second resistances wherein said third capacitor (C_3) and said first resistance (R_4, R_5) form a current path for discharging said second capacitor (C_2) at said one of the beginning and end of said portion that corresponds with a trace interval of said deflection current and for charging said second capacitor (C_2) at said other of said beginning and end of said portion that corresponds with said trace interval such that, at said other of the beginning and end, said second impedance (R_6) reduces the rate by which said second capacitor (C_2) is charged.
5. A television deflection apparatus responsive to a synchronizing input signal ($2V'$) at a frequency that is related to a deflection frequency, comprising:

a controllable switch (U_{6a}) responsive to said input signal for operating said switch (U_{6a}) at a frequency that is related to that of said input signal ($2V'$);

first (C_1) and second (C_2) capacitors forming a series arrangement that is coupled to a terminal (500a) of said switch (U_{6a});

a source (V_5) of DC voltage coupled through a first resistor (R_2) to said capacitors (C_1, C_2) for generating a sawtooth signal (V_o') at said terminal (500a) having a ramping trace portion that changes in a first direction when said switch (U_{6a}) is nonconductive and a ramping retrace portion that changes in an opposite direction, when said switch (U_{6a}) is conductive; characterized by

the invention, reduce or eliminate any tendency for variation in the phase of the trace portion of deflection current i_{27} relative to the irregularly spaced double field rate vertical sync pulse $2V$ over the four field sequence.

Claims

1. A television deflection apparatus responsive to a synchronizing input signal ($2V$) at a frequency that is related to a deflection frequency, comprising:

a controllable switch (U_{8a}) responsive to said input signal that operates at a frequency that is related to that of said input signal ($2V$);

first (C_1) and second (C_2) capacitors forming a series arrangement that is coupled to said switch (U_{8a});

a current source (R_2) coupled to said capacitors (C_1, C_2) for charging said capacitors to generate a sawtooth signal (V_o') having a ramping first portion that changes in a first direction when said switch (U_{8a}) is nonconductive such that when said switch becomes conductive said switch (U_{8a}) discharges said capacitors (C_1, C_2) to form a ramping second portion of said sawtooth signal (V_o') that changes in an opposite direction; and

a source (500) of a ramping voltage (V_3) related to the generated sawtooth signal; characterized by;

a first impedance (R_4, R_5) coupled to said source (500) of said ramping voltage (V_3) and to a first junction terminal (703) that is coupled between said first (C_1) and second (C_2) capacitors for generating a first current that flows in said first impedance (R_4, R_5) that controls S-shaping of said sawtooth signal (V_o') by reducing the rate of change of said sawtooth signal (V_o') at one of the beginning and end of one of said first and second portions of said sawtooth signal in accordance with said first current that flows in said first impedance (R_4, R_5);

a second impedance (R_8) coupled to a terminal (701) of said first impedance (R_4, R_5) that is remote from said first junction terminal (703) for bypassing a portion of a current that flows in a current path between said source (500) of said ramping voltage (V_3) and said first junction terminal (703) for reducing said first current in said first impedance (R_4, R_5) and that reduces the rate of change of said sawtooth signal (V_o') at the other of the beginning and end of said one of said first and second portions of said sawtooth signal (V_o') to control S-shaping at said other of the beginning and end;

a deflection winding (27); and

means (100) responsive to said sawtooth signal (V_o') for generating a deflection current in said deflection winding (27) that is S-corrected.

2. An apparatus according to Claim 1 characterized by a third capacitor (C_3) for capacitively coupling said ramping voltage (V_3) to said first junction terminal (703).

3. An apparatus according to Claim 2 characterized in that said source of ramping voltage (500) comprises a voltage follower (Q_2) having an input terminal (500a) that is responsive to said sawtooth signal (V_o') and wherein said third capacitor (C_3) is coupled between an output terminal (emitter) of said voltage follower (Q_2) and a terminal (701) of said first impedance (R_4, R_5) that is remote from said first junction terminal (703).

4. An apparatus according to Claim 2 characterized in that said first (R_4, R_5) and second (R_8) impedances comprise corresponding first and second resistances wherein said third capacitor (C_3) and said first resistance (R_4, R_5) form a current path for discharging said second capacitor (C_2) at said one of the beginning and end of said portion that corresponds with a trace interval of said deflection current and for charging said second capacitor (C_2) at said other of said beginning and end of said portion that corresponds with said trace interval such that, at said other of the beginning and end, said second impedance (R_8) reduces the rate by which said second capacitor (C_2) is charged.

5. A television deflection apparatus responsive to a synchronizing input signal ($2V$) at a frequency that is related to a deflection frequency, comprising:

a controllable switch (U_{8a}) responsive to said input signal for operating said switch (U_{8a}) at a frequency that is related to that of said input signal ($2V$);

first (C_1) and second (C_2) capacitors forming a series arrangement that is coupled to a terminal (500a) of said switch (U_{8a});

a source (V_5) of DC voltage coupled through a first resistor (R_2) to said capacitors (C_1, C_2) for generating a sawtooth signal (V_o') at said terminal (500a) having a ramping trace portion that changes in a first direction when said switch (U_{8a}) is nonconductive and a ramping retrace portion that changes in an opposite direction, when said switch (U_{8a}) is conductive; characterized by



an impedance (C_3, R_4, R_5) having a first terminal that is coupled to a junction terminal (703) of said first (C_1) and second (C_2) capacitors for generating a first current that is coupled to said junction terminal (703) to control S-shaping of said sawtooth signal;

means (D_1, D_2) coupled to said first (C_1) and second (C_2) capacitors for clamping each corresponding voltage across each of said first (C_1) and second (C_2) capacitors, causing each to be at a corresponding predetermined level prior to a beginning time of said trace portion such that each of said corresponding predetermined levels across each of said capacitors is substantially unaffected by an amplitude of said sawtooth signal at an end of said trace portion;

a deflection winding (27); and

means (100) responsive to said sawtooth signal (V_o') that is S-corrected for generating a deflection current (i_{27}) in said deflection winding (27) that is S-corrected.

6. An apparatus according to Claim 5 characterized in that said impedance includes a third capacitor (C_3) and wherein said clamping means (D_1, D_2) is coupled to said third capacitor (C_3) for clamping a voltage across said third capacitor (C_3), causing it to be at corresponding predetermined level prior to said beginning time of said trace portion.

7. An apparatus according to Claim 5 characterized in that said clamping means comprises a diode (D_1, D_2).

8. A television deflection apparatus responsive to a synchronizing input signal ($2V'$) at a frequency that is related to a deflection frequency, comprising:

a source of said synchronizing input signal ($2V'$);

first (C_1) and second (C_2) capacitors forming a series arrangement;

a source (R_2) of a first current coupled to said capacitors for charging said capacitors to generate a sawtooth signal (V_o') having a ramping trace portion that changes in a first direction during trace and a ramping retrace portion of said sawtooth signal (V_o') that changes in an opposite direction during retrace; and

a source (500) of a first voltage (V_3) at a frequency that is related to that of said input signal ($2V'$); characterised by

a first impedance (C_3, R_4, R_5) coupled between said source (500) of said voltage (V_3) and a junction terminal (703) of said first (C_1) and second (C_2) capacitors for generating a

second current that is coupled to said junction terminal (703) that provides S-correction to said sawtooth signal (V_o');

switching means (U_{6a}) coupled to said first (C_1) and second (C_2) capacitors for establishing prior to a beginning of said trace portion of said sawtooth signal, respective voltages that are developed across the two capacitors at corresponding levels that are substantially unaffected by an amplitude of said sawtooth signal;

a deflection winding (27); and

means (100) responsive to said sawtooth signal (V_o') that is S-corrected for generating a deflection current (i_{27}) in said deflection winding (27) that is S-corrected.

9. An apparatus according to Claim 8 characterized in that said first impedance includes a third capacitor (C_3) and that a second impedance (R_8) is coupled to said third capacitor (C_3) for bypassing a portion of a current that flows in said third capacitor (C_3) for reducing said second current such that by reducing said second current, a rate of change of said sawtooth signal (V_o') at an end time of said trace portion becomes smaller.

Patentansprüche

1. Ablenkvorrichtung für einen Fernsehempfänger, die auf ein synchronisierendes Eingangssignal ($2V'$) mit einer auf eine Ablenkfrequenz bezogenen Frequenz anspricht, mit:

einem steuerbaren Schalter (U_{6a}), der auf das Eingangssignal anspricht und mit einer Frequenz arbeitet, die auf die des Eingangssignals ($2V'$) bezogen ist;

ersten (C_1) und zweiten (C_2) Kondensatoren, die eine mit dem Schalter (U_{6a}) verbundene Reihenanordnung bilden;

einer mit den Kondensatoren (C_1, C_2) verbundenen Stromquelle (R_2) zur Ladung der Kondensatoren, um ein Sägezahnsignal (V_o') mit einem ersten ansteigenden Teil zu erzeugen, der sich in einer ersten Richtung ändert, wenn der Schalter (U_{6a}) nicht leitend ist, so daß der Schalter (U_{6a}) beim Leitendwerden die Kondensatoren (C_1, C_2) entlädt, um einen zweiten ansteigenden Teil des Sägezahnsignals (V_o') zu erzeugen, der sich in entgegengesetzter Richtung ändert, und

einer Quelle (500) einer ansteigenden Spannung (V_3), die auf das erzeugte Sägezahnsignal bezogen ist, gekennzeichnet durch:

eine erste Impedanz (R_4, R_5), die mit der Quelle (500) der ansteigenden Spannung (V_3) und einer ersten Verbindungsklemme (703)



zwischen den beiden Kondensatoren (C_1 , C_2) verbunden ist, um einen ersten Strom zu erzeugen, der in der ersten Impedanz (R_4 , R_5) fließt, der die S-Formung des Sägezahnsignals (V_o) steuert, indem die Änderungsrate des Sägezahnsignals (V_o) an einem der Zustände Anfang oder Ende des ersten oder zweiten Teils des Sägezahnsignals gemäß dem ersten Strom vermindert wird, der in der ersten Impedanz (R_4 , R_5) fließt;

eine zweite Impedanz (R_8), die mit einer Klemme (701) der ersten Impedanz (R_4 , R_5) verbunden ist, die der ersten Verbindungsklemme (703) abgekehrt ist, um für einen Teil des Stroms, der in dem Stromweg zwischen der Quelle (500) der ansteigenden Spannung (V_3) und der ersten Verbindungsklemme (703) fließt, einen Nebenschluß zu schaffen, damit der erste Strom in der ersten Impedanz (R_4 , R_5) vermindert wird, und der die Änderungsrate des Sägezahnsignals (V_o) am anderen der Zustände Anfang oder Ende des ersten oder zweiten Teils des Sägezahnsignals (V_o) vermindert, um die S-Formung am anderen der Zustände Anfang oder Ende zu steuern;

eine Ablenkwicklung (27); und

Mittel (100), die auf das Sägezahnsignal (V_o) ansprechen, um in der Ablenkwicklung (27) einen S-korrigierten Ablenkstrom zu erzeugen.

2. Vorrichtung nach Anspruch 1, gekennzeichnet durch einen dritten Kondensator (C_3), um die ansteigende Spannung (V_3) der ersten Verbindungsklemme (703) kapazitiv zuzuführen.
3. Vorrichtung nach Anspruch 2, dadurch gekennzeichnet, daß die Quelle der ansteigenden Spannung (500) einen Spannungsfolger (Q_2) mit einer Eingangsklemme (500a) umfaßt, der auf das Sägezahnsignal (V_o) anspricht, wobei der dritte Kondensator (C_3) zwischen einer Ausgangsklemme (Emitter) des Spannungsfolgers (Q_2) und einer Klemme (701) der ersten Impedanz (R_4 , R_5) liegt, die der ersten Verbindungsklemme (703) abgekehrt ist.
4. Vorrichtung nach Anspruch 2, dadurch gekennzeichnet, daß die erste (R_4 , R_5) und die zweite Impedanz (R_8) entsprechende erste und zweite Widerstände umfassen, wobei der dritte Kondensator (C_3) und der erste Widerstand (R_4 , R_5) einen Stromweg zur Entladung des zweiten Kondensators (C_2) an einem der Zustände Anfang oder Ende des Teils bilden, der einem Vorlaufintervall des Ablenkstroms entspricht, und um den zweiten Kondensator (C_2) am anderen der Zustände Anfang oder Ende zu la-

den, der dem Vorlaufintervall so entspricht, daß am anderen Zustand Anfang oder Ende die zweite Impedanz (R_8) die Rate vermindert, mit der der zweite Kondensator (C_2) geladen wird.

5. Ablenkvorrichtung für einen Fernsehempfänger, die auf ein synchronisierendes Eingangssignal (2V') mit einer auf eine Ablenkfrequenz bezogenen Frequenz anspricht: mit

einem steuerbaren Schalter (U_{8a}), der auf das Eingangssignal anspricht, um den Schalter (U_{8a}) mit einer Frequenz zu betätigen, die auf die des Eingangssignals (2V') bezogen ist;

ersten (C_1) und zweiten (C_2) Kondensatoren, die eine mit einer Klemme (500a) des Schalters (U_{8a}) verbundene Reihenanzordnung bilden;

einer Gleichspannungsquelle (V_5), die über einen ersten Widerstand (R_2) mit den Kondensatoren (C_1 , C_2) verbunden ist, um an der Klemme (500a) ein Sägezahnsignal (V_o) zu erzeugen, das einen ansteigenden Vorlaufteil hat, der sich in einer ersten Richtung ändert, wenn der Schalter (U_{8a}) nicht leitend ist, und das einen ansteigenden Rücklaufteil hat, der sich in entgegengesetzter Richtung ändert, wenn der Schalter (U_{8a}) leitend ist; gekennzeichnet durch:

eine Impedanz (C_3 , R_4 , R_5) mit einer ersten Klemme, die mit einer Verbindungsklemme (703) des ersten (C_1) und des zweiten (C_2) Kondensators verbunden ist, um einen ersten Strom zu erzeugen, der der Verbindungsklemme (703) zugeführt wird, um die S-Formung des Sägezahnsignals zu steuern;

Mittel (D_1 , D_2), die mit dem ersten (C_1) und dem zweiten (C_2) Kondensator verbunden sind, um die entsprechenden Spannungen über dem ersten (C_1) und dem zweiten (C_2) Kondensator zu klemmen, und um zu bewirken, daß jeder auf einem vorgegebenen Pegel vor einer Anfangszeit des Vorlaufteils ist, so daß die vorgegebenen Pegel über den Kondensatoren an einem Ende des Vorlaufteils durch eine Amplitude des Sägezahnsignals weitgehend unbeeinträchtigt sind;

eine Ablenkwicklung (27); und

Mittel (100), die auf das Sägezahnsignal (V_o) ansprechen, um einen Ablenkstrom (I_{27}) in der Ablenkwicklung (27) zu erzeugen, der S-korrigiert ist.

6. Ablenkvorrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die Impedanz einen dritten Kondensator (C_3) enthält, und daß die Klemm-Mittel (D_1 , D_2) mit dem dritten Kondensator (C_3) verbunden sind, um eine Spannung über dem dritten Kondensator (C_3) zu klem-



men und zu bewirken, daß dieser sich vor der Anfangszeit des Vorlauteils auf einem vorgegebenen Pegel befindet.

7. Ablenkvorrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die Klemm-Mittel eine Diode (D_1 , D_2) umfassen.

8. Ablenkvorrichtung für einen Fernsehempfänger, die auf ein synchronisierendes Eingangssignal ($2V'$) mit einer auf eine Ablenkfrequenz bezogenen Frequenz anspricht, mit:

einer Quelle des synchronisierenden Eingangssignals ($2V'$);

ersten (C_1) und zweiten (C_2) Kondensatoren, die eine Reihenanordnung bilden;

einer Quelle (R_2) eines ersten Stroms, die mit den Kondensatoren zu deren Ladung verbunden ist, um ein Sägezahnsignal (V_o') zu erzeugen, das einen ansteigenden Vorlauteil hat, der sich während des Vorlaufs in einer ersten Richtung ändert, und das einen ansteigenden Rücklauteil hat, der sich während des Rücklaufs in entgegengesetzter Richtung ändert; und

einer Quelle (500) einer ersten Spannung (V_3) mit einer auf die Frequenz des Eingangssignals ($2V'$) bezogenen Frequenz; gekennzeichnet durch:

eine erste Impedanz (C_3 , R_4 , R_5), die zwischen der Quelle (500) der Spannung (V_3) und einer Verbindungsklemme (703) des ersten (C_1) und des zweiten (C_2) Kondensators liegt, um einen zweiten Strom zu erzeugen, der der Verbindungsklemme (703) zugeführt wird und eine S-Korrektur des Sägezahnsignals (V_o') bewirkt;

mit dem ersten (C_1) und dem zweiten (C_2) Kondensator verbundene Schaltmittel (U_{6a}), um vor dem Beginn des Vorlauteils des Sägezahnsignals entsprechende Spannungen zu errichten, die an den beiden Kondensatoren mit entsprechenden Pegeln entwickelt werden, die von einer Amplitude des Sägezahnsignals weitgehend unbeeinträchtigt sind;

eine Ablenkwicklung (27); und

Mittel (100), die auf das Sägezahnsignal (V_o') ansprechen, um in der Ablenkwicklung (27) einen S-korrigierten Ablenkstrom (i_{27}) zu erzeugen.

9. Ablenkvorrichtung nach Anspruch 8, dadurch gekennzeichnet, daß die erste Impedanz einen dritten Kondensator (C_3) enthält, und daß eine zweite Impedanz (R_5) mit dem dritten Kondensator (C_3) verbunden ist, um einen Teil des Stroms, der in dem dritten Kondensator (C_3) fließt, im Nebenschluß zu führen und den zwei-

ten Strom so zu reduzieren, daß eine Änderungsrate des Sägezahnsignals (V_o') bei einer Endzeit des Vorlauteils kleiner wird.

Revendications

1. Dispositif de déviation de télévision sensible à un signal d'entrée de synchronisation ($2V'$) à une fréquence qui est reliée à une fréquence de déviation, comprenant :

un commutateur réglable (U_{6a}) sensible audit signal d'entrée qui fonctionne à une fréquence qui est reliée à celle dudit signal d'entrée ($2V'$) ;

des premier (C_1) et second (C_2) condensateurs formant un agencement en série qui est couplé audit commutateur (U_{6a}) ;

une source de courant (R_2) couplée auxdits condensateurs (C_1 , C_2) pour charger lesdits condensateurs afin de produire un signal en dent de scie (V_o') comportant une première partie à pente linéaire qui varie dans une première direction lorsque ledit commutateur (U_{6a}) n'est pas conducteur de sorte que, lorsque ledit commutateur devient conducteur, ledit commutateur (U_{6a}) décharge lesdits condensateurs (C_1 , C_2) pour former une seconde partie à pente linéaire dudit signal en dent de scie (V_o') qui varie dans une direction opposée ; et

une source (500) d'une tension à pente linéaire (V_3) reliée au signal en dent de scie produit ; caractérisé par :

une première impédance (R_4 , R_5) couplée à ladite source (500) de ladite tension à pente linéaire (V_3) et à une première borne de jonction (703) qui est couplée entre lesdits premier (C_1) et second (C_2) condensateurs pour générer un premier courant qui circule dans ladite première impédance (R_4 , R_5) laquelle contrôle la forme en S dudit signal en dent de scie (V_o') en réduisant le taux de variation dudit signal en dent de scie (V_o') au niveau de l'une des extrémités de début et de fin de l'une desdites première et seconde parties dudit signal en dent de scie en conformité avec ledit premier courant qui circule dans ladite première impédance (R_4 , R_5) ;

une seconde impédance (R_3) couplée à une borne (701) de ladite première impédance (R_4 , R_5), éloignée de ladite première borne de jonction (703), pour dériver une partie d'un courant qui circule suivant un trajet de courant entre ladite source (500) de ladite tension à pente linéaire (V_3) et ladite première borne de jonction (703) afin de réduire ledit premier courant dans ladite première impédance (R_4 , R_5) et qui réduit le taux de variation dudit signal en dent de scie (V_o') à l'autre extrémité des extré-



mités de début et de fin de ladite parties desdites première et seconde parties dudit signal en dent de scie (V_o') pour régler la forme en S au niveau de ladite autre extrémité des extrémités de début et de fin ;

un enroulement de déviation (27) ; et

un moyen (100) sensible audit signal en dent de scie (V_o') pour produire un courant de déviation dans ledit enroulement de déviation (27) qui est corrigé en S.

2. Dispositif selon la revendication 1, caractérisé par un troisième condensateur (C_3) destiné à un couplage capacitif de ladite tension à pente linéaire (V_3) à ladite première borne de jonction (703).

3. Dispositif selon la revendication 2, caractérisé en ce que ladite source de tension à pente linéaire (500) comprend un suiveur de tension (Q_2) comportant une borne d'entrée (500a) qui est sensible audit signal en dent de scie (V_o') et dans lequel ledit troisième condensateur (C_3) est couplé entre une borne de sortie (émetteur) dudit suiveur de tension (Q_2) et une borne (701) de ladite première impédance (R_4 , R_5) éloignée de ladite première borne de jonction (703).

4. Dispositif selon la revendication 2 caractérisé en ce que lesdites première (R_4 , R_5) et seconde (R_8) impédances comprennent les première et seconde résistances correspondantes dans lequel ledit troisième condensateur (C_3) et ladite première résistance (R_4 , R_5) forment un trajet de courant pour décharger ledit second condensateur (C_2) à ladite une desdites extrémités de début et de fin de ladite partie qui correspond à un intervalle de tracé dudit courant de déviation et pour charger ledit second condensateur à ladite autre extrémité desdites extrémités de départ et de fin de ladite partie qui correspond audit intervalle de tracé de telle sorte que, à ladite autre extrémité desdites extrémités de départ et de fin, ladite seconde impédance (R_8) réduit le taux suivant lequel ledit second condensateur (C_2) est chargé.

5. Dispositif de déviation de télévision sensible à un signal d'entrée de synchronisation (2V) à une fréquence qui est reliée à une fréquence de déviation, comprenant :

un commutateur réglable (U_{6a}) sensible audit signal d'entrée pour faire fonctionner ledit commutateur (U_{6a}) à une fréquence qui est reliée à celle dudit signal d'entrée (2V) ;

des premier (C_1) et second (C_2) condensateurs formant un arrangement en série qui est

couplé à une borne (500a) dudit commutateur (U_{6a}) ;

une source (V_5) de tension continue (CC) couplée à travers une première résistance (R_2) auxdits condensateurs (C_1 , C_2) pour produire un signal en dent de scie (V_o') au niveau de ladite borne (500a) possédant une partie de tracé à pente linéaire qui varie dans une première direction lorsque ledit commutateur (U_{6a}) est non conducteur et une partie de retour à pente linéaire qui varie dans une direction opposée lorsque ledit commutateur (U_{6a}) est conducteur ; caractérisé par

une impédance (C_3 , R_4 , R_5) comportant une première borne qui est couplée à une borne de jonction (703) desdits premier (C_1) et second (C_2) condensateurs pour produire un premier courant qui est couplé à ladite borne de jonction (703) pour contrôler la forme en S dudit signal en dent de scie ;

un moyen (D_1 , D_2) couplé auxdits premier (C_1) et second (C_2) condensateurs pour bloquer chaque tension correspondante à travers chacun desdits premier (C_1) et second (C_2) condensateurs, entraînant chacun à se situer à un niveau prédéterminé correspondant, avant un instant de démarrage de ladite partie de tracé de telle sorte que chacun desdits niveaux prédéterminés correspondants à travers chacun desdits condensateurs est sensiblement in affecté par une amplitude dudit signal en dent de scie à une fin de ladite portion de tracé ;

un enroulement de déviation (27) ; et

un moyen (100) sensible audit signal en dent de scie (V_o') qui est corrigé en S pour produire un courant de déviation (i_{27}) dans ledit enroulement de déviation (27) qui est corrigé en S.

6. Dispositif selon la revendication 5 caractérisé en ce que ladite impédance inclut un troisième condensateur (C_3) et dans lequel ledit moyen de blocage (D_1 , D_2) est couplé audit troisième condensateur pour bloquer une tension à travers ledit troisième condensateur (C_3) l'amenant à se situer au niveau prédéterminé correspondant avant ledit instant de démarrage de ladite partie de tracé.

7. Dispositif selon la revendication 5, caractérisé en ce que le moyen de blocage comprend une diode (D_1 , D_2).

8. Dispositif de déviation de télévision sensible à un signal d'entrée de synchronisation (2V) à une fréquence qui est reliée à une fréquence de déviation, comprenant :



une source dudit signal d'entrée de synchronisation ($2V'$) ;

des premier (C_1) et second (C_2) condensateurs formant un agencement en série ;

une source (R_2) d'un premier courant couplée auxdits condensateurs afin de charger lesdits condensateurs pour produire un signal en dent de scie (V_o') comportant une partie de tracé à pente linéaire qui varie dans une première direction pendant le tracé et une partie de retour à pente linéaire dudit signal en dent de scie (V_o') qui varie dans une direction opposée pendant le retour ; et

une source (500) d'une première tension (V_3) à une fréquence qui est reliée à celle dudit signal d'entrée ($2V'$) ; caractérisé par

une première impédance (C_3, R_4, R_5) couplée entre ladite source (500) de ladite tension (V_3) et une borne de jonction (703) desdits premier (C_1) et second (C_2) condensateurs pour produire un second courant qui est couplé à ladite borne de jonction (703) qui fournit une correction de S audit signal en dent de scie (V_o') ;

un moyen de commutation (U_{8a}) couplé auxdits premier (C_1) et second (C_2) condensateurs pour établir, ayant un début de ladite partie de tracé dudit signal en dent de scie, des tensions respectives qui sont développées à travers les deux condensateurs à des niveaux correspondants qui sont sensiblement in affectés par une amplitude dudit signal en dent de scie ;

un enroulement de déviation (27) ; et

un moyen (100) sensible audit signal en dent de scie (V_o') qui est corrigé en S pour générer un courant de déviation (i_{27}) dans ledit enroulement de déviation (27) qui est corrigé en S.

9. Dispositif selon la revendication 8 caractérisé en ce que ladite première impédance inclut un troisième condensateur (C_3) et qu'une seconde impédance (R_3) est couplée audit troisième condensateur (C_3) pour dériver une partie d'un courant qui circule dans ledit troisième condensateur (C_3) pour réduire ledit second courant de telle sorte qu'en réduisant ledit second courant, le taux de variation dudit signal en dent de scie (V_o') à un instant de fin de ladite partie de tracé devienne plus petite.

