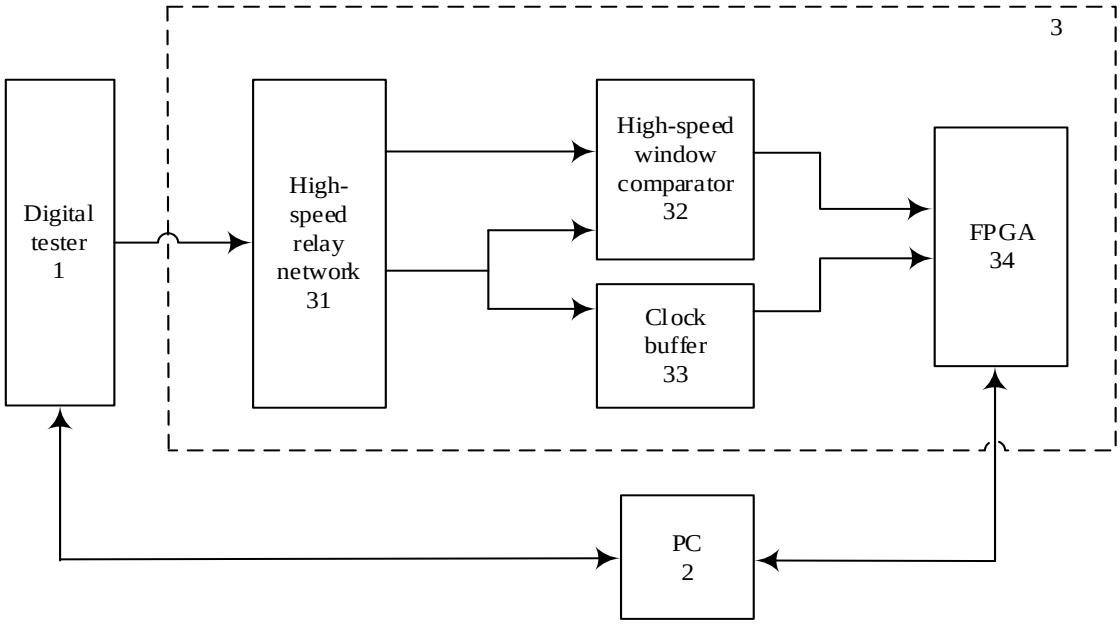

3
Digital tester 1
High-speed relay network 31
High-speed window comparator 32
Clock buffer 33
FPGA 34
PC 2

FIG. 1

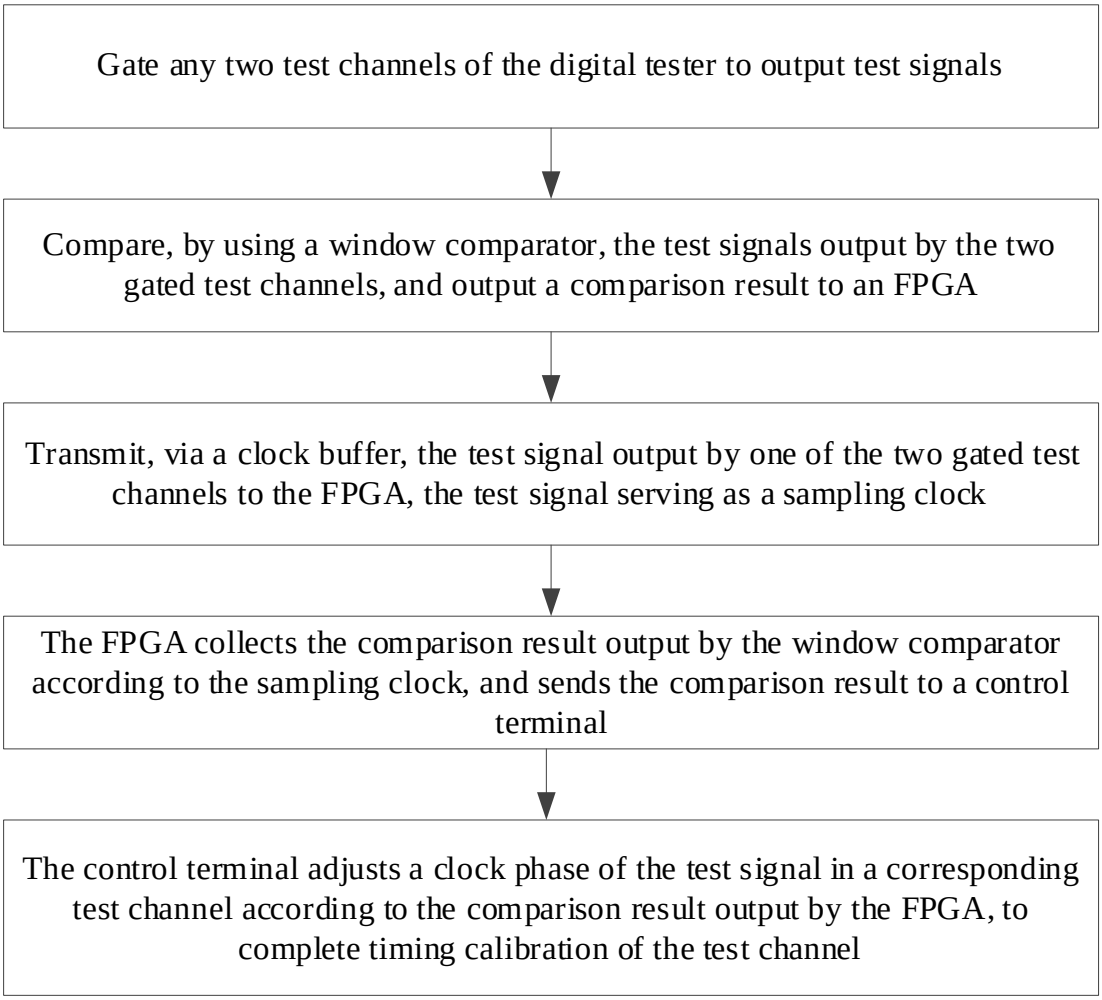

Gate any two test channels of the digital tester to output test signals
Compare, by using a window comparator, the test signals output by the two gated test channels, and output a comparison result to an FPGA
Transmit, via a clock buffer, the test signal output by one of the two gated test channels to the FPGA, the test signal serving as a sampling clock
The FPGA collects the comparison result output by the window comparator according to the sampling clock, and sends the comparison result to a control terminal
The control terminal adjusts a clock phase of the test signal in a corresponding test channel according to the comparison result output by the FPGA, to complete timing calibration of the test channel

FIG. 2