Abstract

A semiconductor device comprising a first active pattern including a first lower pattern, and a plurality of first sheet patterns, a plurality of first gate structures on the first lower pattern, a second active pattern including a second lower pattern and a plurality of second sheet patterns, a plurality of second gate structures on the second lower pattern, a first source/drain recess between adjacent first gate structures, a second source/drain recess between adjacent second gate structures, first and second source/drain patterns in the first and second source/drain recesses, respectively, wherein a depth from an upper surface of the first lower pattern to a lowermost part of the first source/drain pattern is smaller than a depth from an upper surface of the second lower pattern to a lowermost part of the second source/drain pattern, and the first and second source/drain patterns include impurities of same conductive type.

FIG. 3