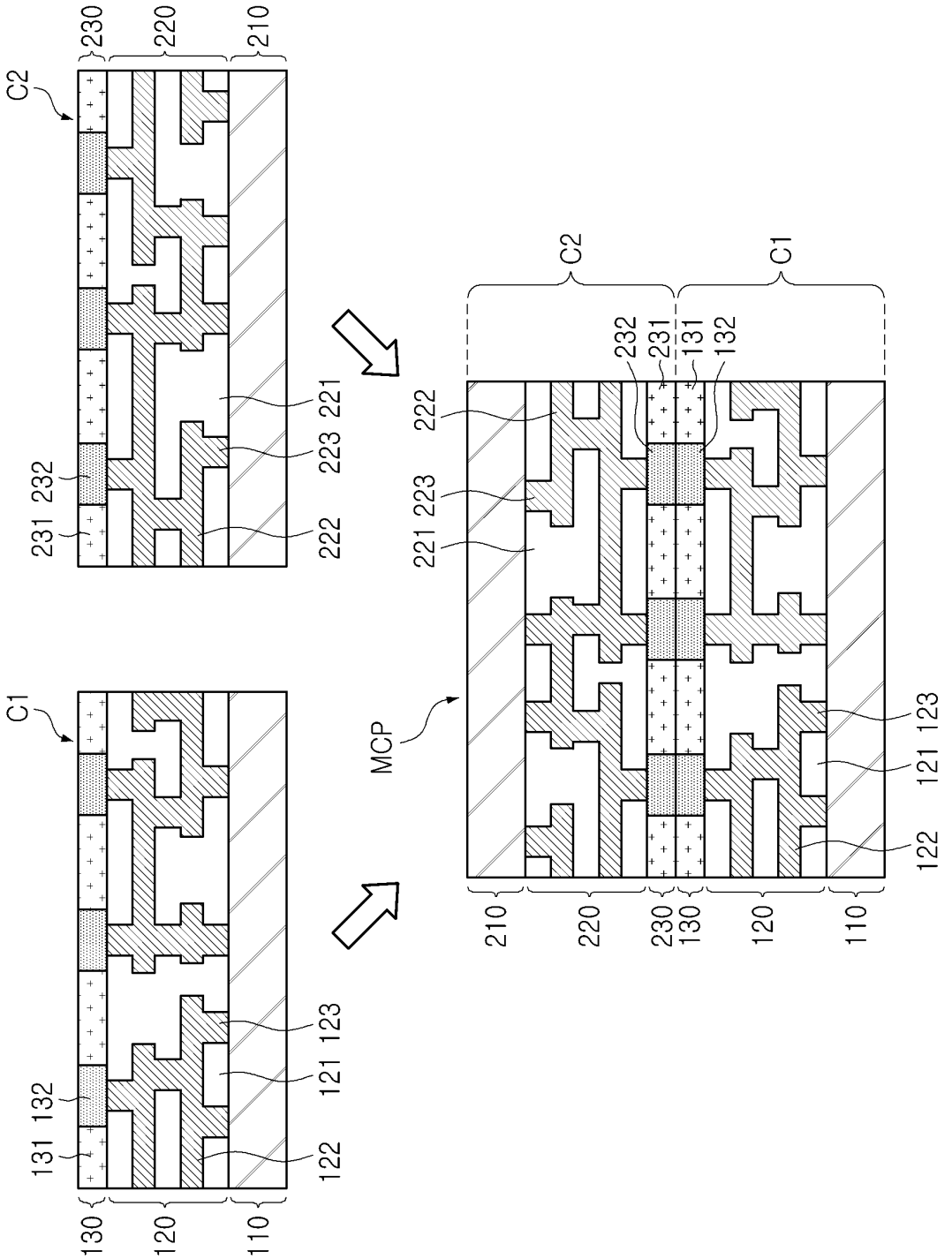

C2
230
220
210
231 232
222
223 221
C1
131 132
122
121 123
130
120
110
MCP
C2
C1
232
231
131
132
222
221 223
122
121 123
210
220
230
130
120
110

FIG. 1

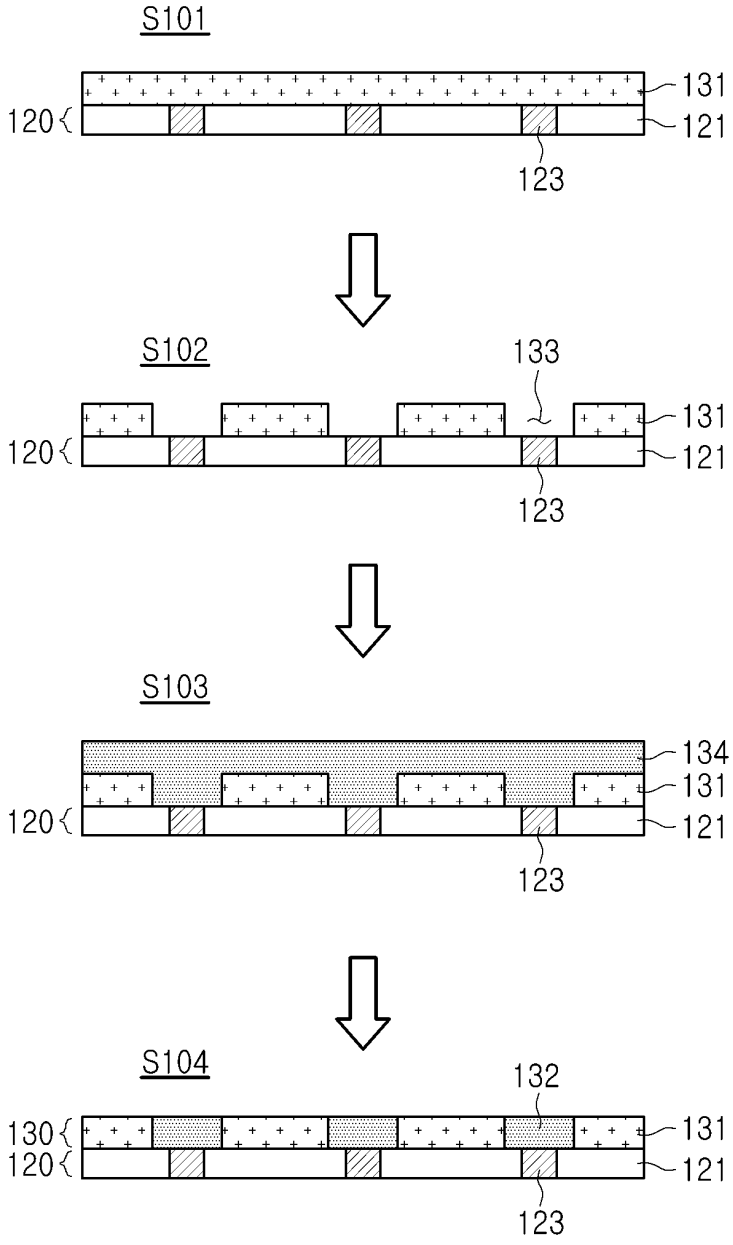

S101
131
120
121
123
S102
133
131
120
121
123
S103
134
131
120
121
123
S104
132
130
131
120
121
123

FIG. 2

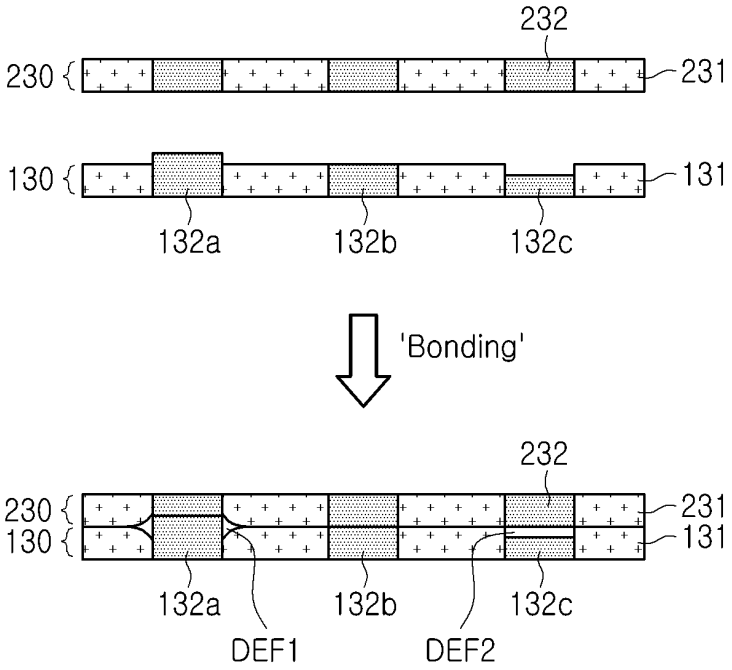

232
230
231
130
131
132a
132b
132c
'Bonding'
232
230
231
130
131
132a
DEF1
132b
DEF2
132c

FIG. 3

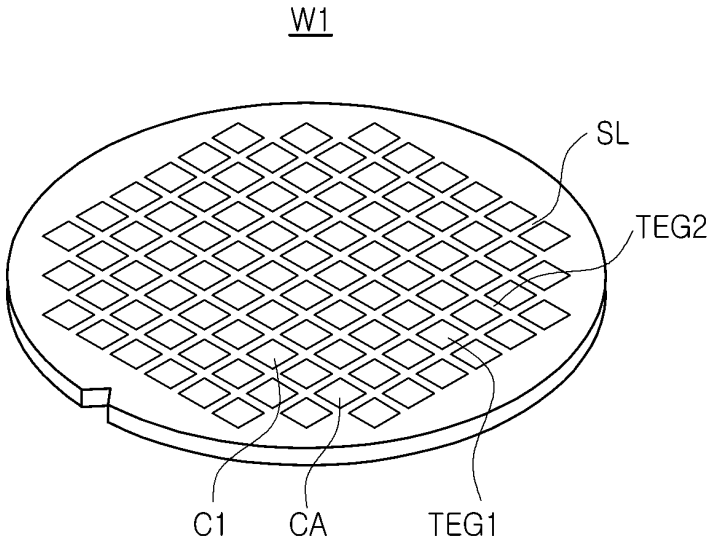

W1
SL
TEG2
C1
CA
TEG1

FIG. 4

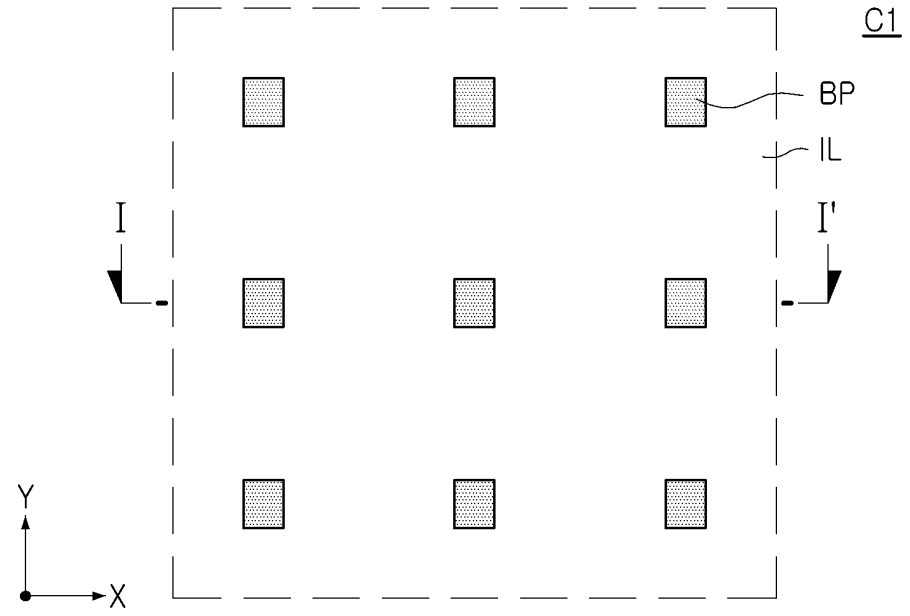


FIG. 5A

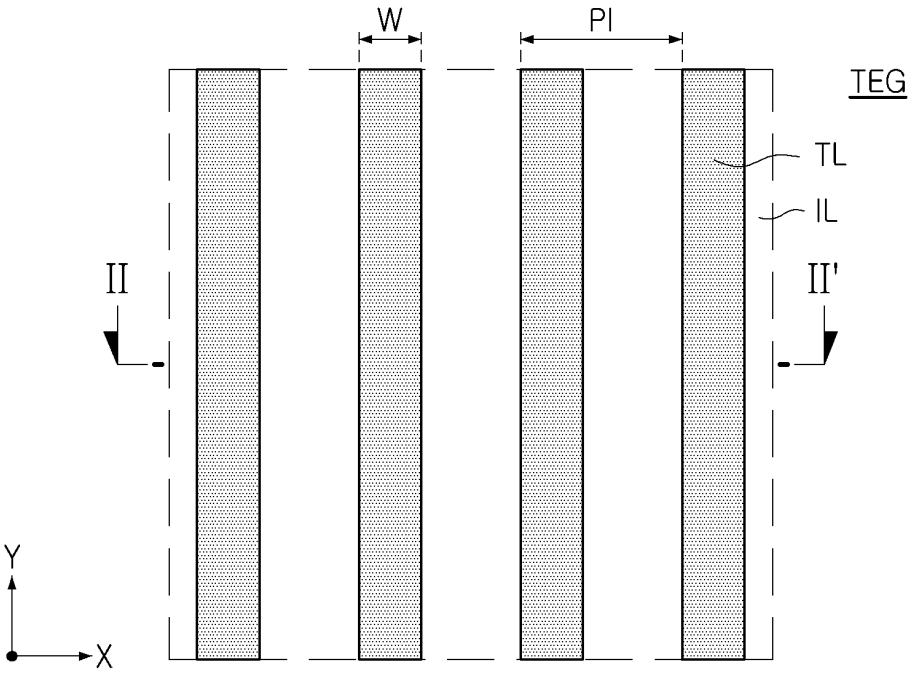
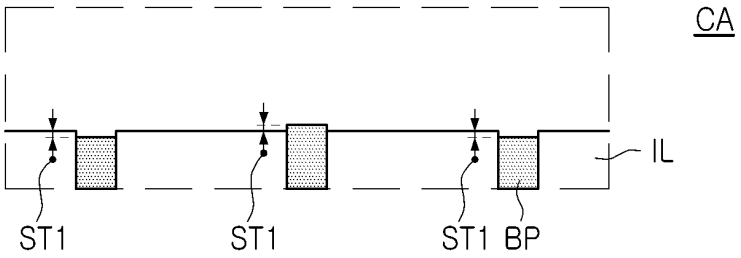
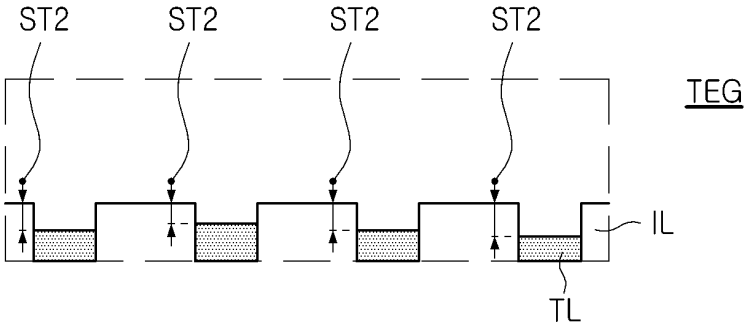


FIG. 5B



I-I'

FIG. 5C



II-II'

FIG. 5D

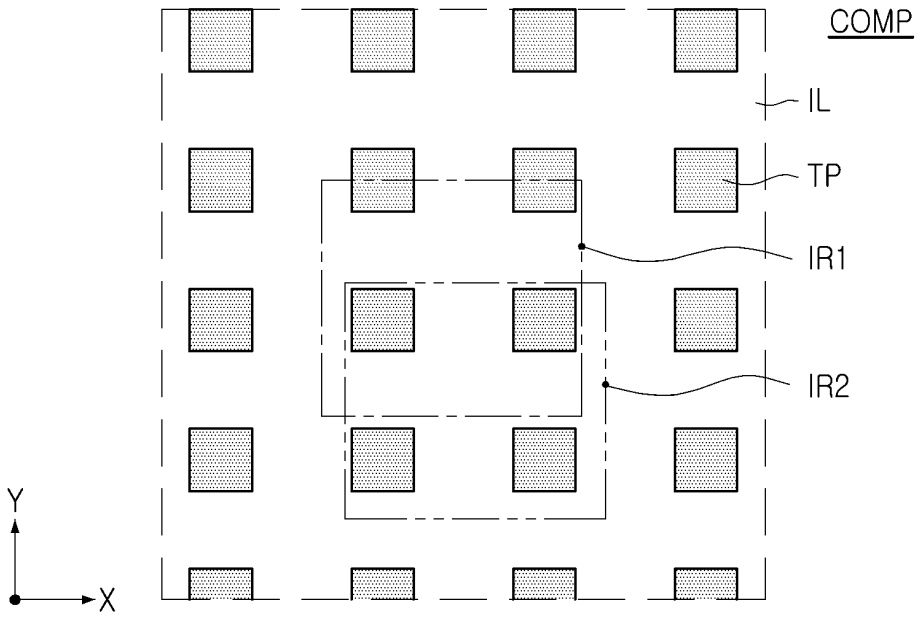


FIG. 6A

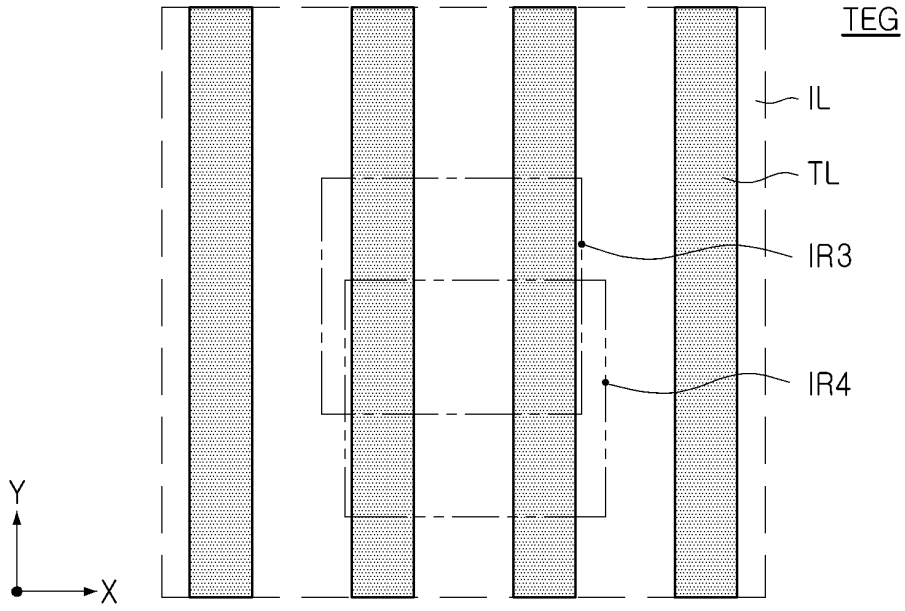


FIG. 6B

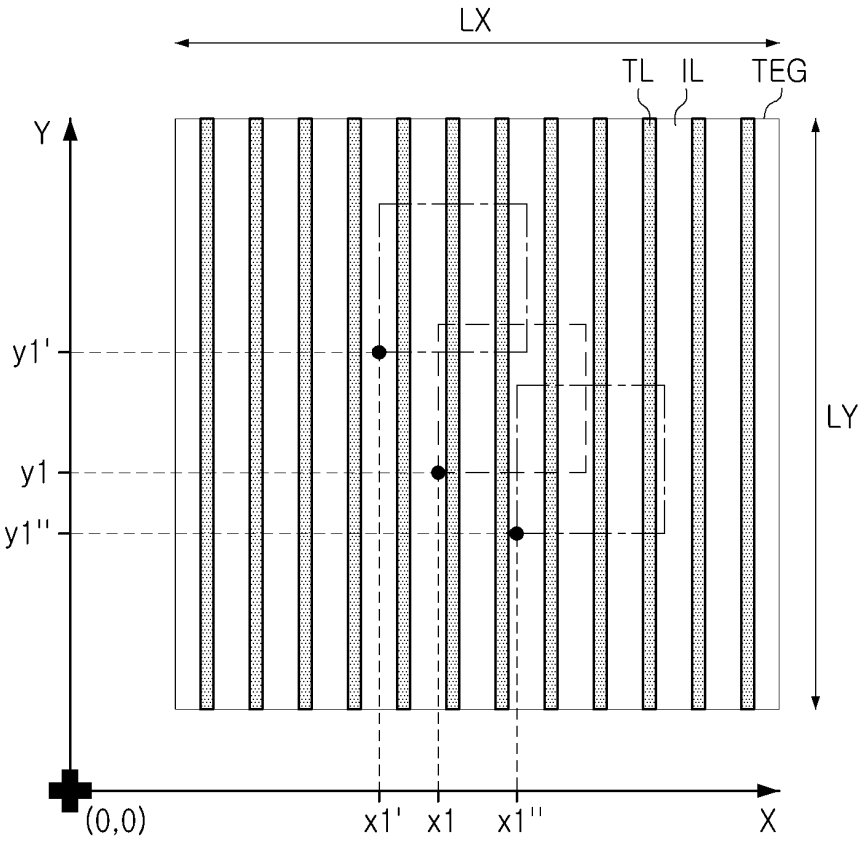


FIG. 7

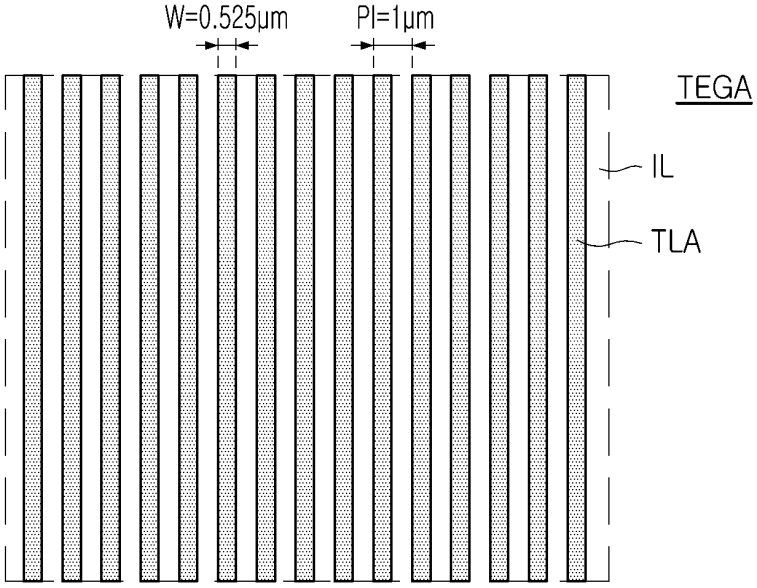


FIG. 8A

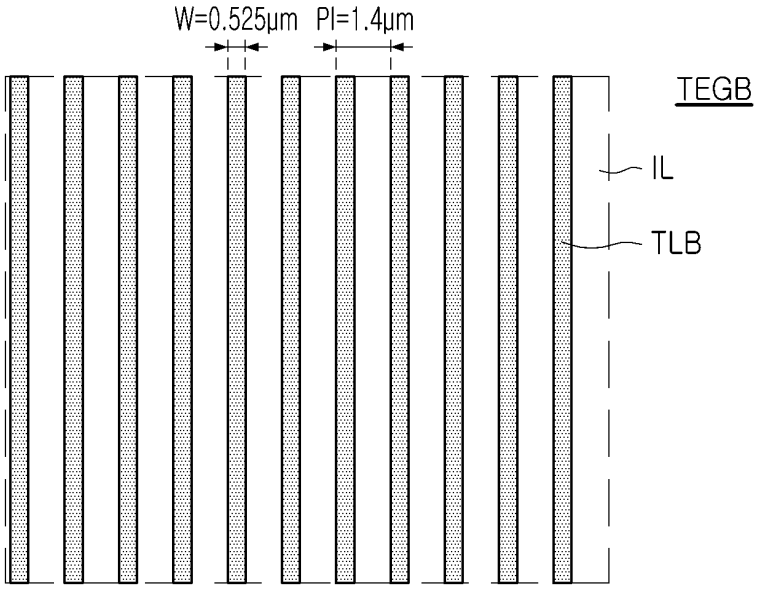


FIG. 8B

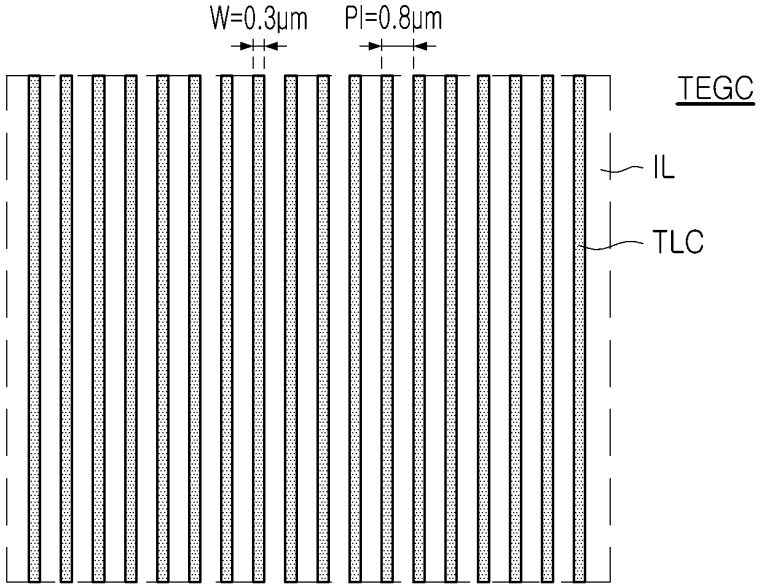


FIG. 8C

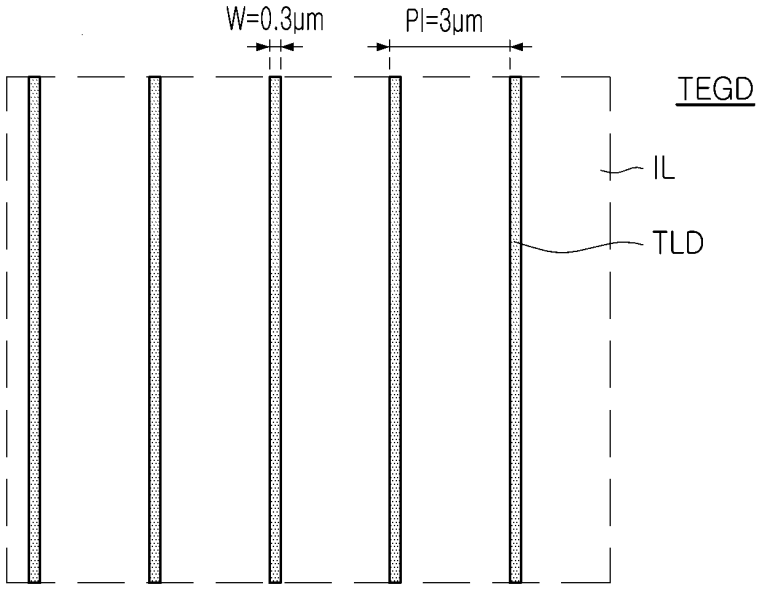


FIG. 8D

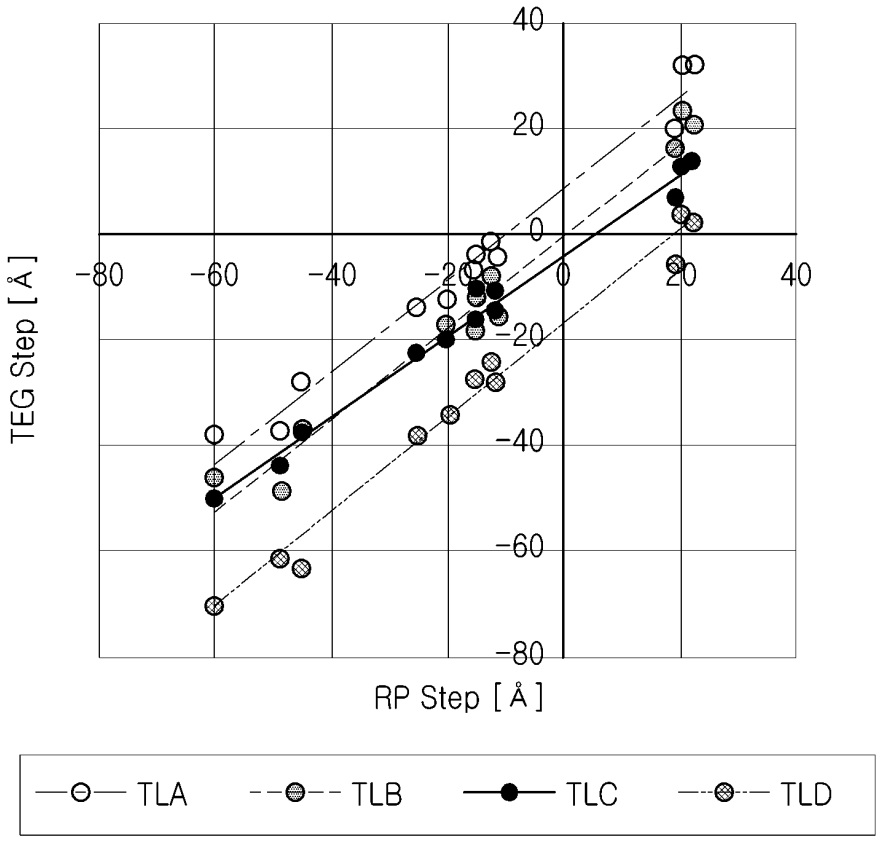

40
20
0
-20
-40
-60
-80
-80
-60
-40
-20
0
20
40
TEG Step [Å]
RP Step [Å]
TLA
TLB
TLC
TLD

FIG. 8E

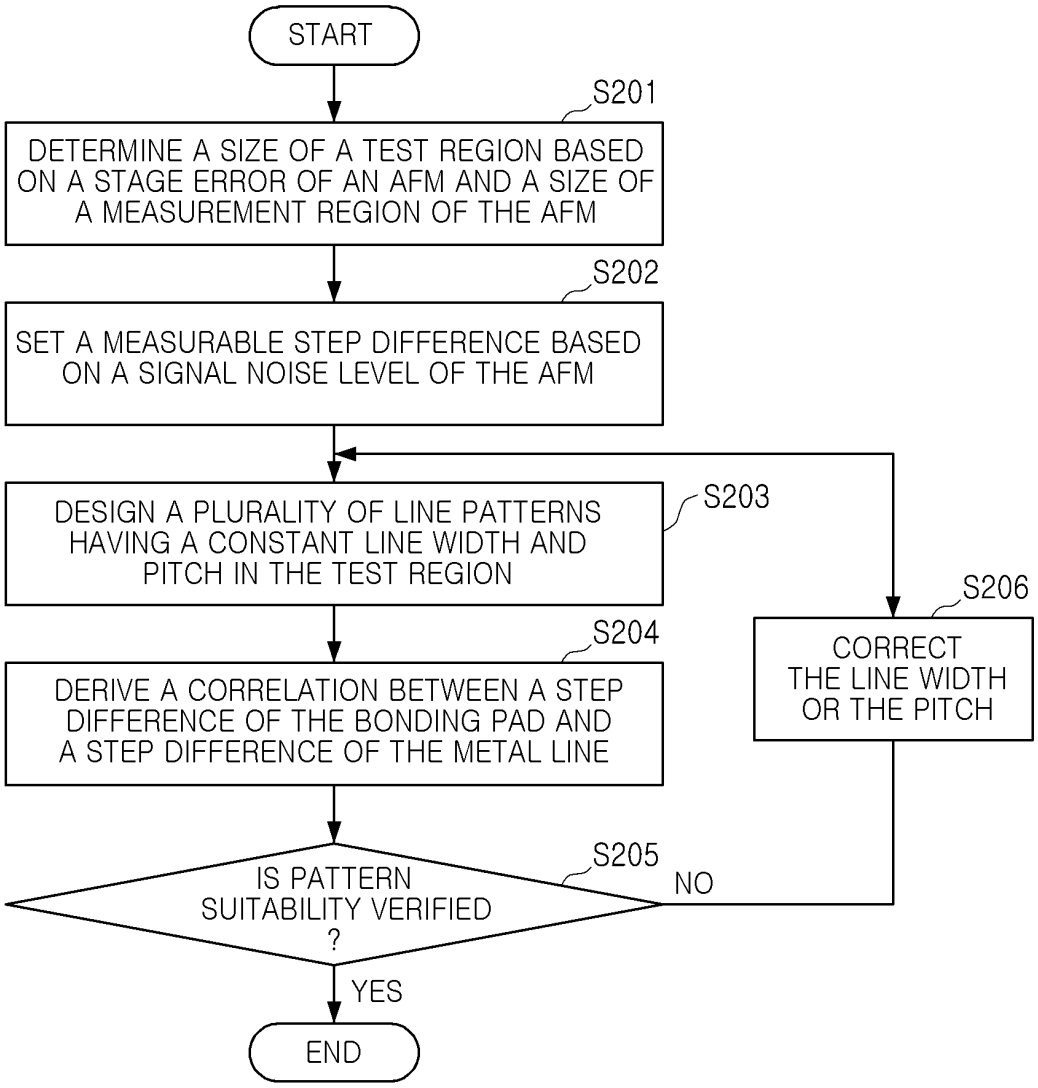

START
S201
DETERMINE A SIZE OF A TEST REGION BASED ON A STAGE ERROR OF AN AFM AND A SIZE OF A MEASUREMENT REGION OF THE AFM
S202
SET A MEASURABLE STEP DIFFERENCE BASED ON A SIGNAL NOISE LEVEL OF THE AFM
S203
DESIGN A PLURALITY OF LINE PATTERNS HAVING A CONSTANT LINE WIDTH AND PITCH IN THE TEST REGION
S204
DERIVE A CORRELATION BETWEEN A STEP DIFFERENCE OF THE BONDING PAD AND A STEP DIFFERENCE OF THE METAL LINE
S205
IS PATTERN SUITABILITY VERIFIED ?
NO
S206
CORRECT THE LINE WIDTH OR THE PITCH
YES
END

FIG. 9

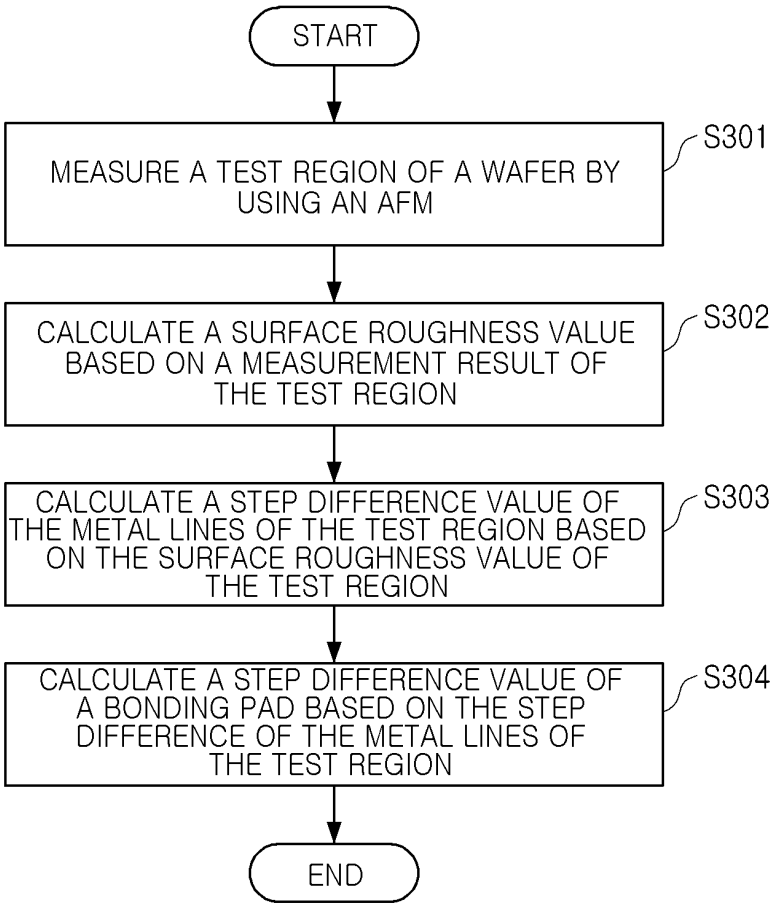

START
MEASURE A TEST REGION OF A WAFER BY USING AN AFM
S301
CALCULATE A SURFACE ROUGHNESS VALUE BASED ON A MEASUREMENT RESULT OF THE TEST REGION
S302
CALCULATE A STEP DIFFERENCE VALUE OF THE METAL LINES OF THE TEST REGION BASED ON THE SURFACE ROUGHNESS VALUE OF THE TEST REGION
S303
CALCULATE A STEP DIFFERENCE VALUE OF A BONDING PAD BASED ON THE STEP DIFFERENCE OF THE METAL LINES OF THE TEST REGION
S304
END

FIG. 10

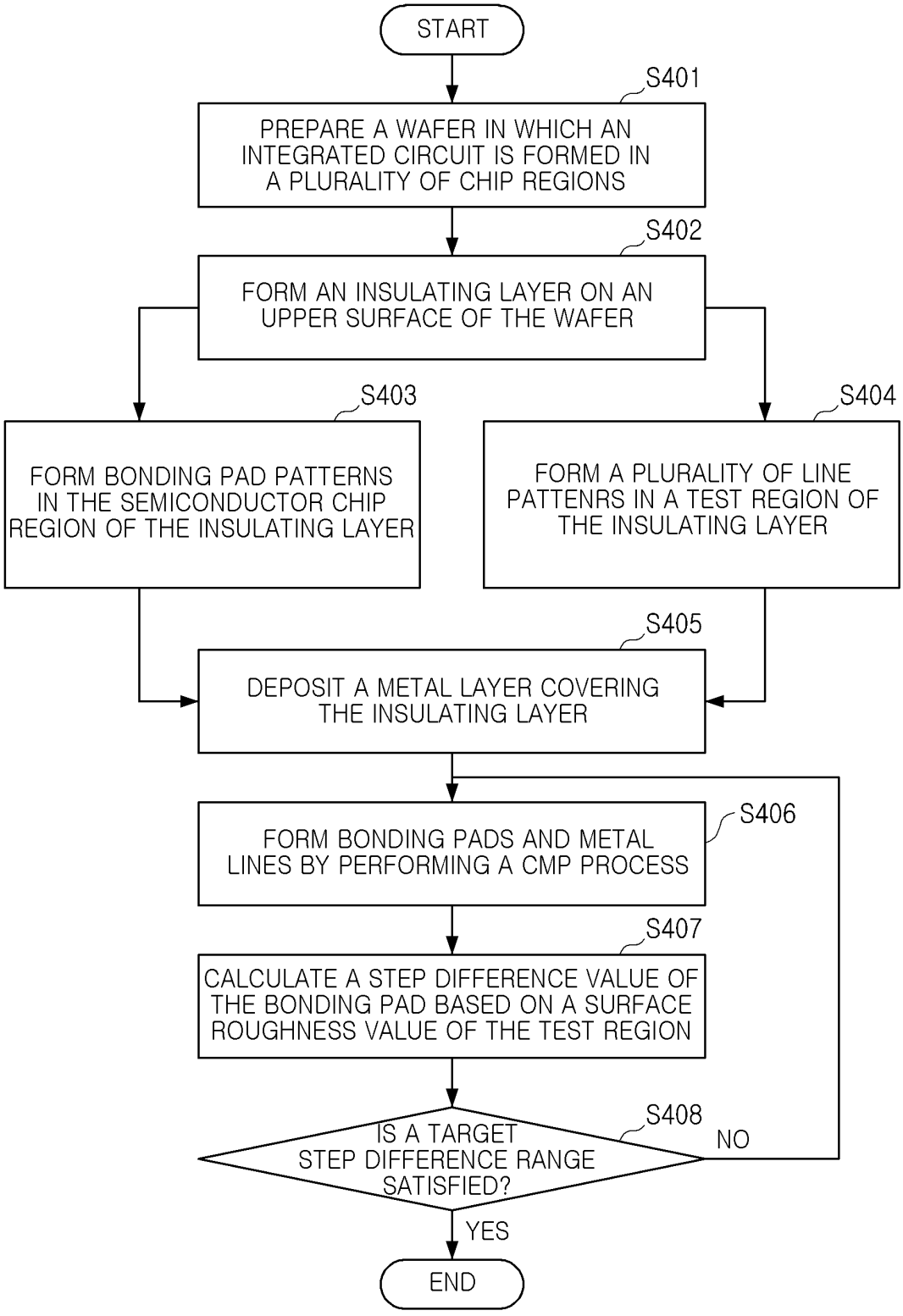

START
S401
PREPARE A WAFER IN WHICH AN INTEGRATED CIRCUIT IS FORMED IN A PLURALITY OF CHIP REGIONS
S402
FORM AN INSULATING LAYER ON AN UPPER SURFACE OF THE WAFER
S403
FORM BONDING PAD PATTERNS IN THE SEMICONDUCTOR CHIP REGION OF THE INSULATING LAYER
S404
FORM A PLURALITY OF LINE PATTENRS IN A TEST REGION OF THE INSULATING LAYER
S405
DEPOSIT A METAL LAYER COVERING THE INSULATING LAYER
S406
FORM BONDING PADS AND METAL LINES BY PERFORMING A CMP PROCESS
S407
CALCULATE A STEP DIFFERENCE VALUE OF THE BONDING PAD BASED ON A SURFACE ROUGHNESS VALUE OF THE TEST REGION
S408
IS A TARGET STEP DIFFERENCE RANGE SATISFIED?
NO
YES
END

FIG. 11

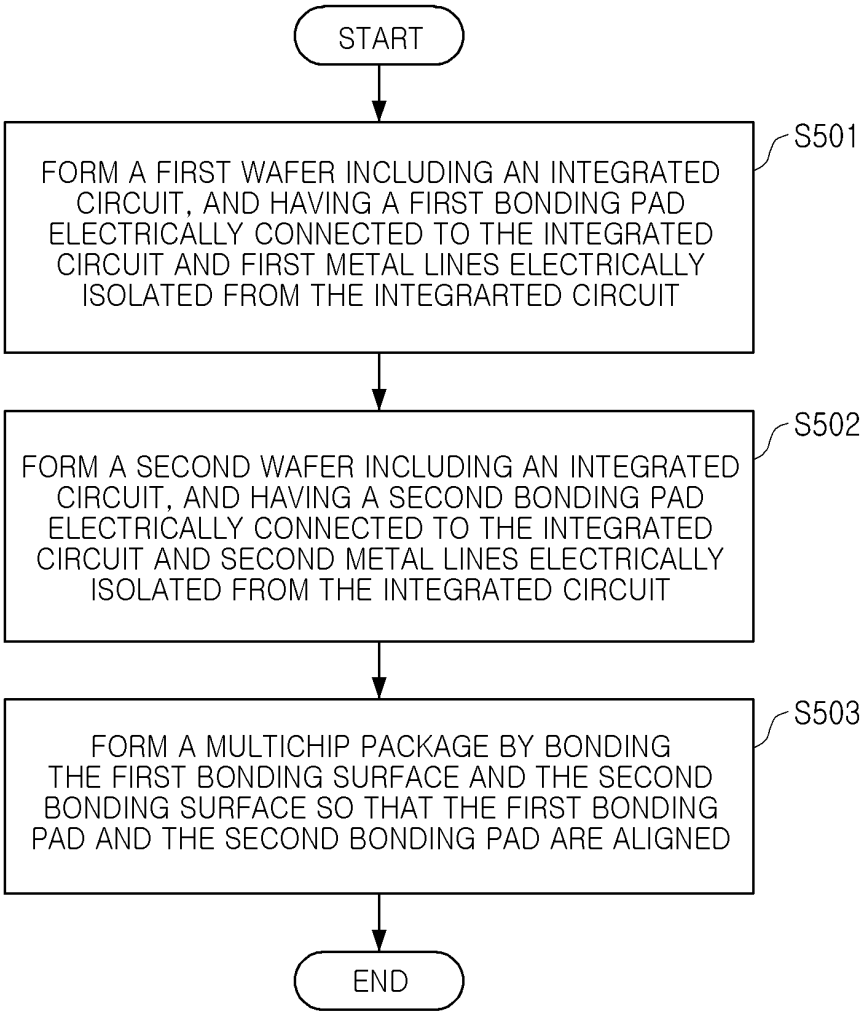

START
FORM A FIRST WAFER INCLUDING AN INTEGRATED CIRCUIT, AND HAVING A FIRST BONDING PAD ELECTRICALLY CONNECTED TO THE INTEGRATED CIRCUIT AND FIRST METAL LINES ELECTRICALLY ISOLATED FROM THE INTEGRARTED CIRCUIT
S501
FORM A SECOND WAFER INCLUDING AN INTEGRATED CIRCUIT, AND HAVING A SECOND BONDING PAD ELECTRICALLY CONNECTED TO THE INTEGRATED CIRCUIT AND SECOND METAL LINES ELECTRICALLY ISOLATED FROM THE INTEGRATED CIRCUIT
S502
FORM A MULTICHIP PACKAGE BY BONDING THE FIRST BONDING SURFACE AND THE SECOND BONDING SURFACE SO THAT THE FIRST BONDING PAD AND THE SECOND BONDING PAD ARE ALIGNED
S503
END

FIG. 12

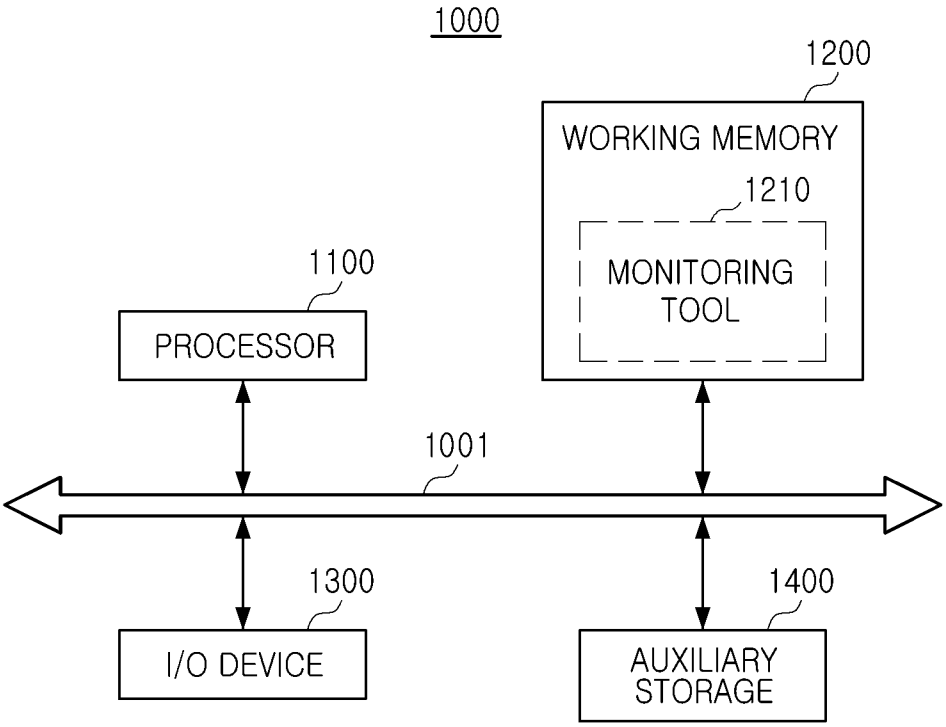

1000
1200
WORKING MEMORY
1210
MONITORING TOOL
1100
PROCESSOR
1001
1300
I/O DEVICE
1400
AUXILIARY STORAGE

FIG. 13