

MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE

TECHNICAL FIELD

5 [0001] The present disclosure belongs to, but is not limited to, the technical field of semiconductor manufacturing, and specifically relates to a method for manufacturing a semiconductor device.

BACKGROUND

10 [0002] With the continuous development of semiconductor manufacturing processes, critical dimensions of semiconductor devices are continuously reduced. However, a reduced gate width may cause the so-called short-channel effects, which may cause drain induced barrier lowering (DIBL), making it impossible to turn off the semiconductor device.

15 [0003] In view of this challenge, fin field-effect transistors (Fin FETs) and gate-all-around field-effect transistors (GAA FETs) have been proposed. In 3nm and finer processes, GAA FETs exhibit greater advantages over Fin FETs, such as better control of leakage current, smaller DIBL, higher performance, greater device density, and the like.

[0004] A conventional GAA FET is shown in FIG. 1, which includes a substrate 11, several channel regions 12 formed on the substrate 11, a gate insulation layer (not shown) arranged around the channel regions 12, and a metal gate 13 arranged around the gate insulation layer. Each channel region 12 is surrounded on all sides by the metal gate 13, thereby obtaining smaller DIBL. However, there is still a need for further improvements to GAA FETs.

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SUMMARY

[0005] Embodiments of the present disclosure provide a method for manufacturing a semiconductor device which can at least solve the problem of poor high-frequency switching characteristics of the semiconductor device in the related art.

30 [0006] To at least solve the above technical problem, an embodiment of the present

disclosure provides a method for manufacturing a semiconductor device, including:

forming a sacrificial region on a surface of a substrate;

forming a stacked structure on the sacrificial region, the stacked structure including a first semiconductor layer and a second semiconductor layer alternately stacked;

5 removing the sacrificial region to form a cavity between the substrate and the stacked structure;

filling the cavity with an insulation layer;

removing one of the first semiconductor layer and the second semiconductor layer;

and

10 forming a gate structure around the other of the first semiconductor layer and the second semiconductor layer.

[0007] In some implementations, forming the sacrificial region on the surface of the substrate includes:

performing ion implantation in a preset region on the surface of the substrate; and

15 performing an annealing process on the region in which the ion implantation is performed, so as to form the sacrificial region.

[0008] In some implementations, the ion implantation is performed for n-type doping with a dose of $1 \times 10^{15}/\text{cm}^2$ to $5 \times 10^{16}/\text{cm}^2$.

[0009] In some implementations, a dopant for the n-type doping includes at least one of
20 Sb, As and P.

[0010] In some implementations, forming the stacked structure on the sacrificial region includes:

forming the first semiconductor layer and the second semiconductor layer alternately stacked on the surface of the substrate; and

25 etching the first semiconductor layer and the second semiconductor layer alternately stacked to obtain the stacked structure and expose at least a part of a sidewall of the sacrificial region.

[0011] In some implementations, etching the first semiconductor layer and the second semiconductor layer alternately stacked includes:

30 forming a hard mask layer above the first semiconductor layer and the second semiconductor layer alternately stacked, wherein a projection of the hard mask layer on the substrate corresponds to the sacrificial region; and

etching the first semiconductor layer, the second semiconductor layer and the substrate by using the hard mask layer to form the stacked structure and form grooves in

the substrate on both sides of the stacked structure.

[0012] In some implementations, the at least a part of the sidewall of the sacrificial region is exposed during formation of the grooves in the substrate on both sides of the stacked structure.

5 [0013] In some implementations, forming the stacked structure on the sacrificial region further includes:

forming a protective layer covering the stacked structure and the substrate; and

performing anisotropic etching on the protective layer and the substrate, so that the protective layer on the sidewall of the stacked structure is retained as a sidewall
10 protective layer, and the at least a part of a sidewall of the sacrificial region is exposed.

[0014] In some implementations, forming the protective layer covering the stacked structure and the substrate includes:

forming the protective layer by atomic layer deposition (ALD) process; or

forming the protective layer including a silicon nitride based material; or

15 forming the protective layer including at least one of silicon nitride, SiON, SiOCN or SiCN.

[0015] In some implementations, performing anisotropic etching on the protective layer includes:

performing the anisotropic etching using a process gas with a high etching rate, a
20 high upper electrode radio frequency power and a high lower electrode radio frequency power.

[0016] In some implementations, the process gas includes chlorine or a fluorocarbon-based gas; or

the upper electrode radio frequency power ranges from 100W to 3000W, and the
25 lower electrode radio frequency power ranges from 50W to 1000W.

[0017] In some implementations, the hard mask layer includes at least one of an oxide insulation layer and a nitride insulation layer; or

the hard mask layer includes a first hard mask layer and a second hard mask layer
above the first hard mask layer, wherein the first hard mask layer includes silicon oxide,
30 and the second hard mask layer includes silicon nitride.

[0018] In some implementations, removing the sacrificial region includes:

performing isotropic plasma etching on the sacrificial region.

[0019] In some implementations, performing isotropic plasma etching on the sacrificial region includes:

etching the sacrificial region in a low-pressure environment without loading a lower electrode radio frequency power.

[0020] In some implementations, the low-pressure environment is from 5 mTorr to 800 mTorr.

5 [0021] In some implementations, an etching gas used for the isotropic plasma etching is an etching gas that makes an etching selectivity between the sacrificial region and the substrate greater than a preset value.

[0022] In some implementations, the substrate includes silicon, the sacrificial region includes heavily doped n-type silicon, and the etching gas used for the isotropic plasma
10 etching is chlorine; and

the etching selectivity between the sacrificial region and the substrate is greater than 200.

[0023] In some implementations, the first semiconductor layer and the second semiconductor layer are made of semiconductor materials with different lattice constants.

15 [0024] In some implementations, each of the first semiconductor layer and the second semiconductor layer includes at least one of Si, Ge, SiGe, GeSn, SiGeSn, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb and InP.

[0025] In some implementations, filling the cavity with the insulation layer includes:

20 depositing the insulation layer around the stacked structure and on the surface of the substrate until the insulation layer below the stacked structure at the cavity is attached to the insulation layer above the substrate at the cavity; and

removing the insulation layer outside the cavity.

[0026] In some implementations, depositing the insulation layer around the stacked structure and on the surface of the substrate includes:

25 depositing the insulation layer by ALD process.

[0027] In some implementations, the method for manufacturing a semiconductor device further includes:

perform an annealing process on the insulation layer.

[0028] In some implementations, the method for manufacturing a semiconductor device
30 further includes:

removing the sidewall protective layer and the hard mask layer; and

filling the grooves to form shallow trench isolation structures.

[0029] In some implementations, before removing one of the first semiconductor layer and the second semiconductor layer, the method further includes:

respectively forming a source region and a drain region on two sides of a region of the stacked structure in which the gate structure is to be formed.

[0030] In some implementations, the gate structure includes a gate dielectric layer arranged around the other of the first semiconductor layer and the second semiconductor layer, and a gate electrode layer arranged around the gate dielectric layer; and

the other of the first semiconductor layer and the second semiconductor layer surrounded by the gate structure is formed as a channel region of the semiconductor device.

[0031] In the method for manufacturing a semiconductor device according to the embodiments of the present disclosure, an insulation layer is formed between the lowermost gate structure in the semiconductor device and the substrate, so that the parasitic gate capacitance between the lowermost gate structure and the substrate is suppressed, and the high-frequency switching characteristics of the semiconductor device are improved.

BRIEF DESCRIPTION OF DRAWINGS

[0032] FIG. 1 shows a schematic diagram of a GAA FET in the related art;

[0033] FIG. 2 shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0034] FIG. 3 shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0035] FIG. 4 shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0036] FIG. 5 shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0037] FIG. 6 shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0038] FIG. 7A shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present

disclosure;

[0039] FIG. 7B shows a schematic cross-sectional view taken along the dashed line in FIG. 7A;

5 [0040] FIG. 8A shows a schematic isometric view of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0041] FIG. 8B shows a schematic front view of FIG. 8A;

[0042] FIG. 8C shows a schematic cross-sectional view taken along the dashed line in FIG. 8B;

10 [0043] FIG. 9A shows a schematic isometric view of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0044] FIG. 9B shows a schematic front view of FIG. 9A;

15 [0045] FIG. 9C shows a schematic cross-sectional view taken along the dashed line in FIG. 9B;

[0046] FIG. 10A shows a schematic isometric view of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0047] FIG. 10B shows a schematic front view of FIG. 10A;

20 [0048] FIG. 10C shows a schematic cross-sectional view taken along the dashed line in FIG. 10B;

[0049] FIG. 11 shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

25 [0050] FIG. 12 shows a schematic isometric view of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

[0051] FIG. 13A shows a schematic diagram of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the present disclosure;

30 [0052] FIG. 13B shows a schematic cross-sectional view taken along the dashed line in FIG. 13A;

[0053] FIG. 14A shows a schematic isometric cross-sectional view of one of the stages of a method for manufacturing a semiconductor device according to an embodiment of the

present disclosure; and

[0054] FIG. 14B shows a schematic front view of FIG. 14A.

DETAIL DESCRIPTION OF EMBODIMENTS

5 [0055] To clarify the objects, technical solutions and advantages of the present disclosure, the technical solutions in the embodiments of the present disclosure will be clearly and completely described below with reference to the accompanying drawings in the embodiments of the present disclosure. Obviously, the described embodiments are some, not all, of the embodiments of the present disclosure. All other embodiments obtained by
10 the ordinarily skilled in the art based on the embodiments of the present disclosure without paying any creative effort shall be included in the protection scope of the present disclosure.

[0056] It should be understood by those skilled in the art that the embodiments of the present disclosure are merely illustration of the structures and methods of the present
15 disclosure that may be embodied in various forms. Furthermore, each example given in connection with the various embodiments is intended to be illustrative, and not restrictive. Furthermore, the figures are not necessarily drawn to scale, where some features may be exaggerated to show details of particular components. Therefore, specific structural and functional details in the embodiments of the present disclosure are not to be interpreted
20 as being restrictive, but merely as a representative basis for teaching one skilled in the art to variously employ the embodiments of the present disclosure. It should also be noted that like and corresponding elements are indicated by like reference numerals.

[0057] In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques,
25 to provide an understanding of various embodiments of the present disclosure. However, it should be understood by those skilled in the art that various embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail to avoid obscuring the present disclosure.

30 [0058] For purposes of the description hereinafter, the terms "upper", "right", "left", "vertical", "horizontal", "top", "bottom", and derivatives thereof shall relate to the orientations of the structures and methods disclosed in the accompanying drawings. It will be understood that when an element as a layer, region or substrate is referred to as being

"on" another element, it may be directly on the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly on" another element, there is no intervening element between the two. It will also be understood that when an element is referred to as being "under" another element, it may be directly under the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly under" another element, there is no intervening element between the two.

[0059] A GAA FET in the related art is shown in FIG. 1, which includes a substrate 11, several channel regions 12 formed on the substrate 11, a gate insulation layer (not shown) arranged around the channel regions 12, and a metal gate 13 arranged around the gate insulation layer. It has been found that in the GAA FET structure, a parasitic gate capacitance will be formed between the lowermost metal gate 13 and the substrate 11, and when an on or off voltage is applied to the metal gate 13, the parasitic gate capacitance is charged, thereby affecting the on or off speed of the GAA FET and reducing the high-frequency switching characteristics of the GAA FET.

[0060] To at least solve this problem, the embodiments of the present disclosure propose a main concept of providing an insulation layer between the lowermost metal gate 13 and the substrate 11 of the GAA FET in the related art to suppress the parasitic gate capacitance and thus improve the high-frequency switching characteristics of the GAA FET.

[0061] The technical solutions provided in the embodiments of the present disclosure will be described in detail below with reference to the accompanying drawings.

[0062] An embodiment of the present disclosure provides a method for manufacturing a semiconductor device, which may include the following steps S110 to S160.

[0063] At S110, a sacrificial region is formed on a surface of a substrate.

[0064] As shown in FIG. 3, a sacrificial region 101 is formed on a surface of a substrate 100. Here, the sacrificial region 101 refers to a sacrificial layer with a certain depth formed in the substrate 100, and the sacrificial layer has an upper surface coplanar with an upper surface of the substrate 100. The method for forming the sacrificial layer is not limited in the embodiments of the present disclosure in any way, as long as a greater etching selectivity is provided between the sacrificial region 101 and the substrate 100, and the sacrificial region 101 can be removed by selective etching in the subsequent process. As described below, the sacrificial region 101 is at a position corresponding to a position of a projection of a channel region of the semiconductor device on the substrate 100.

[0065] The substrate 100 includes a single crystal semiconductor layer on at least a surface portion thereof. The substrate 100 may include a single crystal semiconductor material such as, but not limited to, Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb and InP. In some implementations, the substrate 100 may be made of crystalline Si. The substrate 100 may include one or more buffer layers (not shown) in a surface region thereof. The buffer layer may be configured to gradually change a lattice constant from a lattice constant of the substrate to a lattice constant of a source/drain region. For example, the lattice constant of a plurality of buffer layers gradually changes from the lattice constant of the substrate to the lattice constant of the source/drain region, so as to reduce a difference in lattice constant between every two adjacent film layers (including the substrate and a buffer layer adjacent thereto, every two adjacent buffer layers, and the source/drain region and a buffer layer adjacent thereto). The buffer layer may be formed of an epitaxially grown single crystal semiconductor material, such as, but not limited to, Si, Ge, GeSn, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, GaN, GaP and InP. In some implementations, the substrate 100 may include a silicon germanium (SiGe) buffer layer epitaxially grown on a silicon substrate. The substrate 100 may further include various regions that have been appropriately doped with impurities (e.g., with p-type or n-type conductivity).

[0066] In some implementations of embodiments of the present disclosure, the step S110 may include steps S111 to S114.

[0067] At S111, a photoresist pattern 102 is formed on the substrate 100 by using a mask plate, where the photoresist pattern 102 exposes a preset region on the surface of the substrate 100, as shown in FIG. 2. The preset region is a region in which the sacrificial region 101 is to be formed.

[0068] At S112, ion implantation is performed in the preset region on the surface of the substrate 100.

[0069] As shown in FIG. 2, ion implantation is performed in the preset region masked by using the photoresist pattern 102 to form a doped region, i.e., the sacrificial region 101. The sacrificial region 101 may be, for example, an n-type doped region.

[0070] In some implementations, the ion implantation may be performed with a dose of $1 \times 10^{15}/\text{cm}^2$ to $5 \times 10^{16}/\text{cm}^2$, and the implanted impurity may be, for example, an n-type dopant. The sacrificial region 101 is formed in the substrate 100 by the ion implantation, where the sacrificial region 101 is an n-type heavily doped region, so that the etching selectivity between the formed sacrificial region 101 and the substrate 100 can be

increased. Optionally, the n-type dopant may include at least one of Sb, As and P.

[0071] In some implementations, to improve the pattern precision of the sacrificial region 101, the photoresist pattern 102 may include two layers, i.e., a lower double anti-reflective coating (DARC) layer (adjacent to the surface of the substrate 100) and a photoresist layer above the DARC. It should be understood by those skilled in the art that the photoresist pattern 102 may include more than two layers or may be a single layer.

[0072] At S113, the photoresist pattern 102 is removed.

[0073] Various photoresist removal processes may be employed to remove the photoresist pattern 102, which is not limited in the embodiments of the present disclosure in any way.

[0074] At S114, an annealing process is performed on the region in which the ion implantation is performed, so as to form the sacrificial region 101.

[0075] Lattice damage of the substrate may be caused by the ion implantation. To allow further epitaxial growth on the substrate, the substrate needs to undergo an annealing process so that the lattice-damaged region caused by ion implantation is recrystallized. In some implementations, the above annealing process is performed using a rapid thermal anneal (RTA) process.

[0076] At S120, a stacked structure is formed on the sacrificial region, the stacked structure including a first semiconductor layer and a second semiconductor layer alternately stacked.

[0077] As shown in FIGs. 7A and 7B, a stacked structure is formed on the sacrificial region 101, and the stacked structure may include a first semiconductor layer 110 and a second semiconductor layer 120 alternately stacked. In addition, a hard mask layer 130 is further provided above the stacked structure as a mask for etching the stacked structure.

[0078] The first semiconductor layer 110 and the second semiconductor layer 120 are made of materials with different lattice constants, and may each include one or more layers of Si, Ge, SiGe, GeSn, SiGeSn, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb or InP.

[0079] In some implementations, the first semiconductor layer 110 and the second semiconductor layer 120 are each made of Si, a Si compound, SiGe, Ge, or a Ge compound. In some implementations, the first semiconductor layer 110 includes Si, and the second semiconductor layer 120 includes SiGe. In some other implementations, the first semiconductor layer 110 may also include SiGe, and the first semiconductor layer 110 and the second semiconductor layer 120 have different Ge contents.

[0080] Although three first semiconductor layers 110 and three second semiconductor layers 120 are shown in FIGs. 7A and 7B, the embodiment of the present disclosure is not limited thereto, and more or fewer first semiconductor layers 110 or second semiconductor layers 120 are also possible. In some implementations, the number of first semiconductor layers 110 and the number of second semiconductor layers 120 each range from 2 to 20. A drive current of the GAA FET device can be adjusted by adjusting the numbers of first semiconductor layers 110 and/or second semiconductor layers 120.

[0081] The first semiconductor layer 110 and the second semiconductor layer 120 are epitaxially formed over the substrate 100. The first semiconductor layer 110 may have the same thickness as, or a different thickness from, that of the second semiconductor layer 120. Also, different first semiconductor layers 110 may have the same thickness or have different thicknesses; and different second semiconductor layers 120 may have the same thickness or have different thicknesses. This is not limited in the embodiments of the present disclosure in any way. In some implementations, the thickness of the first semiconductor layer 110 is in a range of 2nm to 20nm. In some implementations, the thickness of the second semiconductor layer 120 is in a range of 2nm to 20nm.

[0082] The hard mask layer 130 may be a single layer, or may include a plurality of layers, which is not limited in the embodiments of the present disclosure in any way. In some implementations, the hard mask layer 130 includes at least one of an oxide insulation layer and a nitride insulation layer. For example, the hard mask layer 130 may include a first hard mask layer 131 and a second hard mask layer 132 above the first hard mask layer 131. The first hard mask layer 131 may include silicon oxide, for example, may be a pad oxide layer made of silicon oxide, which may be formed by thermal oxidation. The second hard mask layer 132 may include silicon nitride, for example, may be made of silicon nitride (SiN), which is formed by chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or any other suitable process. The CVD includes low pressure CVD (LPCVD) and plasma enhance CVD (PECVD). The hard mask layer 130 is patterned into a mask pattern by a patterning process including photolithography and etching.

[0083] In some implementations of embodiments of the present disclosure, the above step S120 may include steps S121 to S125.

[0084] At S121, the first semiconductor layer 110 and the second semiconductor layer 120 alternately stacked are formed on the surface of the substrate 100, as shown in FIG.

4.

[0085] At S122, a hard mask layer 130 is formed above the first semiconductor layer 110 and the second semiconductor layer 120 alternately stacked, where a projection of the hard mask layer 130 on the substrate 100 corresponds to the sacrificial region 101, as shown in FIG. 4.

5 [0086] It should be noted that, before patterning, the hard mask layer 130, as a whole film, covers the entire substrate 100. A photoresist pattern is then formed by using a mask plate, and during patterning, excess portions of the hard mask layer 130 are etched away, thereby obtaining the patterned hard mask layer 130 shown in FIG. 4. The mask plate used in step S122 is the same as that used in step S111, and different photoresists are used in
10 the steps. In an implementation, a positive photoresist is used in step S122, while a negative photoresist is used in step S111. In another implementation, a negative photoresist is used in step S122, while a positive photoresist is used in step S111.

[0087] At S123, the first semiconductor layer 110, the second semiconductor layer 120 and the substrate 100 are etched by using the hard mask layer 130, so as to obtain the
15 stacked structure and form grooves in the substrate 100 on both sides of the stacked structure.

[0088] As shown in FIG. 5, in this step, after the first semiconductor layer 110 and the second semiconductor layer 120 alternately stacked are etched, the substrate 100 below may be further etched to form grooves in the substrate 100 on both sides of the stacked
20 structure, thereby facilitating subsequent formation of a shallow trench isolation (STI) structure.

[0089] In some implementations of this step, at least a part of the sidewall of the sacrificial region 101 may be exposed during formation of the grooves in the substrate 100 on both sides of the stacked structure. In a subsequent process, the sacrificial region
25 101 may be removed by selective lateral etching. However, in this implementation, while the sacrificial region 101 is laterally etched, channel regions in the first semiconductor layer 110 and the second semiconductor layer 120 may be damaged, thereby affecting the performance of the GAA FET device.

[0090] In some other implementations of this step, during formation of the grooves in
30 the substrate 100 on both sides of the stacked structure, an etching depth may be controlled, for example, by detecting an etching endpoint in an optical emission spectroscopy (OES) method, so that the etching depth reaches a level that just does not expose the sacrificial region 101. The subsequent steps are described below.

[0091] At S124, a protective layer 140 covering the stacked structure and the substrate

100 is formed, as shown in FIG. 6.

[0092] The protective layer 140 is configured to protect the channel regions from being laterally etched during the subsequent etching of the sacrificial region 101. The protective layer 140 may include a silicon nitride based material such as silicon nitride, SiON, SiOCN, or SiCN, and combinations thereof formed by CVD (including LPCVD and PECVD), PVD, ALD, or any other suitable process. In some implementations, the protective layer 140 is made of silicon nitride by, for example, ALD process, so that good compactness of the protective layer 140 can be ensured to protect the channel regions from being laterally etched during the subsequent etching of the sacrificial region 101.

[0093] At S125, anisotropic etching is performed on the protective layer 140 and the substrate 100, so that the protective layer on the sidewall of the stacked structure is retained as a sidewall protective layer 141, and at least a part of a sidewall of the sacrificial region 101 is exposed, as shown in FIGs. 7A and 7B.

[0094] In this step, the anisotropic etching may be performed using a process gas with a high etching rate, a high upper electrode radio frequency power and a high lower electrode radio frequency power, so that only the protective layer 140 in the horizontal direction and a part of the substrate 100 are etched, while the sidewall protective layer 141 is retained on the sidewall of the stacked structure and at least a part of the sidewall of the sacrificial region 101 is exposed. Preferably, the entire sidewall of the sacrificial region 101 is exposed to facilitate more complete removal of the sacrificial region 101 in a subsequent process. Here, the protective layer 140 in the horizontal direction refers to the protective layer 140 laid in the horizontal direction or an oblique direction close to the horizontal direction, for example, a portion of the protective layer 140 covering the surface of the substrate 100, and a portion of the protective layer 140 covering the hard mask layer 130.

[0095] The high lower electrode radio frequency power may be adopted to provide downward acceleration energy and direction for plasma, the high upper electrode radio frequency power may be adopted to produce more plasma, and the process gas with a high etching rate is adopted to enhance directivity of the anisotropic etching, so that lateral etching of the protective layer 140 on the sidewall of the stacked structure is minimized while the protective layer 140 in the horizontal direction and a part of the substrate 100 are etched to expose at least a part of the sidewall of the sacrificial region 101, thereby providing protection for the channel regions in the subsequent etching process. It should be understood by those skilled in the art that the upper electrode radio frequency power

generally refers to a radio frequency power applied to a radio frequency coil located at a top of a process chamber, and in some implementations, the radio frequency coil may be located on a side of a process chamber for ionizing the process gas to produce plasma. The lower electrode radio frequency power generally refers to a radio frequency power applied to a lower electrode assembly in a process chamber, and the lower electrode assembly includes a wafer carrier and is used for generating a radio frequency bias to improve directivity of the plasma.

[0096] In some implementations, the protective layer 140 includes silicon nitride, the substrate 100 includes silicon, and the process gas may include chlorine or a fluorocarbon-based gas. The fluorocarbon-based gas may be, for example, CF_4 or CHF_3 . Apparently, in the etching process, the process gas may further include a protective gas to provide protection for the protective layer 140 on the sidewall, and the protective gas may include at least one of N_2 and CH_4 . More specifically, the upper electrode radio frequency power ranges, for example, from 100W to 3000W, and the lower electrode radio frequency power ranges, for example, from 50W to 1000W.

[0097] At S130, the sacrificial region is removed to form a cavity between the substrate and the stacked structure.

[0098] As shown in FIGs. 8A to 8C, the sacrificial region 101 between the substrate 100 and the stacked structure may be removed by selective etching, thereby forming a cavity 103.

[0099] In contrast to step S125, the substrate 100 is subjected to isotropic etching in this step to remove the sacrificial region 101. Therefore, in this step, the lower electrode radio frequency power is not applied, while a lower upper electrode radio frequency power is applied. The upper electrode radio frequency power in this step is lower than that in step S125. In the etching process, the sacrificial region 101 is etched in a low-pressure environment, which means that a lower chamber pressure, which is, for example, lower than the chamber pressure in step S125, is adopted to increase a free path of etching ions, so as to enable complete removal of the sacrificial region 101. Specifically, the chamber pressure used in step S130 is from 5 mTorr to 800 mTorr.

[0100] In some implementations, the etching gas used for the isotropic plasma etching in step S130 is an etching gas that makes an etching selectivity between the sacrificial region 101 and the substrate 100 greater than a preset value, which can ensure that the sacrificial region 101 is completely removed without damaging the structure of the semiconductor device. For example, the substrate 100 includes silicon, and the sacrificial

region 101 includes heavily doped n-type silicon, in which case chlorine may be selected as an etching gas to increase an etching selectivity between the heavily doped n-type silicon and silicon and an etching selectivity between the heavily doped n-type silicon and silicon nitride. The etching selectivity between the heavily doped n-type silicon and silicon is greater than 200 (i.e., the preset value). Further, the etching selectivity is, for example, greater than (200-250): 1, which can ensure that the sacrificial region 101 is completely removed without damaging the structure of the semiconductor device. On the basis, in some embodiments, the sidewall protective layer 141 includes silicon nitride, an uppermost second hard mask layer 132 in the hard mask layer 130 includes silicon nitride, and the etching selectivity between the heavily doped n-type silicon and silicon nitride is greater than 200. Further, the etching selectivity is, for example, greater than (200-250): 1. It should be noted that, in order to ensure that the sacrificial region 101 is completely removed while the substrate 100, the sidewall protective layer 141 and the second hard mask layer 132 are hardly etched, it is necessary to make the etching selectivity between the sacrificial region 101 and the sidewall protective layer 141 and the etching selectivity between the sacrificial region 101 and the second hard mask layer 132 high enough while making the etching selectivity between the sacrificial region 101 and the substrate 100 greater than the preset value.

[0101] It will be understood that the embodiments of the present disclosure are not limited thereto, and the sacrificial region, the substrate, the sidewall protective layer, and the hard mask layer may be made of other materials. A person skilled in the art may reasonably select an etching gas to be used according to the materials of the sacrificial region, the substrate, the sidewall protective layer, and the hard mask layer, as long as the etching selectivity between the sacrificial region 101 and the substrate 100, the etching selectivity between the sacrificial region 101 and the sidewall protective layer 141, and the etching selectivity between the sacrificial region 101 and the second hard mask layer 132 are high enough, which is not described in detail here.

[0102] At S140, the cavity is filled with an insulation layer.

[0103] As shown in FIGs. 10A to 10C, by filling the cavity with an insulation layer 151, the insulation layer 151 is formed between the lowermost gate structure of the GAA FET to be formed subsequently and the substrate 100, so that the parasitic gate capacitance between the lowermost gate structure and the substrate can be suppressed, and the high-frequency switching characteristics of the semiconductor device can be improved. In some implementations, the insulation layer 151 may include, for example, silicon nitride, silicon

oxide, silicon oxynitride, or the like, and the material and filling manner of the insulation layer 151 are not limited in the present disclosure in any way.

[0104] In some implementations of embodiments of the present disclosure, the above step S140 may include steps S141 to S142.

5 [0105] At S141, the insulation layer 150 is deposited around the stacked structure and on the surface of the substrate 100 until the insulation layer 150 below the stacked structure at the cavity 103 is attached to the insulation layer 150 above the substrate 100 at the cavity 103, as shown in FIGs. 9A to 9C.

[0106] It should be understood by those skilled in the art that the horizontal line marked
10 between the insulation layer 150 under the stacked structure at the cavity 103 and the insulation layer 150 above the substrate 100 at the cavity 103 in FIGs. 9A to 9C is merely for the purpose of better illustration, and in the embodiments of the present disclosure, the insulation layer 150 is formed by continuously deposition, such that the insulation layer 150 under the stacked structure at the cavity 103 is attached to the insulation layer
15 150 above the substrate 100 at the cavity 103, and it is not intended to limit the insulation layer 150 to be divided into two layers intentionally. In other words, in the cavity 103, one part of the insulation layer 150 gradually increases in thickness from the top of the cavity 103 (i.e., the lower surface of the stacked structure in the cavity 103) downwards, while the other part of the insulation layer 150 gradually increases in thickness from the
20 bottom of the cavity 103 (i.e., the upper surface of the substrate 100 in the cavity 103) upwards, and surfaces of the two parts of the insulation layer 150 opposite to each other gradually approach to each other along with the increases in thickness until the two parts are attached to each other.

[0107] To enable deposition of the process gas deep inside the cavity 103, the insulation
25 layer 150 may be formed by low-pressure CVD (LPCVD) or atomic layer deposition (ALD) or other processes. Further, the insulation layer 150 may be formed by ALD process to better fill the cavity 103.

[0108] Since the insulation layer 150 outside the cavity needs to be removed in a subsequent process, and only the insulation layer 150 inside the cavity is retained, in some
30 embodiments, a high etching selectivity is required between the insulation layer 150 and the substrate 100 and between the insulation layer 150 and the sidewall protective layer 141, so that the insulation layer 150 outside the cavity can be selectively removed.

[0109] At S142, the insulation layer 150 outside the cavity 103 is removed.

[0110] As shown in FIGs. 10A to 10C, the insulation layer 150 outside the cavity 103

may be removed by dry etching or wet etching, and after the portion outside the cavity 103 is removed, only a portion of the insulation layer 150 retained inside the cavity 103 is used as the insulation layer 151. In some implementations, the insulation layer 150 includes silicon oxide, the sidewall protective layer 141 includes silicon nitride, and the substrate 100 includes silicon, so that the etching selectivity between the insulation layer 150 and the sidewall protective layer 141 and the etching selectivity between the insulation layer 150 and the substrate 100 are relatively high, which can facilitate removal of the insulation layer 150 outside the cavity 103.

[0111] In some implementations, the above step S140 may further include step S143.

[0112] At S143, an annealing process is performed on the insulation layer 151.

[0113] By performing the annealing process on the insulation layer 151, lattice defects in the insulation layer 151 can be reduced, the compactness of the insulation layer 151 can be increased, and the high-voltage tolerance of the insulation layer 151 can be improved, thereby improving the reliability of the insulation layer 151.

[0114] It should be noted that the annealing process in step S143 may be performed before or after the removal of the insulation layer outside the cavity in step S142, which is not limited in the embodiments of the present disclosure in any way. The annealing process may be implemented by, for example, rapid thermal anneal process or laser anneal process.

[0115] In some implementations, after step S143, the method may further include steps S144 to S145.

[0116] At S144, the sidewall protective layer 141 and the hard mask layer 130 are removed, as shown in FIG. 11.

[0117] In some implementations, the sidewall protective layer 141 and the hard mask layer 130 exhibit high etching selectivities relative to the substrate 100, the first semiconductor layer 110 and the second semiconductor layer 120, thereby facilitating the removal of the sidewall protective layer 141 and the hard mask layer 130.

[0118] At S145, the grooves are filled to form shallow trench isolation structures 160, as shown in FIG. 11. Isolation between the GAA FETs can be achieved by the shallow trench isolation structures 160.

[0119] In some implementations, before step S150, the method may further include step S146.

[0120] At S146, a source region and a drain region (hereafter collectively referred to as "source/drain regions 200") are formed respectively on two sides of the region of the

stacked structure in which the gate structure is to be formed, as shown in FIG. 12.

[0121] Specifically, step S146 may include: forming a sacrificial gate in a region where the gate structure is to be formed; doping the stacked structure on both sides of the sacrificial gate to form the source/drain regions 200; forming an isolation layer 210 and an isolation pad 220 on both sides of the sacrificial gate to cover tops and sides of the source/drain regions 200, respectively; and removing the sacrificial gate to expose the channel region between the source/drain regions 200, thereby obtaining the semiconductor structure shown in FIG. 12. The above process steps belong to conventional process steps in the art, and are not described in detail here.

[0122] At S150, one of the first semiconductor layer 110 and the second semiconductor layer 120 is removed.

[0123] As shown in FIGs. 13A and 13B, the first semiconductor layer 110 is removed so that a plurality of voids 111 are formed in the region corresponding to the gate structure.

[0124] For a GAA FET with a Si, SiGe or Ge based channel, Si is typically used for an n-channel GAA FET, while SiGe or Ge is used for a p-channel GAA FET. In the case of a SiGe p-channel GAFET, a higher Ge concentration can improve the performance of the transistor. Those skilled in the art may select to remove the first semiconductor layer 110 or the second semiconductor layer 120 as needed.

[0125] At S160, a gate structure 121 is formed around the other of the first semiconductor layer 110 and the second semiconductor layer 120.

[0126] In some embodiments, the gate structure 121 includes a gate dielectric layer arranged around the other of the first semiconductor layer 110 and the second semiconductor layer 120, and a gate electrode layer arranged around the gate dielectric layer. Further, the other of the first semiconductor layer 110 and the second semiconductor layer 120 surrounded by the gate structure 121 is formed as a channel region of the semiconductor device. For example, as shown in FIGs. 14A and 14B, the gate structure 121 is formed around the second semiconductor layer 120, and the second semiconductor layer 120 surrounded by the gate structure 121 is formed as a channel region of the GAA FET. The gate structure 121 may include a gate dielectric layer and a gate electrode layer arranged around the second semiconductor layer 120.

[0127] In some implementations, the gate dielectric layer may include one or more layers of dielectric materials (such as silicon oxide, silicon nitride, or high-k dielectric materials), other suitable dielectric materials, and /or combinations thereof. The high-k dielectric material may include, for example, HfO₂, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO,

zirconium oxide, aluminum oxide, titanium oxide, an $\text{HfO}_2\text{-Al}_2\text{O}_3$ alloy, any other suitable high-k dielectric material, and /or combinations thereof. In some embodiments, an interface layer may be formed between the channel region and the gate dielectric layer. The gate dielectric layer may be formed by CVD, ALD, or any other suitable method. In an optional embodiment, the gate dielectric layer has a thickness ranging from about 1nm to about 6nm.

[0128] In some implementations, the gate electrode layer may include one or more layers of conductive materials, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, alloys thereof, other suitable materials, and /or combinations thereof. The gate electrode layer may be formed by CVD, ALD, electroplating, or any other suitable method.

[0129] In some implementations, the above process steps belong to conventional process steps in the art, and the gap between two isolation layers 210 may be filled with an insulating overlayer, which is not described in detail here.

[0130] In the method for manufacturing a semiconductor device according to the embodiments of the present disclosure, an insulation layer is formed between the lowermost gate structure in the semiconductor device and the substrate, so that the parasitic gate capacitance between the lowermost gate structure and the substrate is suppressed, and the high-frequency switching characteristics of the semiconductor device are improved.

[0131] The above embodiments of the present disclosure emphasize the differences between various embodiments, and different optimization features between the embodiments can be combined to form a better embodiment as long as they are not contradictory, and further description is omitted here in view of brevity of the text.

[0132] The above are only embodiments of the present disclosure and are not intended to limit the present disclosure. Those skilled in the art knows well that various modifications and changes may be made to the present disclosure. Any amendments, equivalent substitutions, improvements, and the like within the spirit and principle of the present disclosure are included in the scope of protection defined by the appended claims of the present disclosure.

What is claimed is:

1. A method for manufacturing a semiconductor device, comprising:
forming a sacrificial region on a surface of a substrate;
5 forming a stacked structure on the sacrificial region, the stacked structure comprising a first semiconductor layer and a second semiconductor layer alternately stacked;
removing the sacrificial region to form a cavity between the substrate and the stacked structure;
10 filling the cavity with an insulation layer;
removing one of the first semiconductor layer and the second semiconductor layer; and
forming a gate structure around the other of the first semiconductor layer and the second semiconductor layer.
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2. The method for manufacturing the semiconductor device according to claim 1, wherein forming the sacrificial region on the surface of the substrate comprises:
performing ion implantation in a preset region on the surface of the substrate;
and
20 performing an annealing process on the region in which the ion implantation is performed, so as to form the sacrificial region.
3. The method for manufacturing the semiconductor device according to claim 2, wherein the ion implantation is performed for n-type doping with a dose of
25 $1 \times 10^{15}/\text{cm}^2$ to $5 \times 10^{16}/\text{cm}^2$.
4. The method for manufacturing the semiconductor device according to claim 3, wherein a dopant for the n-type doping comprises at least one of Sb, As and P.
- 30 5. The method for manufacturing the semiconductor device according to claim 1, wherein forming the stacked structure on the sacrificial region comprises:
forming the first semiconductor layer and the second semiconductor layer alternately stacked on the surface of the substrate; and
etching the first semiconductor layer and the second semiconductor layer

alternately stacked to obtain the stacked structure and expose at least a part of a sidewall of the sacrificial region.

6. The method for manufacturing the semiconductor device according to claim 5, wherein etching the first semiconductor layer and the second semiconductor layer alternately stacked comprises:

forming a hard mask layer above the first semiconductor layer and the second semiconductor layer alternately stacked, wherein a projection of the hard mask layer on the substrate corresponds to the sacrificial region; and

etching the first semiconductor layer, the second semiconductor layer and the substrate by using the hard mask layer to form the stacked structure and form grooves in the substrate on both sides of the stacked structure.

7. The method for manufacturing the semiconductor device according to claim 6, wherein the at least a part of the sidewall of the sacrificial region is exposed during formation of the grooves in the substrate on both sides of the stacked structure.

8. The method for manufacturing the semiconductor device according to claim 6, wherein forming the stacked structure on the sacrificial region further comprises:

forming a protective layer covering the stacked structure and the substrate; and performing anisotropic etching on the protective layer and the substrate, so that the protective layer on the sidewall of the stacked structure is retained as a sidewall protective layer, and the at least a part of the sidewall of the sacrificial region is exposed.

9. The method for manufacturing the semiconductor device according to claim 8, wherein forming the protective layer covering the stacked structure and the substrate comprises:

forming the protective layer by atomic layer deposition (ALD) process; or forming the protective layer comprising a silicon nitride based material; or forming the protective layer comprising at least one of silicon nitride, SiON, SiOCN or SiCN.

10. The method for manufacturing the semiconductor device according to claim

8, wherein performing anisotropic etching on the protective layer comprises:

performing the anisotropic etching using a process gas with a high etching rate, a high upper electrode radio frequency power and a high lower electrode radio frequency power.

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11. The method for manufacturing the semiconductor device according to claim 10, wherein the process gas comprises chlorine or a fluorocarbon-based gas; or

the upper electrode radio frequency power ranges from 100W to 3000W, and the lower electrode radio frequency power ranges from 50W to 1000W.

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12. The method for manufacturing the semiconductor device according to claim 6, wherein the hard mask layer comprises at least one of an oxide insulation layer and a nitride insulation layer; or

the hard mask layer comprises a first hard mask layer and a second hard mask layer above the first hard mask layer, wherein the first hard mask layer comprises silicon oxide, and the second hard mask layer comprises silicon nitride.

13. The method for manufacturing the semiconductor device according to claim 1, wherein removing the sacrificial region comprises:

performing isotropic plasma etching on the sacrificial region.

14. The method for manufacturing the semiconductor device according to claim 13, wherein performing isotropic plasma etching on the sacrificial region comprises:

etching the sacrificial region in a low-pressure environment without loading a lower electrode radio frequency power.

15. The method for manufacturing the semiconductor device according to claim 14, wherein the low-pressure environment is from 5 mTorr to 800 mTorr.

16. The method for manufacturing the semiconductor device according to claim 13, wherein an etching gas used for the isotropic plasma etching is an etching gas that makes an etching selectivity between the sacrificial region and the substrate greater than a preset value.

17. The method for manufacturing the semiconductor device according to claim 16, wherein the substrate comprises silicon, the sacrificial region comprises heavily doped n-type silicon, and the etching gas used for the isotropic plasma etching is chlorine; and

5 the etching selectivity between the sacrificial region and the substrate is greater than 200.

18. The method for manufacturing the semiconductor device according to claim 1, wherein the first semiconductor layer and the second semiconductor layer are made
10 of semiconductor materials with different lattice constants.

19. The method for manufacturing the semiconductor device according to claim 18, wherein each of the first semiconductor layer and the second semiconductor layer comprises at least one of Si, Ge, SiGe, GeSn, SiGeSn, GaAs, InSb, GaP, GaSb, InAlAs,
15 InGaAs, GaSbP, GaAsSb and InP.

20. The method for manufacturing the semiconductor device according to any one of claims 1 to 19, wherein filling the cavity with the insulation layer comprises:

20 depositing the insulation layer around the stacked structure and on the surface of the substrate until the insulation layer below the stacked structure at the cavity is attached to the insulation layer above the substrate at the cavity; and

removing the insulation layer outside the cavity.

21. The method for manufacturing the semiconductor device according to claim
25 20, wherein depositing the insulation layer around the stacked structure and on the surface of the substrate comprises:

depositing the insulation layer by ALD process.

22. The method for manufacturing the semiconductor device according to claim
30 20, further comprising:

performing an annealing process on the insulation layer.

23. The method for manufacturing the semiconductor device according to claim 8, further comprising:

removing the sidewall protective layer and the hard mask layer; and
filling the grooves to form shallow trench isolation structures.

24. The method for manufacturing the semiconductor device according to claim
5 1, wherein before removing one of the first semiconductor layer and the second
semiconductor layer, the method further comprises:

respectively forming a source region and a drain region on two sides of a region
of the stacked structure in which the gate structure is to be formed.

10 25. The method for manufacturing the semiconductor device according to claim
1, wherein the gate structure comprises a gate dielectric layer arranged around the
other of the first semiconductor layer and the second semiconductor layer, and a gate
electrode layer arranged around the gate dielectric layer; and

the other of the first semiconductor layer and the second semiconductor layer
15 surrounded by the gate structure is formed as a channel region of the semiconductor
device.