CATALYST INFLUENCED PATTERN TRANSFER TECHNOLOGY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 62/591,326 filed November 28, 2017 entitled "Forming Three-Dimensional Memory Architectures Using Catalyst Mesh Patters," U.S. Provisional Patent Application No. 62/665,084 filed on May 1, 2018 entitled "Multilayer Electrochemical Etch process for Semiconductor Device Fabrication," U.S. Provisional Patent Application No. 62/701,049 filed on June 20, 2018 entitled Catalyst-Based Electrochemical Etch Process for Semiconductor Device Fabrication," and U.S. Provisional Patent Application No. 62/729,361 filed on September 10, 2018 entitled "Catalyst Assisted Chemical Etching Technology: Applications In Semiconductor Devices," all of which are incorporated herein by reference in their entirety for all purposes.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0002] This invention was made with government support under Grant No. EEC1160494 awarded by the National Science Foundation and Grant No. FA8650-15-C-7542 awarded by the Air Force Research Laboratory. The U.S. government has certain rights in the invention.

TECHNICAL FIELD

[0003] Various embodiments of the present technology generally relate to semiconductor device architectures and manufacturing techniques. More specifically, some embodiments of the present technology relate to silicon etching using catalyst influenced chemical etching technology with application to three-dimensional memory architectures and transistors.

BACKGROUND

[0004] Semiconductor manufacturing of various types of transistors, memories, integrated circuits, photonic devices and other semiconductor devices have led to the proliferation of modern computing devices and other electronic systems. For example, computers, mobile phones, automobiles, consumer electronics, and the like are all a direct product of advancements in semiconductor manufacturing. An integral part of fabrication of these devices is pattern transfer. Dry plasma etching processes, which are used in the semiconductor industry for anisotropically etching highly controlled nanopatterns, require expensive vacuum equipment and cannot retain

cross-section shape easily when patterning high aspect ratios. They suffer from etch challenges such as Aspect Ratio Dependent Etching (ARDE) and etch taper.

SUMMARY

[0005] Various embodiments of the present technology generally relate to memory architectures and manufacturing techniques. More specifically, some embodiments of the present technology relate to silicon etching using catalyst influenced chemical etching technology with application to three-dimensional memory architectures and transistors.

[0006] In one embodiment of the present technology, a method for preventing substantial collapse of high aspect ratio semiconducting structures by catalyst influenced chemical etching comprises patterning a catalyst layer on a surface of a semiconducting material, where the catalyst layer comprises an intended design and lithographic links. Furthermore, the lithographic links substantially connect one or more isolated features of the catalyst layer and/or the semiconducting material. The method further comprises exposing the patterned catalyst layer on the surface of the semiconducting material to an etchant, where the patterned catalyst layer causes etching of the semiconducting material to form interconnected high aspect ratio structures.

[0007] In another embodiment of the present technology, a method for preventing substantial collapse of high aspect ratio semiconducting structures comprises creating a structure with a capping material deposited on either a patterned catalyst layer or on top of low height structures. The method further comprises exposing the structure to an etchant. The method additionally comprises forming high aspect ratio semiconducting structures by using catalyst influenced chemical etching on the structure with the capping material to prevent substantial collapse of the high aspect ratio semiconducting structures.

[0008] In a further embodiment of the present technology, an apparatus for catalyst influenced chemical etching comprises a plurality of sensors configured to detect an etch state of a semiconducting material.

[0009] In another embodiment of the present technology, a method for making substantially non-collapsing alternating multi-layer stacked nanostructures comprises creating a material stack comprising two or more layers of alternating semiconducting films, where each of the two or more layers of alternating semiconducting films is different from another in at least one of the following properties: material, doping concentration and dopant material. The method further comprises etching the material stack by catalyst influenced chemical etching such that layers differing in the

properties produce etched nanostructures differing in at least one of the following: morphology, porosity, etch rates and thermal processing rates.

[0010] In a further embodiment of the present technology, a method for making substantially non-collapsing alternating multi-layer stacked features comprises creating a material stack comprising two or more layers of alternating semiconducting films, where each of the two or more layers of alternating semiconducting films is different from another in at least one of the following properties: material, doping concentration and dopant material. The method further comprises etching the material stack by a crystallographic orientation dependent etch to form a taper along a crystal plane. The method additionally comprises etching the taper along the crystal plane to reveal one of the two or more layers of alternating semiconducting films while etching part of another layer to create a staircase structure.

[0011] Embodiments of the present technology also include computer-readable storage media containing sets of instructions to cause one or more processors to perform the methods, variations of the methods, and other operations described herein.

[0012] While multiple embodiments are disclosed, still other embodiments of the present technology will become apparent to those skilled in the art from the following detailed description, which shows and describes illustrative embodiments of the technology. As will be realized, the technology is capable of modifications in various aspects, all without departing from the scope of the present technology. Accordingly, the drawings and detailed description are to be regarded as illustrative in nature and not restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Embodiments of the present technology will be described and explained through the use of the accompanying drawings in which:

[0014] Fig. 1A illustrates a jet and flash imprint lithography (J-FIL) enabled catalyst influenced chemical etching (CICE) for shaped nanowires according to one or more embodiments of the present technology;

[0015] Fig. 1B depicts the cross-sectional views of fabricating nanowires using the steps described in Fig. 1A in accordance with one or more embodiments of the present technology;

[0016] Fig. 2 illustrates a SiSE (Silicon Superlattice Etch) process control according to one or more embodiments of the present technology;

[0017] Figs. 3A-3B show the steep interface between porous and non-porous layers after SiSE on a substrate with alternating layers of epitaxial silicon with different doping concentrations according to one or more embodiments of the present technology;

[0018] Fig. 4 shows an SEM cross-section of silicon nanowires created with gold and platinum catalysts, and zoomed in images of the catalyst meshes at the bottom of the nanostructures, according to one or more embodiments of the present technology;

[0019] Fig. 5A shows how connecting links in the catalyst material as well as the semiconductor structures can be used to connect one or more isolated catalysts and high aspect ratio (HAR) nanostructures simultaneously according to one or more embodiments of the present technology;

[0020] Fig. 5B provides a top view illustrating disconnected regions representing the geometry of the catalyst features and connected regions that define the high aspect ratio structures that remain after SiSE according to one or more embodiments of the present technology;

[0021] Figs. 6A-6E illustrate process chamber configurations for CICE according to one or more embodiments of the present technology;

[0022] Figs. 7A-7B illustrate an embodiment of MSP-CICE process chamber with a horizontal substrate according to one or more embodiments of the present technology;

[0023] Fig. 8A illustrates an embodiment of MSP-CICE tool setup according to one or more embodiments of the present technology;

[0024] Fig. 8B illustrates an example of a detailed process chamber layout according to one or more embodiments of the present technology;

[0025] Fig. 8C illustrates an example of a process flow according to one or more embodiments of the present technology;

[0026] Fig. 9 illustrates a genetic algorithm based controller which can be used to determine optimum process parameters for a targeted output according to one or more embodiments of the present technology;

[0027] Figs. 10A-10E illustrate catalyst mesh examples according to one or more embodiments of the present technology;

[0028] Fig. 11 shows a process flow for HAR etch of channels and slits with a catalyst mesh pattern similar to that shown in Fig 10;

[0029] Fig. 12 illustrates a sacrificial process flow for vertical channel 3D NAND according to one or more embodiments of the present technology;

[0030] Fig. 13 shows the process flows and various pathways to make 3D NAND arrays with SiSE according to one or more embodiments of the present technology;

[0031] Figs. 14-16 show some of the process flows for processing alternating layers of porous and non-porous silicon layers that are created by SiSE to create vertical channel 3D NAND arrays according to one or more embodiments of the present technology;

[0032] Fig. 17 depicts an embodiment of the 3D NAND architecture with vertical gates and horizontal silicon channels according to one or more embodiments of the present technology;

[0033] Fig. 18A-18C show layouts and dimensions of 3D NAND according to one or more embodiments of the present technology;

[0034] Figs.19A-19C show an exemplary fabrication template for making patterns shown in Figs. 18A-18C;

[0035] Fig. 19D provides an example of a pattern with lithographic links where the links are made with imprint lithography (whose template is made with electron beam lithography), and the dots are aligned and printed using imprint or photolithography or vice versa;

[0036] Figs. 20A-20J illustrate exemplary photolithography process steps to pattern the CICE catalyst according to one or more embodiments of the present technology;

[0037] Figs. 21A-21H show the process flow for making a catalyst pattern with substantially connected catalyst features using self-assembly and lithography according to one or more embodiments of the present technology;

[0038] Fig. 22 illustrates an example of a 3D NAND staircase etch according to one or more embodiments of the present technology;

[0039] Fig. 23 illustrates a process of staircase etch on bulk silicon with alkaline etchants or angled plasma etch to create contact pads for word lines according to one or more embodiments of the present technology;

[0040] Fig. 24 illustrates an exemplary DRAM design with transistor, capacitor and interconnect material on nanowires etched by CICE according to one or more embodiments of the present technology;

[0041] Figs. 25A-25B illustrate two process flows for CICE wet anisotropic etch to create high aspect ratio pillars without collapse according to one or more embodiments of the present technology;

[0042] Fig. 26 illustrates a SEM image showing collapse of unsupported features vs supported features after CICE on silicon according to one or more embodiments of the present technology;

[0043] Fig. 27A illustrates a 14nm FinFET with a taper angle of ~85^0, and a physical Half Pitch (HP) of 24nm (Ref: TechInsights);

[0044] Fig. 27B depicts the maximum fin height for different fin widths and etch taper angles according to one or more embodiments of the present technology.

[0045] Fig. 28 is a plot illustrating a maximum height of a fin with no taper before lateral collapse along the length of a 50nm long fin, without any support/assist features;

[0046] Fig. 29 illustrates an example of a process flow for making finFETs with CICE according to one or more embodiments of the present technology;

[0047] Figs. 30A-30E illustrates an example of FinFET fabrication process steps after CICE according to one or more embodiments of the present technology;

[0048] Fig. 31 illustrates an example of a process flow for making nanosheet FETs and lateral nanowire FETs with CICE according to one or more embodiments of the present technology;

[0049] Fig. 32A illustrates connecting links when number of fins is greater than 1;

[0050] Fig. 32B illustrates links connecting all the fins with isolated catalysts (top) or with connected links and connected catalysts (bottom);

[0051] Fig. 32C is a plot illustrating critical heights before collapse along the length of the connected fin structure is shown for different fin widths f and for number of fins ranging from 1 to 10; and

[0052] Fig. 32D is a plot illustrating the critical heights before collapse along the width of the connected fin structure is shown for different fin widths f and for number of fins ranging from 1 to 10.

[0053] The drawings have not necessarily been drawn to scale. Similarly, some components and/or operations may be separated into different blocks or combined into a single block for the purposes of discussion of some of the embodiments of the present technology. Moreover, while the technology is amenable to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and are described in detail below. The intention, however, is not to limit the technology to the particular embodiments described. On the contrary, the technology is intended to cover all modifications, equivalents, and alternatives falling within the scope of the technology as defined by the appended claims.

DETAILED DESCRIPTION

[0054] Various embodiments of the present technology describe a novel anisotropic etching process. A fabrication tool for this purpose is also disclosed. This shall enable adoption of this technology in making semiconductor devices. Some embodiments use a catalyst influenced chemical etching (CICE) for manufacture of transistors and various memory architectures. Moreover, various embodiments of the CICE process have demonstrated extremely high aspect ratios without loss of feature size.

[0055] Various embodiments of the present technology also provide various control schemes in catalyst based chemical etching. A wafer scale Multi Scale Precision Catalyst Influenced Chemical Etching (MSP-CICE) fabrication tool for this purpose is also disclosed. Some embodiments use various control schemes and tool designs to extend the capabilities of CICE from small area (sub-150mm substrates) with no etch depth control in literature today, to large area (e.g. 300mm Si wafers) with local and global control and metrology. This shall enable adoption of this technology in making semiconductor devices such as 3D NAND Flash, DRAM, FinFETs and Nanosheet transistors.

[0056] Various embodiments of the present technology generally relate to memory architectures and manufacturing techniques. More specifically, some embodiments of the present technology relate to silicon etching using catalyst influenced chemical etching technology with application to three-dimensional memory architectures and transistors. Scalability of advanced memory architectures by current pattern transfer techniques is limited by non-zero taper, sidewall damage and etch mask degradation due to high aspect ratio plasma etching. Nonvolatile

semiconducting memories, such as three-dimensional (3D) NAND flash, need extremely high aspect ratio etching of > 64 layers of alternating material to increase the storage capacity of flash drives. With increasing layers, the cost and reliability of anisotropic high aspect ratio channel and trench etching, as well as a staircase etch for defining contacts to each layer, becomes a major limiting factor for scaling. A non-zero plasma etch taper angle limits the maximum number of tier stacking that can be reliably achieved.

[0057] Dry plasma etching processes, which are used in the semiconductor industry for anisotropically etching highly controlled nanopatterns, require expensive vacuum equipment and cannot retain cross-section shape easily when patterning high aspect ratios. They suffer from etch challenges such as Aspect Ratio Dependent Etching (ARDE) and etch taper. For the 3D NAND Flash designs, etching circular channels and rectangular slits simultaneously cannot be achieved reliably with plasma etching with accurate control of sidewalls. Similarly, for the features with connecting links, the sub-10nm links between pillars cannot be retained over high aspect ratios.

[0058] Furthermore, DRAM scaling is limited by the area occupied by the capacitor and the cell size factor. Hence, the current techniques in scaling memory architectures are limited due to the high number of lithography and high aspect ratio etch steps. Various embodiments provide improved techniques for DRAM manufacturing.

[0059] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of embodiments of the present technology. It will be apparent, however, to one skilled in the art that embodiments of the present technology may be practiced without some of these specific details.

[0060] The techniques introduced here can be embodied as special-purpose hardware (e.g., circuitry), as programmable circuitry appropriately programmed with software and/or firmware, or as a combination of special-purpose and programmable circuitry. Hence, embodiments may include a machine-readable medium having stored thereon instructions which may be used to program a computer (or other electronic devices) to perform a process. The machine-readable medium may include, but is not limited to, optical disks, compact disc read-only memories (CD-ROMs), magneto-optical disks, ROMs, random access memories (RAMs), erasable programmable read-only memories (EPROMs), electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, flash memory, or other type of media / machine-readable medium suitable for storing electronic instructions.

[0061] The phrases "in some embodiments," "according to some embodiments," "in the embodiments shown," "in other embodiments," and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one implementation of the present technology, and may be included in more than one implementation. In addition, such phrases do not necessarily refer to the same embodiments or different embodiments.

[0062] Various embodiments of the present technology use catalyst influenced chemical etching (CICE) for manufacture of transistors and various memory architectures. CICE is a catalyst based etching method that can be used on semiconductors such as Si, Ge, Si_xGe_{1-x}, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. as well as multilayers of the semiconductors. CICE uses a catalyst to etch semiconducting substrates and it has been used to fabricate high aspect ratio features with patterning techniques such as photolithography, electron beam lithography, nanosphere lithography, block co-polymers, laser interference lithography, colloidal lithography, double patterning, quad patterning, nanoimprint lithography and anodized aluminum oxide (AAO) templates to pattern the catalyst. The catalyst can be used in conjunction with etch-retarding materials such as polymer, Cr, etc.

[0063] In some embodiments, this setup can be immersed in a solution containing an etchant (e.g., fluoride species HF, NH_4F, Buffered HF, H_2SO_4, H_2O) and an oxidant (H_2O_2, V_2O_5, $KMnO_4$, dissolved oxygen, etc.). Other chemicals such as alcohols (ethanol, isopropyl alcohol, ethylene glycol), materials to regulate etch uniformity (surfactants, soluble polymers, dimethyl sulfoxide-DMSO), solvents (DI water, DMSO etc.), and buffer solutions can also be included in the etch composition. The chemicals used can depend on the semiconducting substrate to be etched. Non-aqueous etchants can also be used if needed. The etchants can be in liquid or vapor phase. An embodiment of such an etchant for silicon substrates comprises DI H_2O, H_2O_2, Ethanol and HF.

[0064] Materials such as metals (e.g., Ag, Au, Pd, Pt, Cu, W, Ru, Ir), compounds such as TiN, TaN, RuO_2, IrO_2 and other conductive metal oxides and nitrides, Graphene, carbon etc. can act as catalysts for CICE. The mechanism for the CICE process for etching Si may involve the reduction of the oxidant by a catalyst, thereby creating positively charged holes h^+. These holes are then injected through the metal to the metal-semiconductor interface thereby oxidizing the semiconductor underneath the metal. The oxidized silicon is dissolved by the fluoride component of the etchant that diffuses from the sides of and through the catalyst and the soluble products diffuse away. For CICE of silicon with HF and H_2O_2, this redox reaction can also produce

hydrogen gas. The variable n=2 to 4 is determined by the ratio of oxidant to HF which determines the etch regime that occurs:

$$Si + \frac{n}{2}H_2O_2 + 6HF \rightarrow H_2SiF_6 + nH_2O + \frac{4-n}{2}H_2\uparrow$$

[0065] The etch rate and resulting morphology of this process depends on dopant type, concentration, catalyst film thickness and etchant concentrations. Both electric and magnetic fields have been used to achieve greater uniformity/control of porosity due to diffusion of holes during the etch process. The resulting substrate with the catalyst mesh is placed in an etchant solution and etched precisely to a certain depth actively controlled by electrical fields, temperature gradients and optical imaging systems that can determine the etch depth in situ. After CICE, the catalyst can be removed using chemical or plasma etching, such as with aqua regia, chlorine-based plasmas, etc.

[0066] Diamond-shaped cross-section silicon nanowires made using Jet and Flash Imprint Lithography (J-FIL) and CICE with gold catalyst have been successfully demonstrated (see, e.g., Fig. 1). Capacitors made with diamond shaped silicon nanowires show a 90% higher specific capacitance than NWs with circular cross section of same pitch, and highest specific capacitance per area of NWs in literature. J-FIL and CICE have the potential to fabricate Si nanostructures at fabrication costs of <$1/wafer based on standard cost models.

[0067] Fig. 1A illustrates a J-FIL enabled catalyst influenced chemical etching (CICE) process 100 for making nanowires according to one or more embodiments of the present technology. As illustrated in Figs. 1A-1B, in process step 110, nano-features 111 (e.g., resist material) can be imprinted on silicon substrate 112. The material (e.g., resist) may remain in the trenches 113 after the imprint process. In process step 120, "descum" etching can be performed to remove the resist residual layer thickness (RLT) as well as remove the resist in the trenches 113. One example of a descum etch uses oxygen and argon plasma to etch the resist material. In process step 130, gold (Au) 131 can be deposited in trenches 113 and on top of nano features 111 using a directional deposition process such as electron beam evaporation. An adhesion layer such as Ti may also be deposited prior to deposition of Gold. In process step 140, CICE can be used to form trenches 141, where gold 131 is located at the bottom of trenches 141 and on top of nano features 111. In process step 150, gold (Au) 131 and resist 111 can be removed and the structure can be cleaned using plasma etching or chemical etchants such as aqua regia, potassium iodide, and piranha in liquid or vapor form. Fig. 1B depicts the cross-sectional views

of fabricating nanowires using the steps described in Fig. 1A in accordance with one or more embodiments of the present technology.

[0068] CICE is a superset of a process called Metal Assisted Chemical Etching (MACE). Apart from metals, there are certain non-metallic catalysts such as Graphene or TiN, TaN, RuO_2, IrO_2 etc. that can also be potentially be used as catalysts. Further, while the catalysts usually locally assist in the chemical etching by digging into the substrate in the presence of etchants and oxidants, they can also locally inhibit the etch, as in the case of InP. To encompass all such processes, various embodiments refer to the process Catalyst Influenced Chemical Etching (CICE).

[0069] However, the CICE anisotropic wet etch method used in the high aspect ratio etch steps does not currently have precise etch depth control and wafer scale fabrication. Discontinuous catalyst features tend to wander during the CICE process and cause defects. Catalysts used are not easy to etch with plasma or wet etch without re-deposition or undercut. Lift-off process, currently used to pattern noble metal catalyst, has high defectivity. Various embodiments of the present technology enable etching of arbitrary nanopatterns with feature sizes ranging from mm to nm by precisely controlling various sensors and actuators such as the chemistry of the etchant solution, electric field, the optical/ spectral properties of the nanostructures etc.

[0070] In accordance with various embodiments, CICE can be used to create nanostructures of bulk material or alternating layers of material such as superlattices. CICE of bulk material can be used in devices such as finFETs and nanowire sensors. Superlattice nanostructures have applications such as 3D NAND Flash memory devices and nanosheet transistors. Superlattices can be created by performing CICE on bulk semiconducting substrates with time-varying electric fields, or on substrates with alternating layers of semiconducting material differing in doping concentration, material, dopant type, etc. For an embodiment using silicon as at least one of the materials in the substrate, the process of CICE to create superlattices is described as Silicon Superlattice Etching (SiSE), described below.

Silicon Superlattice Etching (SiSE)

[0071] SiSE can be used on bulk silicon wafers as well as alternating layers of silicon with different doping concentrations. An etchant (such as Hydrofluoric acid HF), an oxidant (such as Hydrogen peroxide H_2O_2), and optionally a low surface tension liquid (such as Ethanol) and DI water can etch semiconducting substrates preferentially at the location of a catalyst (such as Ag,

Au, Pd, Pt, Cu, W, Ru, TiN, RuO_2, IrO_2, Graphene, etc.). Non-aqueous etchants can also be used if needed. Lithography techniques (such as photolithography, electron beam lithography, double patterning, quad patterning, nanoimprint- lithography etc.) can be used to define the catalyst features. The resulting substrate with the catalyst mesh is placed in the MSP-CICE tool and etched precisely to a certain depth actively controlled by electrical fields, thermal actuators and optical imaging systems that can determine the etch depth based on the electrical and optical properties during etch.

[0072] Other semiconductors such as IVs, II-VIs, III-Vs, alloys and heterojunction materials that can be etched with superlattice etching are Ge, $SixGe_{1-x}$, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC, and the like. They can also be included in the material design space but are not further discussed herein for various reasons such as high cost of material and deposition, lack of commercially available methods of deposition and characterization, etc. Various embodiments of the SiSE process containing silicon can be utilized. Reliable and large area wafer scale etching with SiSE process is currently not present in traditional technologies. Various embodiments shall incorporate various technologies to enable this.

[0073] Silicon superlattice etching (SiSE) uses the catalyst to etch a semiconducting substrate while simultaneously creating a superlattice with alternating layers where at least one of the layers is porous. The alternating layers are formed by electric field parameter modulation and/or etching through layers with alternating doping characteristics. Fig. 2 illustrates a SiSE process control 200 according to one or more embodiments of the present technology. As illustrated in Fig. 2, patterning operation 210 can generate a patterned catalyst on the silicon substrate. In accordance with various embodiments, a bulk substrate (as illustrated in 212) may be used or a substrate with alternating doping layers (as illustrated in 214) may be used. Either the bulk substrate or the substrate with alternating doping layers may be loaded into a silicon superlattice etch tool in loading operation 230. The SiSE process 240 can be precisely controlled to generate high-aspect ratio nanostructures 250. In accordance with various embodiments, the high-aspect ratio nanostructures 250 may have a ratio of height to critical dimension (e.g., average of the diameter of the base and the top for nanowire) of 4:1, 5:1, or more.

[0074] Various feedback parameters 260 can be directly measured directly or estimated from direct measurements. These parameters can include, but are not limited to etchant performance parameters (e.g., concentration, volume, flow rate, Reynolds number, refractive index, etc.), electric field parameters, (current, voltage, resistance, capacitance, etc.), optical variations across the whole wafer (e.g., reflectance, intensity, etc.), ambient environmental

parameters (e.g., temperature, pressure, inert gas flow rate, vapor pressures, etc.), and/or other parameters. These can be used to generate a feedback signal which can be used in conjunction with an input etch control signal to control various system parameters (e.g., flow rates, etchant turbulence, temperature, pressure, concentrations, illuminations, electric field parameters such as current, voltage, resistance, capacitance, frequency, duty cycle, amplitude, waveform type, distance between electrodes, and the like).

[0075] In the case of bulk silicon (as illustrated in 212) that is etched by the patterned catalyst along with a modulated electric field, the alternating layers differ in porosity. Modulation in parameters such as current density and illumination density with time can create porous semiconductor multilayers. The current density can be modulated such that, for a p-type silicon substrate, a positive current density causes porosity as the catalyst sinks into the silicon, and a zero or negative current density gives crystalline layers with only the catalyst etch, as shown in Fig. 2. This is unique compared to processes where only modulated electric field is used without the presence of a catalyst, since such cases cannot produce alternating layers where the porosity of one of the alternating layers is very low. Some embodiments of such a multilayer stack can include one set of alternating layers with a porosity of less than 20% and another set comprising layer with a porosity greater than 30%.

[0076] When epitaxial layers with alternate high and low doping concentrations are deposited at sub-micron thickness per layer (e.g., as illustrated in 214), the concentration gradient across the interface of the two layers is shallow due to limitations of the deposition process at high deposition rates, as well as due to diffusion of dopants across the interface. This gives a non-abrupt change of doping across the thickness of the stack, such as a shallow gradient across the interface. With SiSE, the etch is tuned to ensure that the morphology changes from porous to non-porous at a specific doping concentration, thereby changing the shallow doping concentration gradient into an abrupt step function of porous/non-porous interfaces.

[0077] As SiSE progresses, the catalyst mesh etches the semiconductor material stack to reveal high aspect ratio features with holes and slits for 3D NAND channels and word line separation, and fins and trenches for nanosheet FETs. SiSE can be stopped by using an etch stop layer and/or a timed etch. The etchant composition as well as hole-generation during the process results in alternating films of differing morphologies based on their material and doping concentrations. Also, the exact time at which the morphology changes can be detected by measuring electrical parameters such as resistance, voltage, current, capacitance, and the like.

across the epitaxial layers. This information can then be used to precisely modulate the current across the stack.

[0078] Figs. 3A-3B show the steep interface between porous and non-porous layers after SiSE on a substrate with alternating layers of epitaxial silicon with different doping concentrations according to one or more embodiments of the present technology. In Fig. 3A, interface 310 between layer A of porous film 320 and layer B of non-porous film 330 can be seen. In Fig. 3B several collapsing walls 340 with porous and non-porous sections can be seen.

CMOS Compatibility of Catalyst material for CICE

[0079] Various embodiments of the CICE process can use a patterned catalyst that sinks into the substrate as the etch progresses, leaving behind un-patterned areas as high aspect ratio nanostructures. For semiconductor applications such as in transistors and memory devices, the catalyst material should be CMOS-compatible to enable adoption by industry and to prevent deep-level defects in silicon. Materials such as Au, Ag, Pt, Cu, Pd, W, Ni, Ru, Graphene, TiN, RuO_2 can be used as SiSE catalysts. The deep-level defects appear when metals such as Au and Cu are processed at high temperature. As SiSE is a room- to low-temperature process, the effect of such defects might be minimal. Further, CMOS compatible catalysts such as Pt, Pd, Ru, TiN etc. can be used.

[0080] Fig. 4 shows an SEM cross-section of silicon nanowires created with gold and platinum catalysts, and zoomed in images of the catalyst meshes at the bottom of the nanostructures, according to one or more embodiments of the present technology. For a CMOS compatible catalyst like platinum (Fig.4), the deposition and patterning must have high yield. Platinum can be etched using plasma etching with Cl_2 to form $PtCl_2$. At temperatures above 210C, $PtCl_2$ is volatile, and thus can be used as a viable method of etching the metal after deposition and lithography. Similar etch methods can be used for Palladium. Another method of deposition is via electrodeposition after lithography, where the metal is deposited only in areas of the substrate that are not covered by resist. Alternatively, the metal is deposited on top of the lithographed areas and the substrate, such as by electron beam deposition, but only the areas in contact with the substrate are etched by MACE, without requiring liftoff.

[0081] To prevent wandering of the catalyst mesh and for reliable transport of etchant solution: electric fields, ceilings and/or continuous patterns with connecting links can be used in various embodiments. The resulting high aspect ratio features can be prevented from collapse by mitigation techniques such as using low surface tension gradients, super critical drying and

connected features. Wandering and collapse can also be prevented by using a patterning technique comprising of connecting links between desired features of both catalyst and substrate, and by using controlled deposition or etch after the SiSE process to convert the high aspect ratio linked features into the desired device structure.

[0082] A problem that arises during high aspect ratio etching of disconnected features is that of collapse. This is extremely detrimental to yield of the device. Various embodiments solve this problem by creating an interconnected nanostructure with sub-10nm assist features that can prevent collapse and provide stability to the structures during and after etching. For instance, in Figs. 5A-5B, a catalyst design for 3D NAND Flash is shown. After SiSE, the resulting structures may be >20 microns height with sub-40nm feature size.

[0083] Fig. 5A shows how connecting links 510 in the catalyst material as well as the semiconductor structures can be used to connect various isolated catalysts 520 and High Aspect Ratio (HAR) nanostructures 540 simultaneously according to one or more embodiments of the present technology. Fig. 5B provides a top view illustrating disconnected regions representing the geometry of the catalyst features 530 and connected regions 540 that define the high aspect ratio structures that remain after SiSE according to one or more embodiments of the present technology. In accordance with various embodiments, isolated catalyst portions can be connected using a pattern that can be generated from an algorithm used for connecting isolated features using links to ensure that the HAR nanostructures stay standing, and also helps prevent wandering of the catalyst mesh and creates pathways for diffusion of etchant reactants and products to ensure uniform and controlled etch rates. (Fig. 5A) Since the catalyst features are disconnected, wandering can occur, but may be prevented in some embodiments using electric fields. The free standing features are connected to prevent collapse by buttressing the high aspect ratio lines (Fig. 5B).

[0084] In accordance with various embodiments, connected link generation can be done by defining nodes of catalyst material or semiconductor that would be isolated in an ideal intended design. The links can be then generated to ensure that the structures etched by CICE are mechanically stable. The links can also be optimized to ensure that the catalyst does not wander during CICE. Optimizing for such process excursions in the design of the catalyst can be done using standard algorithms such as graph theory based and recursive division methods.

[0085] The catalyst can include one or more of the following: a) lithographic links to prevent wandering – these features result in gaps in the etched structures, which can be filled with material using various deposition processes such as atomic layer deposition, chemical vapor deposition,

electroplating, etc.; and/or b) lithographic gaps to prevent collapse of the etched structures – these features result in stabilizing links in the etched structures. Based on the design requirements, these links may be removed using lithography and etching, selective oxidation, selective oxidation and etching, etc. This can be done after deposition of stabilizing material in other areas as needed.

[0086] If the catalyst mesh comprises both lithographic links and gaps, then a linked structure results. Fabrication of sub-30nm features with even smaller link connections is extremely challenging. Patterning methods such as electron beam lithography can write sub-10nm features but suffers from large overlay, whereas photolithography has superior overlay but poor resolution. Photolithography and imprint lithography (whose template is made with electron beam lithography) may be used to get the final linked structure that can then be made into a nanoimprint template. Examples of such patterns are described in the 3D NAND and transistor device sections.

[0087] Apart from using isolated or linked structures for catalysts, another method to extend the maximum aspect ratio that may be used by various embodiments is by using ceilings. Collapse prevention using a ceiling can be done by etching the features with plasma etching or SiSE to a short, stable height; depositing the ceiling, and continuing the SiSE process. The "ceiling" can also be at a height that is along the length of the short pillars, such as at L/2, where L is the height of the short stable pillar. This gives additional support as the features are further etched and extends the maximum aspect ratio to greater than that with the ceiling on top of the short pillars. This gives structural stability to the high aspect ratio pillars and prevents collapse.

[0088] The ceiling can be deposited by angled deposition; polymer fill, etch back and ceiling deposition; or methods such as spin coating. Materials that can be used for the ceiling include polymers, sputtered/deposited semiconductors, metals and oxides that do not react with the CICE etchants. For Si CICE etchants, materials such as Cr, Cr_2O_3, carbon, silicon, Al_2O_3, polymers, etc. can be used. In some embodiments, the ceiling can also be made porous by an additional low resolution lithography step or by a reaction to induce porosity to the ceiling material. Once the substrate is etched and the catalyst is removed using a liquid or vapor chemical etch, deposition of memory film or dielectric filler by methods like atomic layer deposition can be done before removal of the porous ceiling. The ceiling material could also to tuned to be non-selective to Atomic Layer Deposition (ALD) thereby preventing the pores from closing and blocking the deposition pathways. After filling the features, the ceiling is etched or polished away. ALD can also be used to close off high-aspect ratio shapes after etch to create deep holes without the use of isolated catalysts.

Etch Tool

[0089] Various embodiments of the present technology provide for a unique, high-fidelity nanoscale manufacturing system (Multi-scale Precision CICE or MSP-CICE) that can achieve wafer-scale etching of high aspect ratio nanostructures in semiconducting materials with features such as: 1) high-speed (real-time), high spatial resolution functional or geometric metrology as the etch progresses for precision process monitoring and control; and/or 2) a system that enables multi-scale precision control of the CICE process based on real-time metrology, and based on an array of independently addressable actuators that can locally control the etch process to allow controlled fabrication of devices with diverse arrays.

[0090] Figs. 6A-6E illustrates process chamber configurations for CICE according to one or more embodiments of the present technology. Fig. 6A shows a system with inkjets 605, etchant circulation system 610, front-side electrodes 615, electric field supply 620, polymer walls 625, and backside electrode contacts and thermal actuators 630. In the embodiments illustrated in Fig. 6A, silicon wafer 635 can be positioned between front-side electrodes 615 and back-side electrodes 630 to allow for electric field control. Fig. 6B illustrates some embodiments of the electric field configurations for CICE with the use of wafer chuck 640. Fig. 6C shows a setup for bulk delivery of etchants with backside contact of local electrical and thermal actuators, and micromirror arrays for additional thermal control that may be used in some embodiments of the present technology. Fig. 6D shows a setup for bulk delivery of etchants with frond side electrode needles 645, backside contact of local electrical and thermal actuators, micromirror arrays for additional thermal control that may be used in some embodiments of the present technology. Fig. 6E illustrates a setup with a thermal chuck and embedded electrodes and thermal actuators 650 on the back of the substrate.

[0091] The embodiments illustrated in Fig. 6A and 6B use inkjets 605 coupled with local top electrodes 615 and backside electrode contacts 630 to provide local control of etchant concentrations and electric fields. The different regions for etching can be isolated from each other on the top of the wafer using polymer walls 625 that are patterned using low resolution lithography. In one embodiment, the walls can be made of a different etchant resistant material such as silicon nitride, aluminum oxide, amorphous carbon, silicon or chromium. In Fig. 6A, the backside electrode 630 includes both electric and thermal actuators, and the electric contact is made using conductive substances such as metal, silicon, silicon carbide etc. which may or may not be doped to improve conductance. In Fig. 6B, the backside electric contact 630 is made using an electrolyte which is locally contained between the wafer 635 and the chuck 640. The electrolyte

may be the same as the etchant or is a different conductive liquid such as dilute acids, bases or salts which are CMOS compatible. In both Fig. 6A and 6B, the backside electrode 630 can also include temperature control integrated in the electrode itself (Fig. 6A) or in the chuck (Fig. 6B).

[0092] In the embodiments illustrated in Fig. 6C, the backside electrode contact 630 and the chuck 640 are similar to the configuration in Fig. 6B. The etchant, on the other hand, is dispensed globally on the wafer using and inlet, and may be circulated using an outlet for flow control. An optional diffuser (not shown) may be used to ensure uniform distribution of etchant over the wafer. The different components of the etchant may be mixed in a separate mixing chamber or dynamically mixed in by flowing through the inlet and diffuser. Electrode 615 can be made of a metal mesh, doped silicon wafer, ITO (Indium Tin Oxide) or other such materials and can be coated with etchant resistant material such as polymer, PTFE, aluminum oxide, and the like, and the coated material can be doped to improve conductivity. Local heating can be implemented on either side of the wafer, either by a micromirror array on the topside of the wafer or by embedded thermal actuators in the chuck 640.

[0093] In the embodiments illustrated in Fig. 6D, the wafer 635 can face either top or bottom of the setup. The chuck 640 can be used to create an electric field using an electrode and an electrolyte. The electrolyte can be a very thin film, thereby enabling local temperature control via embedded actuators in chuck 640. Alternatively, micromirrors can be used. An optional diffuser (not shown in Fig. 6D) can be used for both distributing the etchant uniformly and for optical metrology using embedded optical fibers. Local electric field control can be created via sharp electrode tips 645 or by embedded electrodes in the chuck 640.

[0094] Fig. 6E shows an embodiment where the wafer 635 faces the base of the setup. The base comprises an electrode and an etchant at low temperatures. The wafer can be held upside down using a head chuck that comprises electrical and thermal actuators. A thin film of electrolyte may also be present in the head chuck for better electrical contact. The wafer can be spun using the head chuck, and a overflow chamber can be used for transport of excess etchant while spinning the wafer. An optional diffuser (not shown in figure) can be used in the base to enable uniform distribution of the etchant. The diffuser can also include optic cables for metrology.

[0095] CICE can be performed using various methods of etchant delivery in conjunction with catalysts and electric, magnetic, temperature actuators, and the like for different applications, such as: electrochemical etching, electroless chemical etching, catalyst influenced vapor etching, catalyst influenced plasma etching, “digital” layer electrochemical/electroless chemical etching (e.g., alternately pulse H_2O_2 vapor and HF vapor, alternately pulse H_2O_2 liquid and HF liquid,

alternately pulse H_2O_2 vapor and HF liquid, alternately pulse H_2O_2 vapor and HF liquid, H_2O_2, Plasma and fluoride ion flow/pressure alternated for alternating porosities, using stronger oxidant for porous layers and weaker oxidant for non-porous layers, etc.), magnetic field electrochemical/electroless chemical etching, gel-based etching (e.g., by adding a thick polymeric substance and bringing into local contact on top/bottom of wafer for local thermal control and electric field control or changing gel consistency with temperature), and the like.

[0096] In some embodiments, prior to the CICE process, the wetting properties of the etchant chemicals on the catalyst patterned substrate can be modified to make it more hydrophobic or hydrophilic. This helps improve the uniformity of the etch process by ensuring that the initiation of the etch starts in all locations of the substrate at the same time. Exposing the substrate to vapor HF, Piranha (sulfuric acid and hydrogen peroxide in different ratios), buffered oxide etch, hydrofluoric acid, etc.; rinsing it with DI water, isopropyl alcohol, acetone, etc., and then drying it to prevent water stains can improve wetting of the etchant on the substrate.

[0097] After the CICE process is completed, the substrate can be rinsed in DI water, isopropyl alcohol, acetone, etc. to ensure that the etchant is completely removed from the substrate, thereby avoiding any extraneous etching locally. A rinsing station can be the same as the process chamber, where the wafer is flushed with DI water after removal of the etchant. It can also comprise a spinning system to dry the wafer after rinsing. Alternatively, the wafer can be moved to a separate rinsing and drying station after the CICE process using automated handling.

[0098] Fig. 7A illustrates the cross-section of an embodiment of MSP-CICE process chamber 700 with automated handling using a Z-motion actuator 710. The Z-motion actuator may comprise voice coils in the head assembly, bearings 715 in the base assembly, and a compliance in the actuator system to ensure creation of a good seal to prevent leaks using sensors for leak checks 720. This Z-motion actuator is used to lower the head assembly 725 towards the base assembly 730. The Z-motion actuator may be controlled using motion sensors, force sensors, or a combination thereof to ensure the head assembly, the wafer, and the base assembly can be assembled to form the appropriate seals required for the electrolyte in the head assembly and the etchant in the base assembly. In this embodiment, the Si wafer substrate 735 faces the base.

[0099] The base comprises a base electrode 740, power supply 745 to the base electrode, sealing rings 750 which could be an O-ring (circular cross-section polymeric ring) or a rectangular cross-section ring made of etchant resistant materials such as fluoropolymer, Al_2O_3, SiC, Teflon-

coated material etc. that are used to seal the etchant from the electrode and the Si wafer. The base also comprises inlets 755 and outlets 760 for etchant flow and circulation, and a diffuser 765 that may comprise optic fibers for optical sensing of the etch process in-situ. The base may also comprise an overflow chamber (not depicted in figure) to ensure the etchant is filled to the brim before loading of the Si wafer. The head assembly comprises pin chuck zones 770, electrolyte zones 785 and power supply 795. The pin chuck zones are connected to one or more vacuum ports 775.

[00100] Thermal actuators 780 can be embedded behind the pin chuck zones. An embodiment that uses thermal actuators comprising proportional-integral controlled thermoelectric heating/cooling elements such as thermistors and heat sinks is incorporated herein by reference. (Ajay, P. et al., 2016. Multifield sub-5 nm overlay in imprint lithography. *Journal of vacuum science and technology. B, Nanotechnology & microelectronics: materials, processing, measurement, & phenomena: JVST B*, 34(6), p.061605.) An electrolyte port 790 for both inlet and outlet is used to pump in electrolyte into one or more electrolyte zones and seal it during the etch. This can enable a configuration where the head assembly along with the Si wafer can spin while the base remains stationary. The electrolyte may be different from the etchant, such as dilute acids, bases and salts with sufficient conductivity to create an electric field across the Si wafer with the base electrode. An exemplar electrolyte comprises dilute sulphuric acid.

[00101] Fig. 7B shows a cross-sectional view and a top view of an embodiment of the head chuck. The pin chuck zones 770 are used to hold the Si wafer 735, and the electrolyte zones 785 are used to create contact between the Si wafer and the electrolyte. A liquid electrolyte is used in this embodiment to create reliable ohmic contacts with the Si wafer. In other embodiments, metal or SiC pads may be used instead of liquid electrolytes in the “electrolyte zones”. The pin chuck and electrolyte zones are separated from one other using sealing elements 771 machined into the chuck. Local electric field boundaries at the edges of the electrolyte zones are discrete at the back of the Si wafer . However, due to the thickness of the Si wafer and its electronic properties, the electric fields lines between different electrolyte zones may merge at the front of the Si wafer.

[00102] Electromagnetic simulations can be done to determine optimal placement of electrolyte zones and pin chuck zones for effective local and global electric field control and edge uniformity. In one embodiment, the sealing elements are 1mm wide and the pin chuck and electrolyte zones are concentric, with a width of 9mm each, ending with a circular region in the middle as shown in Fig. 7B. Vacuum ports 775 may use pneumatic elements to ensure that the

pin chuck zones are under vacuum, and the wafer is held against the pins 772. Electrolyte flow ports 790 are used to flow in electrolyte after the Si wafer is held by the chuck. Discrete thermal actuators 780 can be integrated behind the pin chuck regions of the Si wafer to facilitate local temperature control. In one embodiment, the head assembly comprises pin chuck elements made with aluminum oxide material.

[00103] In Fig. 7, automated handling can be achieved by starting with a separation between the head and base. The base is stationary and is filled to the brim with etchant, and this can be ensured by using an overflow chamber and etchant level monitors. The etchant in the base can be recirculated using the inlet and outlet valves. A robotic arm is used to load the Si wafer onto the head chuck with the surface to be etched facing the base. In one embodiment, the robotic arm contacts the front of Si wafer at the edge (only in the exclusion zone which is ~1-2mm zone at the edge of the wafer, where there are no functional devices fabricated) and aligns the back of the wafer to the outer sealing ring of the head chuck, which then holds the Si wafer using vacuum in the pin chuck zones. In an alternate embodiment, the head chuck may include "fingers" around the edge of the wafer that protrude out and hold onto the edge of the wafer after the robotic arm holding the wafer facing the base brings the wafer underneath the head chuck. The fingers hold onto the edge of the wafer and then pull the wafer towards the pins in the head chuck. The vacuum zones then hold onto the wafer, which can be detected using vacuum sensors in the chuck vacuum lines. The fingers then retract into the head away from the edge of the wafer.

[00104] Once a seal is created, electrolyte is pumped into the one or more electrolyte zones. This portion may be thin to ensure low volumes of electrolyte need to be pumped in. The head assembly along with the Si wafer is then lowered using a Z-motion actuator towards the base. To ensure smooth contact with the etchant in the base and to minimize bubble formation at the etchant-wafer interface, the head assembly is tilted slightly as it is lowered using elements in the z-motion actuator such as voice coils. Once it makes contact with the etchant at one end, the head assembly is tilted back to a horizontal configuration. This ensures that there is no trapping of air bubbles at the interface of the wafer and the base. An optional bearing in the base then clamps the assemblies together and uses force sensors to check whether an adequate seal has been created between the base and the Si wafer.

[00105] Alternatively, any excess etchant may flow into the overflow chamber near the edge of the wafer. Sensors for leak tests then ensure that the wafer is ready to be processed. CICE may be performed by starting an electric field across the wafer. In processes requiring an oxidant such as H_2O_2, the oxidant may be pumped into the etchant at the base after the wafer is clamped

to make sure that any initial contact does not prematurely start the etch. In an alternate embodiment, the volume of the etchant in the base is slightly less than the amount required to contact the front of the Si wafer. Once the head assembly has completed its z-motion towards the base, a small amount of etchant is added to the base chamber to bring the etchant into contact with the Si wafer. To prevent air bubbles from affecting the etch, the head may be tilted slightly to let the air bubbles escape and then brought back to horizontal position, thereby creating a uniform etchant-wafer interface for CICE.

[00106] Unloading of the wafer after the CICE process in Fig. 7 may also be handled in an automated fashion. Once the CICE process is completed, the head assembly including the wafer is separated from the base. The etched side of the wafer is then rinsed to remove any etchant on the surface. This can be done by spinning the head and spraying DI water, wherein a rinsing system is moved into the area below the head and above the base. The rinsing system comprises a drain, a spray for DI water and a source for heated air or nitrogen gas to dry the etched surface. Once the front surface of the Si wafer is clean, the electrolyte in the head is drained and the wafer is placed face down on an edge contact on the rinsing station. The back of the wafer is then rinsed and dried in a similar fashion. A robotic arm then unloads the Si wafer and the rinsing system is moved away from the middle of the head and base. In an alternate embodiment, the head may move laterally and place the Si wafer on a separate rinsing station.

[00107] Wafer-scale etching of semiconductor bulk or superlattice nanostructures using CICE can use monitoring and control of various parameters such as the etch depth variation, porosity of the alternating layers, stability of the high aspect ratio nanostructures, anisotropy of the etch, wafer edge effects, electric field uniformity, illumination uniformity, etc. This can enable monitoring of etch parameters layer by layer during SiSE. This can use local control of pattern geometries and a measurement of electric current and voltage across the stack to determine number of layers etched etc. to high levels of precision over the entire wafer.

[00108] Additionally, the areas of the wafer that are used for peripheral circuitry and non-3D NAND array circuits must be protected from the SiSE process. This can be done by masking the non-array areas. Etch variation near the edges of these features can be regulated using actuators.

[00109] The flow of etchants through a sub-40nm hole as it etches to depths >10 microns (A.R >250) is enabled by electric fields and by creation of alternating porous layers. The porous layers enhance lateral etchant flow and regulate the etch uniformity. Another way to boost etchant flow, in accordance with various embodiments, is by using a connected link pattern to connect the holes.

[00110] The etch rate may decrease due to slower diffusion of etchants as the etch progresses due to increase in aspect ratio. Such changes can be detected through a change in the electrical properties across the stack, as each etched layer of the superlattice can result in a step change in the electrical property such as current or voltage across the electrodes or the resistance of the stack. To prevent this decrease in diffusion, some embodiments utilize the alternating porous layers to ensure that there are multiple pathways for the etchant to reach the etch front, i.e., the catalyst location. Spinning the substrate during the CICE process can be done in some embodiments at optimized speeds to improve uniformity of the etchant concentrations from the center of the wafer to the edge.

[00111] Wandering of the catalyst is primarily due to an imbalance in the concentration of holes underneath the catalyst. To prevent wandering of the catalyst and to ensure vertical anisotropy of the etch, an electric field can be applied to direct the diffusion of holes towards the bottom of the wafer. The electric field required changes as SiSE progresses due to a change in the resistivity across the electrodes with change in the number of alternating doped layers to be etched. By using a current control power supply circuit, the changes in voltage can be compensated for.

[00112] Various embodiments of the SiSE tool system enable multi-scale precision control of the SiSE process based on real-time metrology, and based on an array of independently addressable actuators that can locally control the etch process to allow controlled fabrication of devices with diverse geometries and multilayers. Parameters like the resistivity and doping of the substrate material, geometry and aspect ratio required, the etchant ratios, electric-field, temperature and illumination of the process chamber can be modified to control etch. Once the SiSE process is complete as detected by inline metrology, the solution in the machine has to be flushed out and replaced with a wet etchant for the catalyst. Next, since the high aspect ratio nanostructures can collapse due to capillary forces as the device is being dried, use of efficient and highly controlled fluid exchange coupled with advanced drying techniques and novel mesh architectures and/or ceilings to prevent pattern collapse is described.

[00113] Inline electrical metrology and electrochemical etch stops may be used in various embodiments. For example, an electric bias when applied to a semiconductor substrate can control the etching profile in real-time. Excessive etching due to migration of excess holes generated below the catalyst can be controlled by an external electric field. A negative bias on the backside of the wafer will attract the excess holes and prevent unwanted pores in the Si. A wide range of current, bias and polarity settings including high speed pulse and periodic reverse

waveforms will control the electric field across the wafer in real-time. Electric field parameters such as current, voltage, resistance, capacitance, waveform frequency, duty cycle, amplitude, distance between electrodes etc. are used both to detect changes in the etch state as well as control the porosities of the alternating layers while preventing wandering of the catalysts.

[00114] Measurement of the current and voltage across the substrate as the etch progresses can be used to determine the number of alternating layers etched in the 3D NAND Flash process. Also, the exact time at which the morphology changes can be detected by measuring electrical parameters such as resistance, voltage, current, capacitance etc. across the epitaxial layers. This information can then be used to precisely modulate the current across the stack.

[00115] Electric fields can be used for various functions during the CICE process such as for making alternating porous/non-porous layers, preventing wandering of the catalyst during etch, maintaining uniformity across the wafer and detecting etch depth variations in a die, die-to-die variations, and center-to-edge variations. Applying electric fields across the substrate, both locally and globally, requires designing the tool and process to ensure compatibility with different CMOS processing equipment and constraints such as front and back contact, edge width contact, electric back contact materials etc. Some embodiments of this design are shown in Figs. 6A-6E.

[00116] To perform multiple functions, more than one electric field can be applied across the wafer, such as: 1) DC voltage across the wafer to prevent wandering of the catalyst; 2) alternating electric fields with a certain waveform, frequency, wavelength and duty cycle to create alternating porous/non-porous layers; 3) detection of local variations of etch from center to edge via pulsed electric fields at frequencies and voltages that do not affect the porosity of the substrate being etched; and/or 4) etch depth monitoring by measurement of current, voltage, resistance, capacitance etc. in each local electrode.

[00117] Apart from Electric Fields, temperature can also influence the CICE etch rates. For instance, it has been demonstrated in literature that the etch rates of CICE depend on the temperature of the etchant, and drop off exponentially near 0^0C. (Ref: Backes, A. et al., 2016. Temperature Dependent Pore Formation in Metal Assisted Chemical Etching of Silicon. *ECS Journal of Solid State Science and Technology*, 5(12), pp. 653–P656 is hereby incorporated by reference in its entirety for all purposes.) Various embodiments take advantage of this property by locally controlling the etch temperature by maintaining the global etchant temperature near zero degrees using coolants such as liquid nitrogen and dry ice, and locally modifying the temperature of the substrate. This can be done using thermal chucks, micromirrors or electrodes near the wafer that can locally heat the solution. Alternatively, etchant temperatures can be

controlled locally by using individual wells for each die which are filled with finite and temperature controlled etchant volume and are pumped out or circulated. In some embodiments, the temperature can be mapped with precision across the wafer using thermal cameras, thermocouples, and the like.

[00118] An optical imaging system will be used to measure the reflectance over large sample areas in real-time. The samples will be illuminated with light with known spectral content. The light can be white light, colored light, single wavelength, in a narrow or wide spectral band, etc. A camera can then image the samples reflecting this light. The camera may be monochrome, color (RGB), multi-spectral, hyperspectral, etc. Multi-megapixel resolutions found in modern cameras make it possible to observe millions of points on a sample simultaneously. Video framerates enable in-situ real-time measurement. Each image can be divided by an image of a reference to calculate reflectance images of the samples or used as they are. An image processing algorithm will determine process completion and gather data about uniformity of MSP-CICE both within samples and sample to sample. In an embodiment where CICE is used to create Si nanowires (NWs), the optical properties of Si NWs of variable geometries lead to a wide spectrum of colors under white light illumination. In our preliminary experiments with CICE, samples exhibit profound changes in hue during the CICE etch. Since the pitch and diameter of the nanowires remain relatively fixed, observing changes in the hue of samples is a useful indicator of the height of the nanowires, and thus the etch depth. Changes in hue can be characterized by measuring the reflectance of the sample as a function of the spectral content of the light being.

[00119] The spectral properties of the alternating layers can also be used to enable detection of number of layers and porosity during the etch process. Infrared (IR) spectroscopy can be used to determine the etch layers in-situ, using metrology similar to that used to characterize Bragg reflectors and Rugate filters in literature. In one embodiment, optic cables in a diffuser plate in the etch chamber can be used to incorporate such metrology elements.

[00120] Visible wavelengths of light from the backside of the wafer cannot detect the etch depth during CICE. Infrared (IR) spectroscopy can be used instead, as is it a rapid, non-destructive and in-situ method of etch state detection. Silicon is transparent in IR wavelengths, while a catalyst such as Pt or Pd is not. This differentiation can be used to determine both the etch rate and the etch depth at any particular instance of the CICE process.

[00121] The concentration of the etchant can be measured using a variety of techniques. For example, in some embodiments, a conductivity measurement may be used since the HF has a linear dependence between concentration and conductivity. In some embodiments, a refractive

index measurement may be used. For example, an optical metrology system can be used to measure the refractive index (RI) via a reflection-type geometry using an optical window in contact with the solution, thus avoiding turbidity, diffraction and absorption.

[00122] To ensure etchant concentration uniformity across the wafer, the wafer can be spun using a wafer chuck, wherein local electric fields can be provided by connecting the spinning arrays of local electrodes on the chuck to a stationary patterned conductor disc. The local electrodes can be connected to the stationary patterned conductor disc using slip rings. Compatibility with the etchant chemicals can be ensured by using Teflon coating.

[00123] In some embodiments, a "send-ahead" wafer can be used to optimize the etch, and the send-ahead wafer can be inspected using various in-situ (online) and ex-situ (offline) methods. Offline metrology comprises of various destructive and non-destructive inspection methods such as scatterometry, ellipsometry, optical feature size measurement, laser scanning, Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), Transmission electron microscopy (TEM), x-ray diffraction (XRD), etc. The data collected is then analyzed using image processing algorithms to determine sources of defects and process excursions.

[00124] Magnetic fields, pressure variations, electromagnetic fields, solvents to improve uniformity and prevent sticking of bubbles, spinning of the wafer, edge effects, spraying of etchants, atomizing etchants can also be included in some embodiments of the CICE tool as necessary.

Overall tool designs and control schemes

[00125] Some embodiments provide for a wafer-scale system for high aspect ratio etching of semiconductor substrates. The multi-scale precision (MSP) CICE system used in some embodiments can have a modular architecture to allow for installation of sensors and actuators such as a large array electrodes and real-time optical imaging systems. Figs. 8A-8C illustrate and example of an MSP-CICE tool setup, an example of a detailed process chamber layout, and an example of a process flow that may be used in one or more embodiments. Nonlinear optimal process control schemes can be used in some embodiments to achieve controlled wafer scale nano-manufacturing based on large array of independently controlled electrodes.

[00126] Fig. 8A shows a cross-sectional view of a complete etching tool, with automated substrate, electrode and etch cell loading. Fig. 8B shows a detailed cross-sectional view of some embodiments of the process chamber 815. As illustrated in Fig. 8B, the etching tool can include loading dock 805, robotic arm 810, process chamber 815, top electrode 820, tunable light source

825, wafer chuck 830, wafer chuck holder 835, stirrer 840, power supply 845, sensors 850, drain pipe 855, optical metrology system 860, high resolution camera 865, bottom electrode 870, circulation setup 880, exhaust 885, and inlet flow 890. In the embodiments illustrated, process chamber 815 can include robotic arm 810 that places a wafer on wafer chuck 830. Wafer chuck 830 can sit upon wafer chuck holder 835. The wafer chuck holder and the wafer chuck assembly separate the electrolytes in contact with the bottom electrode 870 and the top electrode 820.This ensures that the electric field is applied across the wafer. Process chamber 815 can also include in-line optical metrology system 860 which can include high resolution camera 865 and tunable light source 825. Process chamber 815, in accordance with various embodiments, can also include an etching flow system with an inlet flow 890, drain pipe 855, and circulation setup 880 for both the bottom electrolyte and the top electrolyte/etchant. The etching flow system may also include stirrer 840 (e.g., a magnetic stirrer). An electric field can be applied across the wafer using first electrode 820 and second electrode 870 with power supply 845. The inline metrology can be done using embedded sensors 850 (e.g., temperature, electric field properties, fluid concentration properties, etc.). Exhaust 885 can be used to dispense of fumes. Processor 890 can use one or more algorithms to control the processing.

[00127] In the embodiments illustrated in Figs. 8A-8B, a wafer with a patterned catalyst will be loaded into the loading dock 805. A robotic arm 810 can be used to transfer the wafer into the process chamber 815. The transparent top electrode 820 can then be placed on the rails above the wafer holder. When the processing is complete, the top electrode array 820 can be removed and the wafer will be unloaded back to the loading dock 805. A key challenge in building this tool is that all the elements of the system be HF (Hydrofluoric Acid)-compatible. Various embodiments propose to do this by coating all equipment that comes in contact with HF with polymers such as Teflon PTFE, Epoxy, TPX (or PMP), polypropylene(PP) and PVDF, which are compatible with H_2O_2 as well. TPX and epoxy are transparent and easy to process.

[00128] Based on the requirements of the application, the wafer chuck can be a Bernoulli chuck with no backside contact with the wafer, or have O-rings to contain the wet etchant to the front of the wafer. Flow valves and actuators can be used to control relative ratios of the etchant components (such as HF, H_2O_2, Ethanol, Isopropyl alcohol and DI water) in the chamber. The etchant can be dispensed locally by inkjets or over the whole wafer by flow valves. After etch and catalyst mesh removal, the etchants will be flushed with DI water, and may be replaced with low surface tension liquids. A drain valve will safely dispose of the fluids or store them for use in a subsequent etch.

[00129] Fig. 8C depicts an example of various processes that the wafer goes through in the etch tool. The wafer can be loaded into the tool using a loading dock 812 which can comprise of the FOUP (Front Opening Universal Pod) of wafers. A robotic arm (or other transport mechanism) can transport the wafer from the loading dock 805 to the process chamber 815. The process chamber 815 may comprise of one or more chambers for pre-processing 816, etching 818, post-processing 828 and rinsing steps 830.

[00130] The pre-processing step 816 may be a lift-off process or a surface modification step such as dispensing of piranha (sulphuric acid and hydrogen peroxide), vapor HF, diluted HF, Buffered Oxide Etch, Ethanol, Acetone, Isopropyl Alcohol, DI water. The pre-processing step may also be via plasma activation using oxidizing plasmas such as oxygen, carbon dioxide plasma, or hydrogenating plasmas such as hydrogen, ammonia plasma. A helium or argon plasma can also be used.

[00131] The etch process 818 can be then done on the wafer, with sensors and actuators for in-situ monitoring and control, such as:

- Flow control 824 can include etchant concentration measurement. In accordance with various embodiments, the concentration of the etchant will be measured using two techniques: a) Conductivity measurement - HF has a linear dependence between concentration and conductivity. b) Refractive Index measurement - An optical metrology system will measure the Refractive Index (RI) via a reflection-type geometry using an optical window in contact with the solution, thus avoiding turbidity, diffraction and absorption.
- Local temperature control 822: The etch rate is dependent on the local temperature and mesh profile. Using a temperature actuator wafer chuck, various embodiments can control the local temperature variations for process control.
- Process chamber environment control (not illustrated in Fig. 8C): The tool will be enclosed and have inert gas flow. Pressure and global temperature will be monitored and controlled. A computer interface will promote operator safety and will be used to monitor the etch using image processing, and to control temperature and electric fields.
- Electric field 826: An electric bias when applied to a semiconductor substrate can control the etching profile in real-time. Excessive etching due to migration of excess holes generated below the catalyst can be controlled by an external electric field. A negative bias on the backside of the wafer will attract the excess holes and prevent unwanted pores

in the Si. Although etch rates decrease with increase in electric bias, higher temperatures can be used to keep them high enough for high throughput. Since MSP-CICE will be used for varying pattern densities and shapes on different areas of the wafer, an electrode array will be used to locally control and attenuate the electric field above different patterns to ensure uniformity in etch. A wide range of current, bias and polarity settings including high speed pulse and periodic reverse waveforms will control the electric field across the wafer in real-time. A transparent top electrode such as ITO film on a glass or sapphire wafer, a doped Si wafer (transparent to IR), a platinum mesh or optic fibers can be used above or below the wafer to allow for optical measurements. The bottom electrode can be an array for local control, and a modular design will be chosen to allow easy installation and investigation of various bottom electrode arrays. The top and bottom electrodes and electrolytes are isolated from each other using the wafer chuck and wafer chuck holder assembly. Cross-talk will be minimized using simulations. Measurement of the current and voltage across the substrate as the etch progresses can be used to determine the number of alternating layers etched in the 3D NAND Flash process or as an etch stop indicator for nanostructure etching, for example if the substrate has a buried epi layer.

- Inline optical metrology 820: An optical imaging system comprising RGB cameras, optical fibers, spectral imaging setups, will be used to measure the reflectance over large sample areas in real-time. An image processing algorithm will determine process completion and gather data about uniformity of MSP-CICE both within samples and sample to sample.

[00132] Post-processing 828 may include etching of the catalyst metal and rinsing and drying of the substrate. In order to prevent collapse of high aspect ratio etched nanostructures, fluid transfer can be used to enable a surface tension gradient (Marangoni-effect), low surface tension fluid transfer or preparation of the wafer for transfer into a critical point drying tool.

[00133] In one embodiment, based on the resistivity and doping of the silicon, and the geometry and aspect ratio required, the etchant ratios can be tuned to get the desired results. Factors such as electric-field, temperature and illumination of the process chamber can also be modified to control etch. Once the CICE process is complete as detected by inline metrology, the solution in the machine has to be flushed out and replaced with a wet etchant for the catalyst. Next, since the high aspect ratio nanowires can collapse due to capillary forces as the device is being dried, use of efficient and highly controlled fluid exchange coupled with advanced drying techniques and novel mesh architectures and/or ceilings to prevent pattern collapse is used.

[00134] Once the MSP-CICE system has been designed and fabricated (including the optical imaging system and electrical parameter measurements), it is necessary to develop optimal control techniques to operate the MSP-CICE system to fabricate wafer-scale device-specific VA-NSs. As discussed earlier, it is important to have the ability to monitor the etch progression over different layers of the 3D NAND Flash stack or the shaped nanowires for DRAM. This requires local control of pattern geometries and a measurement of electric current and voltage across the stack to determine number of layers etched etc. to high levels of precision over the entire wafer.

[00135] A key challenge is that the forward model of the full system – that provides a relationship between control variables and sensed output over the full wafer – is expected to be highly nonlinear making it difficult to obtain comprehensive experimentally validated models due to the complexity of the MSP-CICE system. However, certain aspects of the process can be modeled through established physical models. For example, the control variables, in various embodiments, can include temperature, chemical composition, and electric field, in which the variation of chemical composition can be analytically modeled with the help of equations governing transport. Electric field and temperature control could be distributed over a large array of actuators– consisting of as high as hundreds to thousands of actuators – providing local control over the etching process, and their distribution can also be modeled through physical models.

[00136] However, models establishing their influence on the etching process is less clear. The optical imaging system is expected to provide spectral information with spatial resolution of as high as $1mm^2$ or higher and wavelength resolution of as high as 1nm or better. The optical, thermal and electrical outputs of the system provide a large volume of sensed information which can be used to automatically control the system's process using the control variables mentioned previously. Automatic process control for the MSP-CICE system can be divided into two distinct categories: (i) offline optimization and tuning of process parameters to obtain a targeted output, and (ii) real-time adjustment of process parameters to minimize defects and maximize yield. The latter relies on a process that is well-established and provides large volume of data, and the former relies on optimizing for process parameters in the absence of a large amount of data. In the next paragraph, a scheme is described which enables the optimization of process parameters for establishing a baseline process for a given pattern geometry with the help of in-situ and offline measurements.

[00137] Fig. 9 illustrates a learning algorithm-based controller 900 which can be used to perform the first category of automatic process control in the absence of large amounts of data, i.e., determining optimum process parameters for a targeted output with the help of learning

algorithms that include evolutionary algorithms such as genetic algorithm, neural networks, etc. This scheme relies on both, in-situ electrical and optical feedback, as well as offline measurements such as ellipsometry, CD-SEM, etc. on send-ahead wafers. Because of the presence of this offline component, the cycle time for each experiment with a send-ahead wafer may be too high, thereby requiring that the number of experiments be low or each send-ahead wafer representing a combinatorial set, rather than an individual experiment. This embodiment is further described in the context of genetic algorithms. The first step 910 of the scheme is to define the targeted output and the corresponding objective function for the optimization. Then, an initial "population" 920 is generated. Genetic algorithms rely on the interactions between individuals in a population, where each individual is a set of the control variables or model parameters 925. In one embodiment, each population may be a design of experiments and confined to a single wafer.

[00138] For example, if each wafer consists of 10x10 sq. mm zones that can provide electrical and optical feedback, there can be O(700) such zones on each wafer, thereby providing a population size of as high as 700 in each experiment. In another embodiment, the population size may be kept to a lower number, such as 20, with each individual experiment having 35 copies on the full wafer. Then, this population is used to perform the CICE process 930. Sensors are then used to extract information about the substrate before, during and after CICE as shown in step 940. The sensed information for this scheme can include the output of both inline metrology sensors such as the imaging system as well as offline measurements (e.g., CD-SEM, optical, electrical, etc.) on the wafer (945). The sensed information is then fitted against the desired output or objective function, 950.

[00139] The desired output parameters include the spectral signature of the etched structures, electrical parameters such as resistance and capacitance across the wafer during the etch process, CD-SEM and optical images of one or more portions of the wafer, etc. Based on the objective function calculated using the sensed information, a new batch of control variables is generated, using population interaction parameters (965). CICE is then performed using the new batch and the result is evaluated using sensors. If the sensed information is within the limits of the desired result, then the tuning of control variables is completed. If not, then the control variables optimization process is repeated till a final number of wafers may be reached (960). In one embodiment, the genetic algorithm controller is purposely designed to get close to the desired optimum process parameters for an actual process run, with the final achievement of desired

process performance being taken over by a real-time in-situ process control scheme 935, described next.

[00140] The second category of automatic process control relies on data analytics for real-time adjustment of process parameters to achieve the desired process performance. Current advanced manufacturing factories, such as semiconductor manufacturing, heavily rely on these concepts to maximize manufacturing yield with high levels of automation. Several concepts exist in this category of automatic process control, ranging from run-to-run control to predictive maintenance. The key concept underpinning this scheme is the use of a high volume of sensory information, such as the in-situ optical output, to run real-time analytics based on heuristics (e.g., neural networks to determine the mapping between the control and sensed variables), statistics (e.g. statistical process control), as well as any physical or heuristic model to arrive at optimum process parameters. An example of a situation that benefits from such models is the ability to accurately predict a time delay between a change in the control variable to a corresponding change in the sensed output. Moreover, such techniques can also be used to construct a virtual MSP-CICE tool, i.e., a constantly adapting simulation of the actual tool that can be a proxy for a physical forward model, and which can be used for offline process tuning as per the first category. Such virtual tool models be tool-specific and specific to the lithographic pattern being etched, and they may vary from one tool to another even though they are of the same design as tolerances in manufacturing in electrical and thermal controllers etc. can cause distinct process signatures in different tools.

[00141] Various embodiments of the CICE system may support various substrates, such as, but not limited to Si, Ge, Si_xGe_{1-x}, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. as well as multilayers of semiconductors. In addition, various catalyst such as, but not limited to, Ag, Au, Pd, Pt, Cu, Ni, Ti, Al, W, TiN, TaN, RuO_2, IrO_2, Graphene, and the like may be used. Some embodiments of the MSP-CICE system may use various patterning techniques, such as, but not limited to plasma etching, chemical vapor etching, electrodeposition (selective), and the like. Removal techniques that may be used in some embodiments include, but are not limited to chemical vapor etching, electrolytic etching, and/or wet chemical etching. Some embodiments may use various etchants (e.g., HF, H_2SO_4, HCl, H_2O, etc.), oxidants (e.g., H_2O_2, V_2O_5, $KMnO_4$, O_2, HNO_3, electric fields etc.), solvents, additions (e.g., H_2O, Ethanol, IPA, DMSO, polymers (PVA, PLA etc.), H_2SO_4, etc.), etchant states (e.g., liquid, vapor, solid-gel, plasma), and/or catalyst assisted etch processes (e.g., electrochemical etching, electroless chemical etching, vapor etching, plasma etching, “digital” layer electrochemical/electroless chemical etching, magnetic

field electrochemical/electroless chemical etching, gel-based etching). In addition, various local and global etch monitoring techniques may be used. Examples include, but are not limited to electric field (e.g., current, voltage, capacitance, inductance, impedance, conductance, etc.), optical metrology (e.g., using a camera, spectrophotometer, image processing, etc.), concentration measurements (e.g., refractive index, conductance of solution), pressure (e.g., vapor pressure), temperature (e.g., using thermocouples, IR camera, etc.). Some embodiments may use local and/or global etch control based on electric fields (e.g., current, voltage, waveforms, wavelength, frequency, duty cycles, pulsed electric fields, etc.), optical metrology (e.g., illumination), concentration (e.g., etchant concentrations, mixing and diffusion), and/or temperature (e.g. using thermal chucks, micromirrors, etc.). Various embodiments of the setup can etch industry standard wafers or wafers that can go through standard CMOS processes. A such some embodiments may be compatible with the etchant. Some embodiments may also provide for automated handling of all substrates and etch components and chemicals.

[00142] In one embodiment, the etchant can be in the form of vapor. The apparatus for vapor based CICE comprises: control of local temperatures using a thermal chuck, monitoring of vapor pressure of each component, and/or applying an electric field in the form of a plasma. Vapors can be used to facilitate "digital" layer electrochemical/electroless chemical etching by methods: 1) alternately pulse H_2O_2 vapor and HF vapor, 2) alternately pulse H_2O_2 liquid and HF liquid, 3) alternately pulse H_2O_2 vapor and HF liquid, 4) alternately pulse H_2O_2 vapor and HF liquid, 5) H_2O_2, Plasma and fluoride ion flow/pressure alternated for alternating porosities, and/or 6) using stronger oxidant for porous layers and weaker oxidant for non-porous layers.

3D NAND Flash

[00143] Scalability of advanced memory architectures made by current pattern transfer techniques is limited by non-zero taper, sidewall damage and etch mask degradation due to high aspect ratio plasma etching. Non-Volatile Memory architectures such as 3D NAND Flash need extremely high aspect ratio etching of >64 layers of alternating material to increase the storage capacity per unit area. With increasing layers, the cost and reliability of (1) multilayer deposition, (2) anisotropic high aspect ratio channel and trench etch, and (3) staircase etch for defining contacts to each layer becomes a major limiting factor for scaling. Various embodiments provide for vertical 3D memory architectures and semiconductor process integrations using an anisotropic and highly selective etch technique.

[00144] Various embodiments of the present technology define novel lithography patterns, material stacks and process flows that incorporate various interdisciplinary technologies to get improvement in memory performance and scalability. The 3D NAND Flash process flows incorporate semiconducting material stacks that can enable metal or crystalline silicon gates, angled staircase etch, crystalline silicon channels and low-k porous dielectrics while reducing the number of lithography and high aspect ratio etch steps. In some embodiments, a wafer scale Multi Scale Precision Silicon Superlattice Etching (MSP-SiSE) fabrication tool for this purpose is also disclosed. The high selectivity and anisotropy of this etch technique can enable an indefinite number of 3D NAND Flash layers.

[00145] The ITRS Roadmap for 3D NAND Flash predicts that the number of memory layers will increase steadily from 48 layers in 2016 to 512 in 2030, at 80nm half-pitch. This requires significant development in highly anisotropic (~90^0) high aspect ratio etching of layers of alternating material. The current plasma etching methods involve expensive and time consuming alternating deposition and etch steps to ensure that this anisotropy and selectivity is maintained. A non-zero plasma etch taper angle limits the maximum number of tier stacking that can be reliably achieved. Also, due to a non-zero taper the channels etched by plasma etching limit the number of layers that can reliably be scaled as the bottom most layer has a much smaller critical dimension than the lithographically defined top layer. A workaround to overcome this limitation by stacking multiple wafers with 64 memory layers each is inefficient, expensive and increases the device volume. Separate lithography and etch steps are required for the circular channels and the rectangular slits, as different geometries cannot be etched simultaneously and reliably with plasma etching due to Aspect Ratio Dependent Etch (ARDE). Fabrication of the “staircase” for contacts to individual layers requires multiple lithography and etch steps while trying to preserve the etch masks. Various embodiments of the present technology aim to solve that by enabling an inexpensive high aspect ratio etch with high selectivity and anisotropy that can be extended to future demands of 3D NAND Flash.

[00146] Two of the most popular architectures in industry are BiCS and TCAT. Both architectures use the basic concept of Stack (multilayers of plates and dielectrics), Punch (etch holes in entire multilayer stack), Plug (deposit memory films and pillar electrodes in the etched holes). A staircase etch is then performed to create contacts to each of the plates. BiCS uses a silicon oxide/poly-Si stack, while TCAT uses a silicon oxide/silicon nitride stack where the silicon nitride is later replaced with lower resistivity material for conducting lines such as Tungsten. P-BiCS is a variant of BiCS with better lower source gate performance.

[00147] For both the vertical channel as well as vertical gate architectures, a new material stack and process flow is suggested that can be etched using SiSE. The catalyst pattern is lithographically defined such that both the circular channels and rectangular slits can be etched simultaneously with high aspect ratio anisotropic etching. The material stack will be made of either bulk Si or alternating layers of semiconducting material like Si, Ge with different dopant types and/or doping concentrations. The CICE etch will result in layers with different etch and oxidation rates for layer-selective processing. This shall enable both increase in number of layers as well as a decrease in half pitch resulting in many-fold increase in storage capacity per die. Also, by combining both the channel and slit lithography and high aspect ratio etch steps, significant gains in cost per wafer shall be realized. An optional alkaline crystal-plane dependent etch can also be done for a taper that can be converted into a staircase with a plasma etch.

[00148] Some embodiments can be used both for Charge Trap (CT) as well as Floating Gate (FG) NAND Flash memories. The Lower Select Gates (LSG) can be fabricated before or after the deposition of the alternating material stack. The memory material can be either CT or FG. A timed etch can be used to create a recess in the oxidized porous layers for 3D FG NAND. Polysilicon and core filler deposition in the channel can be done before (channel last process) or after (dielectric last process) the CICE Etch. In an embodiment of the gate last approach, Si and Ge layers can be etched, and Ge can be removed prior to filling with a low-k dielectric.

[00149] The final device thus is a 3D NAND Flash memory array with more than 20 alternating layers of conducting (or doped semiconducting) and insulating material, where the vertical gate or vertical channel is extremely vertical and has an angle of $>89.5^0$ which is measured by taking a cross-sectional image using a scanning electron microscope (SEM) and then using an image analysis software such as ImageJ. The average taper angle is measured using a straight line approximately conformal using a linear-fit algorithm between any difference in the feature size of the top and bottom of the critical feature. The critical dimensions of the vertical gate architectures can be the width of the channel or the width of the trenches between the channels. For the vertical channel embodiment, the critical dimensions are the diameter of the channel or the width of the trenches between blocks of memory. Since the vertical sidewall angle is greater than 89.5^0 for CICE processes, center-to-center distance between critical features such as the circular channels or rectangular slits can be sub-20nm. The dimensions of the critical features can be measured using metrology techniques such as SEM, CD-SEM, transmission electron microscopy (TEM) and atomic force microscopy (AFM). The arrangement of circular channels can be hexagonal to create more compact 3D NAND cells.

[00150] The complete fabrication process to create 3D NAND arrays for both vertical channel and vertical gate architectures with SiSE is shown in Fig. 13. Since 3D NAND devices require alternating layers of conducting and insulating lines, the SiSE process is designed to get alternating layers of material that differ in processing parameters such as oxidation rates and etch rates to enable further processing via layer material replacement or modification. Various paths can be taken to get the alternating layers of conducting and insulating structures as described in Table 1. Paths I and II describe the initial substrates required to get superlattices. Path I uses bulk silicon wafers with no multilayer depositions, while Path II uses a stack of silicon layers with alternating doping concentrations. Paths A-G can be used in conjunction with both Path I and II, i.e. with either bulk SI or alternating layers of Si with different doping concentrations. Path A gives the option of including staircase etch by creating a taper using crystallographic or inclined etching, and the dashed lines represent some of the options where this step can be performed in the process flow. Paths B-G describe some of the methods of modifying or replacing the superlattices that are produced by the SiSE process to get final 3D NAND arrays.

Table 1: Paths I and II for 3D NAND array fabrication with SiSE, based on Fig. 13.

Paths	Initial Layers	Superlattice layers after SiSE
I, A-G	Bulk Silicon substrate	Porous Si/ Non-porous Si
II, A,C-G	p++ Si / p Si	
	n++ Si / n Si	
	n++ Si /p Si	
	p++ Si / n Si	
II, A,B	p++ Si / p Si	
	n++ Si / n Si	
	n++ Si / p Si	
	p++ Si /n Si	

[00151] The main purpose of this alternating stack etch is to get a large difference in etch or thermal processing (such as oxidation and nitridation) rates between the different layers (Layer A vs Layer B for bilayer stacks) and to use this difference to modify the stack and ultimately get insulating/conducting multilayer structures.

[00152] The porosity of the layers is a function of the etchant concentrations, the doping of the silicon substrate, and the current density across the wafer during SiSE. An embodiment of multilayers of porous and non-porous silicon made with SiSE consist of porous layers having a

porosity from 30% to 75%, while the non-porous layers have a porosity less than 10%. The porosity is measured by cross-sectional SEM and TEM images and processed using an image processing software such as ImageJ. Porosities of single layers may also be measured using gas adsorption experiments such as by using the Brunauer–Emmett–Teller (BET) theory, wherein CICE is performed on a bulk substrate with a patterned catalyst and exposed to a current density to create a thick layer of porous silicon with porosity parameters corresponding to the porous set of alternating layers.

[00153] Figs. 10A-10E illustrate catalyst mesh examples according to one or more embodiments of the present technology. In Fig. 10A, isolated catalyst nanodots 1010 and trenches 1020 are illustrated. In Fig. 10B, catalyst nanodots 1010 and trenches/slits 1020 can be connected by lines 1030 (top figure) or by controlling the diameter and alignment of the dots and trenches to ensure they are connected as illustrated in the bottom figure of Fig. 10B. In Fig. 10C, staggered connected catalyst nanodots 1010 and trenches/slits 1020 are illustrated. In Fig. 10D, connected links 1040 are patterned into the catalyst features for BiCS-type layout with sparse word-line trenches/slits 1020 are illustrated. In Fig. 10E, connected links 1040 are patterned into the catalyst features for P-BiCS-type layout with word line trenches/slits between every 2 rows of channels are illustrated.

[00154] In another embodiment, features such as holes for VC 3D NAND or lines for VG 3D NAND are etched in bulk silicon using plasma etching. Electrochemical etching without a catalyst is then performed on the etched substrate to create alternating layers of silicon with highly porous and lower porosity porous layers with a sufficient etch or thermal processing selectivity between the layers. This results in a multilayer stack of high aspect ratio features, wherein one of the layers may be oxidized or selectively replaced to create 3D NAND devices.

[00155] Path I – SiSE with Catalyst and Electrochemical Etching

[00156] The substrate, such as a bulk silicon wafer, is patterned with a catalyst and etched with a solution containing fluoride species and (optionally) an oxidant species. During the SiSE process, electric field parameters such as current density are modulated to create alternating layers with different porosities. In one embodiment, the current density is modulated using a square wave function with one zero and one non-zero value. This causes the “zero value” current density etch to progress solely with the catalyst etch, while the non-zero value uses a combination of catalyst etching as well as electric field etching to create porosity in the layers. Thus, the resulting superlattice has alternating layers of zero and non-zero porosities along with high aspect ratio etched features that correspond to the inverse of the catalyst pattern. In another embodiment,

the current density can be modulated using a square wave function with a negative and a positive value. This causes the "negative value" current density etch to prevent wandering of the catalyst, and the "positive value" current density etch to create porosity in the layers. This path does not require expensive process such as the deposition and etch of multiple alternating layers of material.

[00157] Path II – SiSE with Catalyst Etching

[00158] Path II requires alternating layers of semiconducting material that vary in at least one of the following properties: material type, doping concentration and dopant material. These layers are deposited via epitaxy, chemical vapor deposition (CVD), physical vapor deposition (PVD) etc. to enable creation of superlattices during SiSE. Table 1 describes examples of various combinations of semiconductor alternating multilayers that can be used in the process flows described above, focusing on Silicon. In Table 1, Donor and Acceptor doping of silicon is denoted by p- and n-Si, and the "++" denotes the doping concentrations. For example, p++ Si means highly doped silicon with a Boron concentration of 1e18 cm-3 or higher. More than 2 alternating layers can be used (e.g. ABCABC) for higher degree of control over doping variations and diffusion. An embodiment of this is using atomically thin layers of Ge between the doped Si layers to decrease migration of dopants during deposition. The main feature of this alternating stack etch is to get a large difference in processing parameters such as etch or oxidation rates between the different layers (Layer A vs Layer B for bilayer stacks) and use this difference to modify the stack and ultimately get insulating/conducting lines.

[00159] The etched stack of alternating materials with alternating morphologies as a result of the SiSE process are post-processed with thermal oxidation and/or ALD to get the desired stable configuration of etched channels and slits. Fig. 11 shows an embodiment of the process flow 1100 for an alternating stack of highly doped and undoped (or low-doped) silicon. Highly p-doped silicon becomes porous and this porosity can be controlled based on the etchant concentrations and the doping of the silicon layer. The low doped silicon does not change morphology after etch. The porous silicon can then be oxidized at a much higher rate than the non-porous Si. A thermal step to transfer dopants from the oxidized porous silicon (OPS) and flow more dopant gases will then modify the low doped silicon into a word line in the Vertical Channel regime. A short anisotropic oxide etch and subsequent ALD of metal will make the word lines continuous on both sides of the etched channel, and annealing will form low resistivity silicide WLs. This process is termed "Dielectric/Gate first" as the material stack deposited (or grown epitaxially) prior to the SiSE process is in the final etched and thermally processed stack.

[00160] Fig. 11 shows a process flow 1100 for high aspect ratio (HAR) etch of channels and slits with a catalyst mesh pattern similar to that shown in Fig 10. The etched stack of alternating materials with alternating morphologies as a result of the SiSE process are post-processed with sacrificial layer removal and/or atomic layer deposition (ALD) to get the desired stable configuration of etched channels and trenches/slits. As illustrated in Fig. 11, during process step 1110, deposition of alternating multilayers is performed. This step is not needed if the system starts with a bulk silicon substrate. During process step 1120, a catalyst mesh is patterned and then SiSE is performed to get alternating layers of porous and non-porous material. During process step 1130, oxidation of porous layers is performed. The oxidation process can also oxidize a thin edge of the non-porous layer that needs to be removed. Process Step 1140 is used to remove the oxide using an anisotropic etch such as Atomic Layer Etching or plasma etching after lithography to block of material that shouldn't be etched. Process Steps 1150 – 1160 comprise of multiple lithography, deposition and etch processes needed to create a 3D NAND Flash memory array. In some embodiments, process step 1150 comprises selective deposition of metal on the non-porous layers and subsequent silicide formation. Process step 1160 comprises lithography and deposition of memory film e.g., for charge-trap (CT) 3D NAND- a trilayer of silicon Oxide, silicon Nitride, silicon Oxide (ONO), poly-Si, and deposition of low k dielectric and core filler using ALD and CVD.

[00161] Fig. 12 illustrates a sacrificial process flow 1200 for vertical channel 3D NAND according to one or more embodiments of the present technology. This process is similar to that of Fig. 11 with the major difference being the post-processing steps after CICE. Instead of modifying one set of alternating layers, they are etched away and then replaced with conducting material such as tungsten, cobalt, titanium nitride, tantalum nitride. First, CICE is performed on an alternating stack of highly doped and undoped (or low-doped) silicon during operation 1210. The highly doped silicon becomes porous and this porosity can be controlled based on the etchant concentrations and the doping of the silicon layer. The low doped silicon does not change morphology after etch, i.e. it remains crystalline and non-porous. The alternating stack is not required if bulk Si with time varying electric fields is being used to create layers with alternating porosities. Poly silicon and core filler are deposited in operation 1220 in the cylindrical channels and provide support during sacrificial etch 1230 of one of the alternating layers. Subsequent deposition of metal (e.g. tungsten, cobalt, titanium nitride, tantalum nitride) using CVD, ALD or electroplating in step 1240 will make the word lines. This process is termed "Dielectric/Gate last" as the material stack deposited (or grown epitaxially) prior to the CICE process is replaced either

partially (one set of alternating layers replaces by metal) or completely (the second set is then etched away and replaced with low-k dielectric) during process 1240.

[00162] Table 2 describes some examples of layer modifications that are outlined in Fig. 13. Modifications where one layer is selectively "etched away" are sacrificial process flows where Gate and/or dielectric films are replaced. This is similar to the TCAT process flows for 3D NAND fabrication. Some embodiments of this are paths C, D, E, F, G, as well as the process shown in Fig. 12. In such process flows, vertical channels have to be filled with material to support the structure as one set of alternating layers is etched away. The etched stack of alternating materials with alternating morphologies as a result of the SiSE process are post-processed with sacrificial layer removal and/or ALD to get the desired stable configuration of etched channels and slits. In one embodiment, the high aspect ratio lines are stabilized by creating lithographic links between the lines and removing them later. Poly silicon and core filler material are deposited in the cylindrical channels and provide support during sacrificial etch of one of the alternating layers. Subsequent deposition of metal (e.g. Tungsten, cobalt, nickel, tantalum nitride, titanium nitride, copper) will make the word lines. This process is termed "Dielectric/Gate last" as the material stack deposited (or grown epitaxially) prior to the SiSE process is replaced either partially (one set of alternating layers replaces by metal) or completely (the second set is then etched away and replaced with low-k dielectric).

Table 2: Paths B-G for 3D NAND array fabrication by modifying the materials in the superlattices made with SiSE, based on Fig. 13.

Paths	Superlattice Layers after SiSE	Superlattice modification 1	Superlattice modification 2	Superlattice modification 3	Superlattice modification 4	Superlattice modification 5
B	Porous Si	Porous Oxide	-	-	-	-
	Non-porous Si	Non-porous Si				
C	Porous Si	Porous Oxide	Porous Oxide	Porous Oxide	-	-
	Non-porous Si	Non-porous Si	Etched away	Metal Fill		
D	Porous Si	Porous Oxide	Etched away	Metal Fill	Metal Fill	Metal Fill
	Non-porous Si	Non-porous Si	Non-porous Si	Non-porous Si	Etched away	Dielectric Fill
E	Porous Si	Porous Oxide	Etched away	Etched away	Metal Fill	-
	Non-porous Si	Non-porous Si	Non-porous Si	Oxidized Si	Oxidized Si	
F	Porous Si	Etched away	Etched away	Metal Fill	-	-
	Non-porous Si	Non-porous Si	Oxidized Si	Oxidized Si		
G	Porous Si	Etched away	Metal Fill	Metal Fill	Metal Fill	-
	Non-porous Si	Non-porous Si	Non-porous Si	Etched away	Dielectric Fill	

[00163] Fig. 14-16 show some of the process flows for processing alternating layers of porous and non-porous silicon layers that are created by SiSE to create vertical channel 3D NAND

arrays. Fig. 14 comprises one replacement step and represents Path C from Fig. 13. Fig. 15-16 comprises two replacement steps, where Fig. 15 represents Path D and Fig.16 represents Path G as depicted in Fig. 13.

[00164] In Fig. 14, there are multiple steps including 1) SiSE to create high aspect ratio channels and slits with alternating layers of non-porous and porous Si, 2) Oxidation of porous layers, where a thin edge of the non-porous layer as well as connecting links are also oxidized, 3) Lithography to block the slits by depositing material such as a polymer and etching away material in areas around the slits, 4) Deposition of films that form the memory core, e.g. Oxide-Nitride-Oxide layers, poly-Si and oxide core using ALD and CVD, 5) Removal of material from slits and lithography to protect the channels. The selective removal of material from the slits such as polymer and the oxidized connecting links is done using selective etches such as with oxygen plasma to remove the polymer and atomic layer etching to remove the oxide links, 6) Selective removal of silicon layers using etchants such as TMAH without affecting the oxidized porous silicon layer, 7) Deposition of conducting material (e.g. W, Co, TiN) using chemical vapor deposition (CVD), atomic layer deposition (ALD), sputtering or physical vapor deposition (PVD), etc. and subsequent etch back to isolate the conducting lines, and 8) (not depicted in image) Fill exposed areas with insulating material.

[00165] In Fig. 15, the steps include 1) SiSE to create high aspect ratio channels and slits with alternating layers of non-porous and porous Si, 2) Oxidation of porous layers, where a thin edge of the non-porous layer as well as connecting links are also oxidized, 3) Lithography to block the slits by depositing material such as a polymer and etching away material in areas around the slits, 4) Deposition of films that form the memory core, e.g. Oxide-Nitride-Oxide layers, poly-Si and oxide core, 5) Removal of material from slits and lithography to protect the channels. The selective removal of material from the slits such as polymer and the oxidized connecting links is done using selective etches such as with oxygen plasma to remove the polymer and atomic layer etching to remove the oxide links, 6) Selective removal of oxide layers using etchants such as HF without affecting the silicon layers, 7) Deposition of a thin Oxide layer using ALD and conducting material (e.g. W, Co, TiN) using chemical vapor deposition, atomic layer deposition, sputtering, etc, followed by subsequent etch back to isolate the conducting lines, 8) Selective removal of silicon layers using etchants such as TMAH without affecting the deposited conducting material, and 9) Deposition of insulating material such as silicon oxide using ALD.

[00166] In Fig. 16, the steps include 1) SiSE to create high aspect ratio channels and slits with alternating layers of non-porous and porous Si, 2) Lithography to block the slits by depositing

material such as a polymer and etching away material in areas around the slits, 3) Deposition of films that form the memory core, e.g. Oxide-Nitride-Oxide layers, poly-Si and oxide core , 4) Removal of material from slits and lithography to protect the channels. The selective removal of material from the slits such as polymer and the silicon connecting links is done using selective etches such as with oxygen plasma to remove the polymer and atomic layer etching to remove the silicon links. 5) Selective removal of porous silicon layers using etchants such as HF or HF + H_2O_2 without affecting the non-porous silicon layers , 6) Deposition of conducting material (e.g. W, Co, TiN) using chemical vapor deposition (CVD), atomic layer deposition (ALD), sputtering, etc. and subsequent etch back to isolate the conducting lines, 7) Selective removal of silicon layers using etchants such as TMAH without affecting the deposited conducting material, and 8) Deposition of insulating material such as silicon oxide using ALD.

[00167] Fig. 17 depicts an embodiment of the 3D NAND architecture with vertical gates and horizontal silicon channels. As illustrated in Fig. 17, which represents Path F from Fig. 13, the steps include 1) SiSE to create high aspect ratio channels and slits with alternating layers of non-porous and porous Si, 2) Oxidation of porous layers, where a thin edge of the non-porous layer as well as connecting links are also oxidized, 3) Deposition of films that form the memory core, e.g. Oxide-Nitride-Oxide layers, poly-Si and oxide core using CVD, ALD, etc., 4) Lithography to create a mask for subsequent etching of memory material, 5) Etching of memory material from un-patterned areas using atomic layer etching, plasma etching, etc., 6) Deposition of Gate material such as W, poly-Si, Co, TiN, etc. In an alternative embodiment, the gate material can be patterned by removing the lithographed mask, depositing gate material over the entire structure, performing lithography and etching away gate material in un-patterned areas, 7) Removal of excess gate material and lithographed mask using plasma or chemical etching, and 8) (not depicted in image) Fill exposed areas with insulating material such as silicon oxide.

[00168] Non-sacrificial paths are similar to BiCS 3D NAND fabrication process flows and do not involve etching away any layers, such as in path B. The etched stack of alternating materials with alternating morphologies as a result of the SiSE process are post-processed with oxidation (thermal, anodic etc.) and/or ALD to get the desired stable configuration of etched channels and slits. For example, highly p-doped silicon becomes porous and this porosity can be controlled based on the etchant concentration, electric field and the doping of the silicon layer. The low doped silicon does not change morphology after etch. The porous silicon can then be oxidized at a much higher rate than the non-porous Si. A thermal step to transfer dopants from the oxidized porous silicon (OPS) and flow more dopant gases will then modify the low doped silicon into a

word line in the Vertical Channel regime. An optional short anisotropic oxide etch and subsequent ALD of metal will make the word lines continuous on both sides of the etched channel, and annealing will form low resistivity silicide WLs. This process is termed "Dielectric/Gate first" as the material stack deposited (or grown epitaxially) prior to the SiSE process is in the final etched and thermally processed stack.

[00169] Note that the superlattices that used in various embodiments begin with in Table 2 (Porous Si/ Non-porous Si) can be fabricated using Paths I or II. Also, Path A, which describes including staircase etching, can be added to the process flows of any of the paths. Other embodiments of the superlattice can include alternating layers with differing porosities and/or different materials such as such as Ge, Si_xGe_{1-x}, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. All layers of the superlattice can be non-porous as well with the alternating layers still having different processing rates of oxidation, chemical etch etc. An example is a p-doped Si/ n-doped Si superlattice where alkaline etchants such as TMAH or KOH etch only the p-type Si under electric bias. Path B can also be used to make Vertical Gate based 3D NAND Flash architectures, with crystalline horizontal silicon channels.

[00170] Various embodiments of the CICE process use a patterned catalyst that sinks into the substrate as the etch progresses, leaving behind un-patterned areas as high aspect ratio features. The catalyst meshes can be patterned to etch both channels and word-line slits (trenches) in one lithography step, and the CICE process can etch both these features simultaneously. Some examples of the catalyst meshes are shown in Figs. 18A-18C. To prevent wandering of the catalyst mesh and for reliable transport of etchant solution, electric fields, ceilings and/or linked continuous patterns can be used. The resulting high aspect ratio features can be prevented from collapse by mitigation techniques such as using surface tension gradient chemicals (ethanol, isopropyl alcohol etc.), super critical drying and lithographically connected features. These two constraints can also be met by using a patterning technique with features connected by links, and by using controlled deposition or etch after the CICE process to convert the high aspect ratio linked structure into the desired 3D NAND configuration.

[00171] Fabrication of the catalyst pattern for SiSE requires multiple lithography and etch steps. The critical dimensions and overlay requirements are shown in Figs. 18A-18C for various layout schemes for 3D NAND Flash arrays based on both Vertical Channel (VC) as well as Vertical Gate (VG) Architectures. Figs. 18A-18C show the etched features. As illustrated in Figs. 18A-18C, "a" represents the width of a block of memory channels, "b" represents the width of the lithographic links, "c" is the distance between blocks of width a, "d" represents the diameter of the

circular channels, “e” is the pitch between holes in the lateral direction, “f” is the shortest pitch of the holes arranged hexagonally, and “g” is the shortest distance between the block of width “a” and the circular channel. The thin connecting lines with width “b” are called lithographic links, and they connect isolated semiconducting features to improve stability of subsequently etched interconnected high aspect ratio multilayer semiconductor structures. The intended design of the catalyst mesh depends on the layouts of the 3D NAND Flash arrays and incorporates lithographic links to stabilize the etched structures and optionally improve diffusion of etchants and prevent wandering of the catalyst features.

[00172] Fig. 18A-18C shows layouts and dimensions for embodiments of 3D NAND arrays. Two sets of dimensions are described below: one with aggressive scaling limited by lithography constraints, and the other by assuming the minimum channel diameter is 50nm for VC based devices. VG based devices have more aggressive scaling possibilities as the lithography pattern requires mainly lines and spaces (L/S) and not holes or pillars, and L/S can be made smaller by multiple patterning.

[00173] Some embodiments for dimensions of features in Fig. 18 are: Fig. 18A shows a VC 3D NAND configuration with two rows of staggered holes per block. For a half pitch of 20nm (in X-direction) and 25nm for dots and 35nm for blocks in Y-direction, a=60nm, b=10nm, c=10nm, d=25nm, e=40nm, f=35nm and g=10nm. For a half pitch of 35nm (in X-direction) and 42nm for dots and 85nm for blocks in Y-direction, a=110nm, b=10nm, c=20nm, d=50nm, e=70nm, f=60nm and g=10nm. Fig. 18B shows a VC 3D NAND configuration with four rows of staggered holes per block. For a half pitch of 20nm (in X-direction) and 25nm for dots and 65nm for blocks in Y-direction, a=120nm, b=10nm, c=10nm, d=25nm, e=40nm, f=35nm and g=10nm. For a half pitch of 35nm (in X-direction) and 42nm for dots and 120nm for blocks in Y-direction, a=220nm, b=10nm, c=20nm, d=50nm, e=70nm, f=60nm and g=10nm. Fig. 18C shows a Vertical Gate 3D NAND geometry where lines with width “a” denote silicon channel dimensions, with a=20nm, b=10nm and c=20nm in one embodiment.

[00174] The examples of dimensions described for Fig.18 are limited by lithography and electronic properties required for the memory arrays. The VC 3D NAND channel hole must be filled with memory layer, e.g. Oxide-Nitride-Oxide (ONO) and poly-silicon channel material. The minimal poly-Si channel diameter, which is constrained by the string read current and the tolerable field enhancement, is around 20nm. The minimal ONO thickness, which is constrained by the device performance and reliability, is around 15nm. Thus, the minimal hole diameter is around 50nm. For certain process flows, an oxidation step is performed after SiSE to create alternating

layers of porous silicon oxide and non-porous silicon. This oxidation step can also oxidize a thin layer (<5nm) of the non-porous silicon at the edges. This thin layer can be retained as a memory layer or removed. If it is removed, the effective dimensions of the pattern with change by twice the dimension of the oxide. e.g., for oxidation and subsequent removal of 5nm of material, the diameter of the channel will increase by 10nm, the width of the word line will decrease by 10nm, and the width of the spacing between the lines increases by 10nm. The initial dimensions should therefore be adjusted accordingly, based on the final desired parameters.

[00175] Fabrication of sub-30nm features with even smaller connections for structural stability is extremely challenging, as electron beam lithography can write sub-10nm features but suffers from large overlay, whereas photolithography has superior overlay but poor resolution. Some embodiments can use photolithography and imprint lithography to pattern the films.

[00176] The 3D NAND feature designs shown in Figs. 18A-18C can be patterned using lithography techniques such as photolithography with multiple patterning, imprint lithography, electron beam lithography, directed self-assembly, laser interference lithography etc. The process of making the masks for these various lithography techniques is described below.

Patterning with Imprint Lithography

[00177] Fig. 19D depicts a catalyst design that has a linked structure to prevent wandering and improve diffusion. In one embodiment, the width of the link pattern is 10nm, the pitch is 25nm, and the lines are not in a regular arrangement. To fabricate such patterns, a grid pattern is made using electron beam lithography. Elements of the grid are then removed by patterning a linked structure using electron beam lithography and etching away selected regions of the grid. The resulting pattern can then be etched into the template substrate to create a master template for imprint lithography.

[00178] Imprint lithography can be used to pattern aperiodic irregular patterns with high resolution and tight pitch. For imprint lithography, a template can be made to print the catalyst patterns shown in Figs. 18A-18C. The fabrication of a template is shown in Fig. 19A-19C. The master templates 1910 and 1920 shown in 19A and 19B can be made using electron beam lithography. In one embodiment, features in Fig. 19A can be made using two sets of L/S perpendicular to each other create 20nm x 20nm blocks at a pitch of 100nm, and features in Fig. 19B can be made using 20nm diameter holes at 40nm pitch and 20nm lines at 80nm pitch.

[00179] The final master template 1930 shown in 19C can be made by imprinting with master template 1910 shown in Fig. 19A, the imprinted features are etched into a hard mask, and then

master template 1920 shown in Fig. 19B can be patterned after aligning with the features imprinted by master template 19A. In accordance with various embodiments, template alignment can be done using an alignment method where, within a lithographic field, template 1920 shown in Fig. 19B has features that are intentionally offset with varying magnitudes and directions from one subfield to the next. After imprinting, the sub-field that has the ideal alignment requirements is selected and used to create a final master template 1930 shown in Fig. 19C using a step-and-repeat method. Based on overlay alignment requirements, the final master template 1930 shown in Fig. 19C can also be made using photolithography. In this case, the second template 1920 shown in 19B is a photolithography mask with larger dimensions to take into consideration the photolithography resolution. These larger dimensions can then be decreased using plasma etch techniques. Fig. 19D is an example of a lithographically linked pattern where the lines are made with imprint lithography (whose template is made with electron beam lithography), and the dots are aligned and printed using imprint or photolithography or vice versa.

[00180] In another embodiment, fabrication of patterns such as in Fig. 19D is done using photolithography and multiple patterning. Elements of the grid are then removed by patterning and shrinking holes in selected areas and etching away the grid lines, thereby creating a linked pattern. The patterning of holes may take multiple steps due to limitations of minimum pitch with photolithography.

[00181] The current form of photolithography, 193nm wavelength with immersion, uses trilayer resists and is limited to ~ 38nm half pitch for lines and spaces. Methods such as self-aligned double (SADP)/quad (SAQP) patterning and Litho-Etch-Litho-Etch (LELE) are required to go to smaller dimensions and tighter pitch. This requires multiple deposition and etch steps, and is inherently suited towards periodic patterns. The minimum resolution and pitch for circles, however, is larger. For VG 3D NAND architectures without circles, photolithography along with trim etching can be used to create lines and spaces perpendicular to each other. The process of making patterns for VC 3D NAND are more involved.

[00182] Figs. 20A-20J show a method of making such patterns using photolithography. In the figure, the catalyst is deposited after the photolithography process, such that the exposed regions (silicon) are now covered by the catalyst material. The catalyst deposited on top of the patterned features can optionally be lifted off. Another embodiment can be used where the photolithography is done on the catalyst film and then the catalyst is etched away in exposed areas. In that case, the pattern is the inverse of that shown in Fig. 18.

[00183] Figs. 20A-20E show both cross-sectional views (top) and top-views of the lithography steps. Figs. 20F-20J show the top views only. In Fig. 20A lithographic links are made using squares of side 40nm and pitch 80nm (y direction) and 40nm (x direction) patterned with first hard mask, poly-silicon (pink) on a silicon nitride (blue) layer. In Fig. 20B trim etch is done to get squares of side 10nm. In Fig. 20C, the features are planarized with spin on glass and lines of 40nm width, 80nm pitch are aligned and patterned. In Fig. 20D, spacer material is deposited to increase the line width to 70nm. In Fig. 20E, the lines and squares are etched into a hard mask layer such as silicon nitride. In Fig. 20F, LELE is performed: align and pattern 50nm holes with 80nm pitch (x direction), 80nm pitch (y direction); trim etch to decrease the diameter to 25nm and etch into underlying silicon nitride. In Figs 20G, 20H, and 20I, step 20F is repeated with shifted alignment. In Fig. 20J catalyst material can be deposited.

[00184] Density multiplication can be used using directed self-assembly instead of multiple LELE steps in photolithography. Fig. 21 shows the process flow for making a catalyst pattern with substantially connected catalyst features using self-assembly and lithography. In Fig. 21A, dots are patterned using photolithography. In Fig. 21B, these dots are used to direct block copolymers to multiply the density using directed self-assembly. Lines are then patterned to block off areas in accordance to 3D NAND Flash catalyst designs (Fig. 21C). A subsequent etch transfers the dots that are not blocked by lines into a hard mask such as silicon nitride or carbon (Fig. 21D). Another lithography step is done to pattern lines (Fig. 21E), and etch into the hard mask (Fig. 21F). The resist is then removed to reveal the final features int eh hard mask. (Fig. 21G). In Fig. 21H, catalyst material is be deposited. Although the process does not depict lithographic links, they can be made incorporated into the process flow similar to Fig. 20. Also, patterning with self-assembly can be used to make an imprint lithography template as well.

[00185] For the 3D NAND Flash designs, etching circular channels and rectangular slits simultaneously cannot be achieved reliably with plasma etching with accurate control of sidewalls. Similarly, for the features with connecting links, the sub-10nm connections between pillars cannot be retained over high aspect ratios. Dry plasma etching processes, which are used in the semiconductor industry for anisotropically etching highly controlled nanopatterns, require expensive vacuum equipment and cannot retain cross-section shape easily when patterning high aspect ratios (>50:1). They suffer from etch challenges such as Aspect Ratio Dependent Etching (ARDE) and etch taper.

[00186] The SiSE process, on the other hand, can anisotropically etch the required pattern as well as create a superlattice without loss of resolution. However, there are various challenges

that need to be addressed to make SiSE a viable technology for commercialization. This section describes these challenges and solutions for achieving wafer-scale etching of high aspect ratio nanostructure stacks in semiconducting materials.

[00187] A step-by-step description of the various processes that could be used for this new fabrication method is defined. Parameters that need to be optimized at each step for good electrical performance of final device, mechanical stability at intermediate steps, CMOS compatibility, and cost and throughput are also listed in the following sections.

[00188] Traditional 3D NAND processes use alternating layers of SiO/SiN or SiO/Poly-Si which are etched and optionally replaced with conducting material such as W to get stacks of alternating conducting and insulating lines that form the word lines and dielectrics of 3D NAND cells. In various embodiments, alternating layers of semiconducting material may be used instead of SiO/SiN or SiO/Poly-Si. Since SiSE can etch semiconducting material while simultaneously changing their morphology depending on tailorable material properties such as doping concentration and dopant type, the alternating layers are designed to ensure selective removal or oxidation to get final conducting and dielectric lines.

[00189] This is not a problem for Path I (see, e.g., Fig. 13), where bulk silicon substrate is used for SiSE and no alternating layer deposition has to be taken into account.

[00190] The method employed for deposition of the alternating layers or "superlattice" depends on commercial availability, cost, throughput, growth rate, thermal budget, number of layers, thicknesses of layers, mobility and resistivity of layers before and after etch, employability of crystallographic etching etc. For example, poly-Si layers need higher thicknesses than epitaxial silicon to overcome grain boundary issues and get good conductivity of etched word lines. Poly-Si layers may also require a thin diffusion blocking layer between the alternatively doped layers to suppress diffusion of dopants across layers, as diffusion of dopants is higher in poly-Si than crystalline Si. In the case of epitaxial silicon, a taper etch to create staircase contacts can also be done on the crystalline layers by using alkaline etchants like KOH, TMAH and EDP.

[00191] Epitaxial (epi) growth of silicon in production today is based on Chemical Vapor Deposition (CVD), a process whereby a thin solid film is synthesized from the gaseous phase by a chemical reaction. High temperature epi growth of silicon, above 1000C, offers high throughput, in situ doping and prevents contamination, whereas Molecular Beam Epitaxy (MBE) enables abrupt steps in doping profile but with very low growth rates. Low temperature epitaxy using CVD at around 650-850C offers a compromise for the growth of the silicon superlattices described in

Table 1. Temperature, pressure, gas flow rates, substrate preparation, surface treatment and oxidation prevention are the main parameters that determine the epi superlattice quality. The partial pressure of the gas used for doping, such as B_2H_6 or PH_3, determines the doping concentration in the epi layer. Having a low total pressure during growth will allow for better junctions due to decreased contamination from gases of the previous layer. While all these parameters play a critical role in the epi growth, temperature, dopant concentrations and epi layer thicknesses are the most important as they determine what the results of the next process steps will be, as explained further below.

- Temperature: The temperature of epi growth depends on various factors. The crystallinity of the epi films can be achieved at temperatures ranging from 500C onwards. At low temperatures the diffusion of dopants is reduced and some embodiments can get abrupt profiles, but the growth rate is low. Depending on the dopant type and its diffusivity in silicon, some embodiments can calculate the diffusivity across a high-doped/low-doped interface.
- Dopant concentrations: Simulations of Fick's Laws with appropriate modifications for electric field effects, concentration values and gradients etc. are used to determine what the doping material and concentration for each alternating layer can be to get the required final diffusion profiles. This depends on the temperature of the reaction chamber, the required thermal budget of the subsequent process steps, the concentration gradient across the layers and the presence of any defects during epi growth. The diffusion coefficients of common dopants in silicon depend exponentially on the temperature. ($D = D_0.\exp(-E_a/kT)$) Slow diffusers (As and Sb) are preferred over fast diffusers (P, B and In) and the dopant selection also depends on the solid solubility limits in silicon.
- Layer Thickness: Depending on the width of the final word lines, the thickness of the conducting layer has to be tuned to minimize resistivity, while the thickness of the dielectric layer has to be tuned to reduce parasitic capacitance and maximize resistivity. If the word-line layers are made of polycrystalline silicon then the increase in resistance due to grain boundaries has to be taken into consideration.

[00192] Let us consider an example of a P++/P superlattice where one layer has Boron with a concentration of 1E18 while the other layer has a Boron concentration of 1E15. For epitaxial growth at 650C and a pressure of 10Pa mixture in an ultraclean environment, the deposition rate can be ~100nm/min. At this temperature, the diffusion constant for B is 7.7E-20 cm^2/s. To determine the diffusion profile, some embodiments need to know the thickness of each layer and

the amount of time the wafer is in the chamber, i.e. the number of layers that need to be grown. At a Boron concentration of 1E18, the resistivity of the word line is 0.04 ohm-cm. This can be decreased further by incorporating a metal to form a silicide or by annealing after the subsequent SiSE process to transfer all the dopants from the oxidized porous layer to the crystalline silicon layer. For a layer thickness of 100nm, the total growth time for 256 layers is ~5hrs. The maximum diffusion will then occur at the first layer grown, and the diffusion length is given by $x_j=2*\text{sqrt}(Dt)$. This gives the maximum diffusion length of 0.8nm. Thus, since the diffusivity is very low at 650C, the impact of temperature on the diffusion length is minimal. Further factors such as multilevel concentration gradients and electric fields can be factored in using simulations. Slow deposition rates such as 100nm/min cannot be justified from a cost perspective. At 1000C, the deposition rate is 10 microns/min, and 256 layers can be deposited in less than 3 minutes.

[00193] However, the diffusion constant for Boron at this temperature is 1.39E-14 cm^2/s, and the diffusion length is 31nm. To achieve a compromise between the 2 parameters, some embodiments pick a temperature of, or around, 800C, where a deposition rate of 1 micron/min is obtained. This will make the process of depositing 256 layers take ~30min, and 100 layers take 10min. The diffusion length of B is then ~6nm at the bottommost layer (worst case scenario) for 256 layers, and is 3nm for 100 layers. Having a sub-5nm junction for 100nm thick layers should be sufficient. However, the above junction lengths denote the distance from the interface where the concentration has changed by 1/e. This is not sufficient to make a reliable process. The SiSE process is therefore tuned to ensure that the dopant concentration at which the morphology changes from solid to porous is sharp, and this can be done by tuning the etchant concentrations.

[00194] Plasma enhanced ALD can be used in some embodiments to seal the pores of the porous layers. ALD of SiO_2 is used to fill up the holes and slits that are etched using SiSE. The substrate is then planarized to enable the next process steps including lithography and plasma etching. In accordance with various embodiments, lithography can be performed to open up the channels and prevent deposition of films in the slits. Memory layers (such as Oxide-Nitride-Oxide), poly-Si channel and core filler material can be then deposited into these channels (vertical holes).

[00195] For epitaxially grown crystalline layers of silicon, alkaline etchants such as KOH and TMAH can be used to anisotropically etch the <100> crystal plane. This would reduce the number of etch and lithography steps required for the staircase etch to create contacts to each word line layer in the vertical channel structure. This alkaline wet etch can be done on the as-grown epitaxial material stack before or after CICE. If one of the alternating layers is highly p-doped,

TMAH can be used instead of KOH depending on relative etch rates along crystal planes and at different dopant concentrations.

[00196] Fig. 22 illustrates an example of a 3D NAND staircase etch according to one or more embodiments of the present technology. After epitaxial growth of doped/undoped Si, a taper etch process is done using alkaline etchants to create contact regions for word lines. The length of the projection for contact regions depends on the thickness of the insulating layer. Another embodiment of this process involves use of electrochemical etching to create alternating layers of silicon with differing porosities based on the doping of the individual layers, without the use of CICE. This stack could then be etched with plasma etching, and angled etch prior to electrochemical etch to create the staircase.

[00197] Fig. 23 is similar to Fig. 22, with the main difference being that the taper etch is done on bulk Si instead of alternating semiconducting layers. SiSE is then performed on the taper-etched bulk Si, and then after 3D NAND memory fabrication steps, selective plasma etching is done to reveal contact regions on the conducting lines.

[00198] For Path I, bulk silicon is etched, whereas for Path II, epitaxially grown crystalline layers of silicon are etched. Crystallographic etchants such as KOH, EDP and TMAH can be used to create a taper. For instance, 30% KOH or 10% TMAH at a temperature of 60C.

[00199] Some embodiments use the process of staircase etch on bulk silicon with alkaline etchants or angled plasma etch to create contact regions for word lines. The length of the projection for contact pads depends on the thickness of the insulating layer since crystallographic etching creates a taper of 54.74^0. This would reduce the number of etch and lithography steps required for the staircase etch to create contacts to each word line layer in the vertical channel structure. However, the taper does not create vertical sidewalls for the stairs, and this might affect the reliability of placement of metal contacts to the word lines. This can be corrected by increasing the thickness of the dielectric layers or the width of the word lines depending on area consumed by the stair-stepping features . Alternatively, an angled plasma etch with faraday cages can also be used to create a taper.

[00200] As the SiSE progresses, the catalyst mesh etches the semiconductor material stack to reveal high aspect ratio features with holes and slits for 3D NAND channels and word line separation. SiSE can be stopped by using an etch stop layer, a timed etch, or by monitoring and controlling electric field parameters. The etchant composition as well as electronic hole-generation during the process results in alternating films of differing morphologies based on their

material and doping concentrations. After SiSE, one of the layers can be selectively removed or modified (e.g. oxidized) to make 3D NAND layers. The volume change during oxidation of porous silicon can be suppressed by controlling the porosity and density of pores in the porous silicon layers, thereby reducing the mechanical stress on the structures. The porous layer oxidation rate is much greater than that of single crystal silicon, and can be done at lower temperatures to increase selectivity. For instance, at 700C, the surface and bulk of porous silicon layers (for individual layers thinner than 1 micron) get oxidized in 3min, while only 3nm of the surface of crystalline silicon is oxidized in dry O_2.

[00201] Oxidation rate differences between porous silicon layers and crystalline silicon layers and etch rate differences between porous oxide and silicon or porous silicon and crystalline silicon has to be very high. This is to ensure that there is no undercut and to increase the number of memory layers that can be made with the SiSE process. Table 3 lists etchants that can be used to selectively remove one layer from a superlattice for various superlattice modifications to get 3D NAND flash arrays with alternating layers of insulating and conducting films. Surfactants and other such chemicals can be added to the etchants to improve etch selectivity of Layer A to Layer B at all crystallographic orientations where applicable. The etchants may be in liquid or vapor form.

Table 3: List of etchants that can be used to remove one layer from a superlattice with a selectivity

Layer A/Layer B	Etchants to selectively remove Layer A
Porous Si/Non-porous Si	Dil. Hydroxide solutions (KOH, NH4OH, NaOH, TMAH etc.), photoresist developer, ethylene di-amine pyro-catechol (EDP), HF, Buffered HF, HF + oxidants (H_2O_2, dissolved oxygen, DMSO, $KMnO_4$, $K_2S_2O_8$), HF + illumination, HF + alcohols, NH_4F etc.
Porous Oxide/Non-porous Si	HF, Buffered HF, Vapor HF
Non-porous Si/Porous Oxide	Dil. Hydroxide solutions (TMAH, KOH), EDP
Non-porous Si/Tungsten	Si iso etch (126 parts HNO_3 : 60 parts H_2O : 5 parts NH_4F), KOH, TMAH
SiGe/Si	HCl
Ge/Si	H_2O_2

[00202] Table 4 describes examples of various combinations of semiconductor alternating multilayers with process steps required to ensure selective removal or oxidation of one of the alternating layers to get final metal lines and dielectric layers. Donor and Acceptor doping of silicon is denoted by p- and n-Si, and the "++" denotes the doping concentrations. For example, p++ Si means highly doped silicon with a Boron concentration of 1e18 cm^{-3} or higher. More than 2 alternating layers can be used (e.g. ABCABC) for higher degree of control over doping variations.

An embodiment of this is using atomically thin layers of Ge between the doped Si layers to prevent migration of dopants during epitaxial growth. A staircase etch can also be done if the layers are grown epitaxially to get crystalline morphology by using alkaline etchants like KOH, TMAH and EDP to etch the <100> planes selectively over micron-scale range. The main feature of this alternating stack etch is to get a large difference in etch or oxidation rates between the different layers (Layer A vs Layer B for bilayer stacks) and use this difference to modify the stack and ultimately get insulating/conducting lines.

Table 4: Examples of various combinations of semiconductor alternating multilayers with process steps required to ensure selective removal or oxidation of one of the alternating layers to get final metal lines and dielectric layers.

Process	Initial Layers		Selectivity	Layer Modifications	Final Layers
Sacrificial (Similar to TCAT process)	Si	Ge	Selective etching of Ge, e.g. with peroxide	Oxidation of remaining layer	Dielectric and conducting layers (e.g. porous SiO2 and W)
	n-Si	p-Si	Alkaline etchants with electric bias etches only p-Si		
	p++ Si	p-Si	1 layer becomes porous by tuning MACE etchant ratio, dil. Alkaline solutions etch only porous layer; Alternatively, after oxidation of porous silicon, Alkaline etch of only Si		
	n++ Si	n Si			
	n++ Si	p Si			
	p++ Si	n Si			
Non-sacrificial (Similar to BiCS process)	p++ Si	p-Si	1 layer becomes porous by tuning MACE etchant ratio	Oxidation of porous layer, Anneal and dope to get dopant diffusion from the porous oxide	Dielectric and conducting layers (e.g. porous SiO2 and highly doped Si/Silicide)
	n++ Si	n Si			
	n++ Si	p Si			
	p++ Si	n Si			

[00203] Various embodiments of the present technology may be used to create 3D NAND VC with no replacement steps, similar to the BiCS process. For example, in some embodiments a substrate may be provided. Then, alternating layers of a semiconductor material (e.g., doped

or undoped Si) may be deposited. Then, lithography and taper etch using a crystallographic anisotropic etchant may be performed. The catalyst can then be patterned. For example, some embodiments may use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the catalyst may be removed using a wet etch (e.g. aqua regia) or isolate with insulator. The layers can be selectively processed (e.g., oxidize porous layers and connecting links) and the pores sealed with Atomic Layer Deposition (ALD). Lithography can be used to block areas between word lines before deposition of memory material such as Oxide-Nitride-Oxide (ONO) along with poly-Si core and/or oxide core filler. Material can then be removed from word line slits and a low-k dielectric can be deposited in slits. To create a staircase along the etched taper, the taper can be etched using a plasma etch that is selective to one set of alternating layers.

[00204] In some embodiments, a process for 3D NAND VC with Oxidation and Replacement can be utilized, similar to the TCAT process. For example, in some embodiments a substrate may be provided. Then, alternating layers of a semiconductor material (e.g., doped or undoped Si) may be deposited. Then, lithography and taper etch using crystallographic anisotropic etchant may be performed. The catalyst can then be patterned. For example, some embodiments may use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the catalyst may be removed using a wet etch (e.g. aqua regia) or isolate with insulator. The layers can be selectively processed (e.g., oxidize porous layers and connecting links) and the pores sealed with ALD. Lithography can be used to block areas between word lines and a stabilizing core (e.g., poly-Si core and oxide core filler) can be deposited.

[00205] The material can be removed from the word line slits. Atomic Layer Etching is used to remove the thin oxide layer surrounding the porous-oxide/crystalline Si structures. The next set to processes to make 3D NAND Flash arrays may include one replacement step (e.g., etch crystalline Si selective to porous oxide, pore sealing with ALD, deposit memory material ONO, deposit W and etch back to isolate word lines, etc.); or two replacement steps (e.g., etch porous oxide selective to crystalline Si, deposit memory material ONO, deposit W and etch back to isolate word lines, etch Si selective to W, deposit SiO_2, etc.) or (e.g., etch porous oxide selective to crystalline Si, deposit SiO_2 and etch back to isolate, etch crystalline Si selective to deposited SiO_2, deposit memory material ONO, deposit W and etch back to isolate word lines, etc.). And so forth and so on. Then, a low-k dielectric can be deposited in slits. To create a staircase along the

etched taper, the taper can be etched using a plasma etch that is selective to one set of alternating layers.

[00206] In some embodiments, a process for 3D NAND VC with Replacement can be utilized similar to the TCAT process. For example, in some embodiments a substrate may be provided. Then, alternating layers of a semiconductor material (e.g., doped or undoped Si, Si/SiGe, Si/Ge, etc.) may be deposited. Then, lithography and taper etch using crystallographic anisotropic etchant may be performed. The catalyst can then be patterned. For example, some embodiments may use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the catalyst may be removed using a wet etch (e.g. aqua regia) or isolate with insulator. The pores can be sealed with ALD. Lithography can be used to block areas between word lines and a stabilizing core (e.g., poly-Si core and oxide core filler) can be deposited. The material can be removed from the word line slits. The next set to processes to make 3D NAND Flash arrays may include one replacement step (e.g., etch porous silicon selective to crystalline Si, deposit memory material ONO, deposit W and etch back to isolate word lines, etch Si selective to W, deposit SiO_2, etc.); or two replacement steps (e.g., etch porous silicon selective to crystalline Si, oxidize crystalline Si, deposit memory material ONO, deposit W and etch back to isolate word lines, etc.) or (e.g., etch porous silicon selective to crystalline Si, deposit SiO_2 and etch back to isolate, etch crystalline Si selective to SiO_2, deposit memory material ONO, deposit W and etch back to isolate word lines, etc.). And so forth and so on. Then, a low-k dielectric can be deposited in slits. To create a staircase along the etched taper, the taper can be etched using a plasma etch that is selective to one set of alternating layers.

[00207] In some embodiments, a process for 3D NAND with Vertical Gate can be utilized. For example, in some embodiments a substrate may be provided. Then, alternating layers of a semiconductor material (e.g., doped or undoped Si, Si/SiGe, Si/Ge, etc.) may be deposited. Then, lithography and taper etch using crystallographic anisotropic etchant may be performed. The catalyst can then be patterned. For example, some embodiments may use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the catalyst may be removed using a wet etch (e.g. aqua regia) or isolated with insulator. The layers can be selectively processed (e.g., oxidize porous layers and connecting links). The pores can be sealed with ALD. Lithography can be used to block areas between layers and ONO memory material can be deposited. Word lines can also be deposited perpendicular to the horizontal channel lines. Then, a low-k dielectric can

be deposited in slits between the word lines. To create a staircase along the etched taper, the taper can be etched using a plasma etch that is selective to one set of alternating layers.

[00208] In one embodiment, 3D NAND can be fabricated using silicon nanowires as the channel material followed by deposition of alternating layers of conducting and insulating material. MSP-CICE and novel connecting links- or ceiling-based collapse mitigation techniques are used to pattern arrays of NWs instead of Deep Reactive Ion Etching processes. DRIE uses processes such as the Bosch process which creates a scalloped sidewall, with surface damage, which degrades FET performance. Various embodiments of the CICE process proposed here should be significantly less damaging, offering smooth sidewalls and more sophisticated cross-section geometries, thereby leading to superior performance. The high aspect ratio vertical NWs created using CICE can be used for vertical 3D NAND flash memory. This involves deposition of memory material including a high-k dielectric with large trap density for charge storage by conformal ALD on the vertical NWs. A sequence of conducting material, separated by insulating material is then deposited to form the word lines and create a NAND string leading to multi-layer ultra-high density 3D NAND Flash memory.

DRAM

[00209] DRAM products are approaching fundamental limitations as scaling DRAM capacitors and transistors is very difficult with 2D structures. The current workaround is to use stack or trench capacitors to increase capacitance per cell without compromising on real estate. However, this method has limitations of high aspect ratio trench etching for trench capacitors, and stability for stack capacitors. Also, decreasing feature sizes affect the reliability of planar and recessed channel or fin-based DRAM transistors. Certain DRAM cell configurations also use a cell size factor of 5-6F^2 instead of the ideal 4F^2 cell. As feature sizes decrease from the current 20nm half pitch to sub 10nm by 2025, there is a need for incorporating vertical cell access transistors with high aspect ratio capacitors in a self-aligned fashion.

[00210] Fig. 24 illustrates an exemplary DRAM design with deposition of transistor, capacitor and interconnect material on nanowires etched by CICE according to one or more embodiments of the present technology. The top of Fig 24 illustrates a sectional view of the capacitor region; Bit lines run perpendicular to the figure and connect the top N+ doped silicon regions. Various embodiments use a vertical nanowire based DRAM architecture that incorporates both Gate-All-Around transistors as well as self-aligned capacitors to produce a 4F^2 cell size factor. This can enable scaling of DRAM to sub-10nm half pitch. Since the vertical sidewall angle is greater than 89.5^0 for CICE processes, center-to-center distance between pillars can be sub-20nm, sub-15nm,

sub-10nm, etc. The arrangement of pillars can be hexagonal to create more compact DRAM cells. The etched pillars can be aligned perpendicular to the substrate or at an angle based on the CICE etchant concentrations. The cross-sections of the pillars can be optimized to give maximum surface area, depending on whether they can be fabricated by traditional photolithography and nanoimprint lithography with acceptable defect levels.

[00211] To isolate the nanowires for each DRAM cell, an SOI (silicon-on-insulator) substrate can be used, where the insulator acts as an etch stop for CICE and it isolates the individual nanowires. Alternatively, the base of the nanowires can be made porous using electric fields. Selective oxidation of the porous base can then be performed to electrically insulate the nanowires.

[00212] Figs. 25A-25B illustrate two process flows for CICE wet anisotropic etch to create high aspect ratio pillars without collapse according to one or more embodiments of the present technology. Fig. 25A depicts a method of collapse prevention using ceilings to extend the maximum aspect ratio that may be used. Collapse prevention using a ceiling can be done by etching the features with plasma etching or SiSE to a short, stable height; depositing the ceiling, and continuing the SiSE process. The "ceiling" can also be at a height that is along the length of the short pillars, such as at L/2, where L is the height of the short stable pillar. This gives additional support as the features are further etched and extends the maximum aspect ratio to greater than that with the ceiling on top of the short pillars. This gives structural stability to the high aspect ratio pillars and prevents collapse. The ceiling can be deposited by electron beam deposition at an angle; polymer fill, etch back and ceiling deposition; or methods such as spin coating. Materials that can be used for the ceiling include polymers, sputtered/deposited semiconductors, metals and oxides that do not react with the CICE etchants, such as Cr, Cr_2O_3, carbon, silicon, Al_2O_3, etc. In some embodiments, the ceiling can also be made porous by an additional low-resolution lithography step or by a reaction to induce porosity to the ceiling material, for instance, the ceiling material could be amorphous or poly-Si that becomes porous in the CICE etchant. Once the substrate is etched and the catalyst can be removed, deposition of memory film or dielectric filler by methods like atomic layer deposition can be done before removal of the porous ceiling. The ceiling material could also be removed in certain areas or tuned to be non-selective to Atomic Layer Deposition (ALD) thereby preventing the pores from closing and blocking the deposition pathways. After filling the features, the ceiling is etched or polished away. ALD can also be used to close off high-aspect ratio shapes after etch to create deep holes (e.g., apertures, structural voids defined by lithography pattern, etc.) without the use of isolated catalysts.

[00213] Fig. 25B shows a links-based method of ensuring stability of etched nanostructures with a diamond-shaped cross-section. If the catalyst mesh comprises both lithographic links and gaps, then a linked structure is created by etching. Fig. 26 illustrates a SEM image showing collapse of unsupported features vs supported features after CICE on silicon according to one or more embodiments of the present technology. Fabrication of sub-30nm features with even smaller link connections is extremely challenging, as electron beam lithography can write sub-10nm features but suffers from large overlay, whereas photolithography has superior overlay but poor resolution. Photolithography and imprint lithography (whose masks and templates are made with electron beam lithography) may be used to get the final linked structure that can then be made into a nanoimprint template.

[00214] In an alternate embodiment, holes can be etched with CICE to create trench capacitor DRAM cells. This architecture can also be designed to be a $4F^2$ layout to minimize area occupied by the DRAM cells. Since the vertical sidewall angle is greater than 89.5^0 for CICE processes, center-to-center distance between holes can be sub-20nm, sub-15nm, sub-10nm, etc. The arrangement of holes can be hexagonal to create more compact DRAM cells. To enhance etchant diffusion in the holes, electric fields can be used to create one or more layers of porosity along the length of the etched holes, except for the top region. The non-porous top region can be used to create a silicon transistor for the DRAM cell. The one or more porous layers can be selectively oxidized to electrically isolate the trench capacitors. The pores created in the layers of porosity can be sealed after the CICE process using atomic layer deposition of insulating material such as SiO_2, SiN, SiON etc. Trench capacitors can be created in the high aspect ratio holes by depositing capacitor material such as electrodes (poly-Si, W, TiN, Co, TaN) and high-k dielectrics (HfO_2, ZrO_2, Al_2O_3) to create MOS (metal-oxide-semiconductor), MIM (metal-insulator-metal) or MIMIM etc. configuration capacitors.

TRANSISTORS

[00215] CMOS scaling has been employed in the semiconductor industry to improve chip performance, reduce power consumption and enhance functionality, typically by increasing the transistor density. This scaling occurs by releasing a new technology node every 18 months to 2 years. Transistor density is increased by reducing the dimensions of the transistors such as gate lengths, gate oxide thickness, spacer thickness etc. As the feature sizes decreased, new technologies such as high-k dielectrics, metal gates, strain engineering and low-k spacer dielectrics have been employed with planar or recessed transistors. However, to improve electrostatics despite reduce area per transistor, 3D scaling in the form of FinFETs was introduced.

The process of making tall, thin fins with minimal sidewall damage and no collapse has been challenging as the dimensions reduced to sub-20nm. For sub-10nm nodes, innovative methods of improving electrostatics using horizontal nanosheets and nanowires has been proposed.

[00216] However, for all of these 3D geometries, the stability of the structures coupled with the fabrication challenges has limited the potential of the technology. Taller fins and/or increased number of stacked nanosheets and nanowires can improve the performance of chips and enable scaling for many technology nodes. However, plasma etching for fabrication of fins suffers from etch taper and sidewall damage that affects device performance. High aspect ratio fins with low sidewall damage having sub-10nm critical dimension can be achieved with CICE by eliminating etch taper and thereby decreasing the number of fins required per transistor. Large area control and inline metrology will be incorporated for wafer scale fabrication of the first level of transistors of optimized cross-sections ranging from rectangular fins to circular and shaped NWs. Various embodiments include a novel etch technique, Catalyst Influenced Chemical Etching (CICE) and lithography requirements to enable making high aspect ratio fins with vertical sidewalls with no plasma damage.

[00217] CICE is a catalyst based etching method that can be used on semiconductors such as Si, Ge, Si_xGe_{1-x}, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. as well as multilayers of the semiconductors. An electric field may or may not be used in conjunction with the catalyst for the etch. An etchant (such as Hydrofluoric acid HF), an oxidant (such as Hydrogen peroxide H_2O_2), and optionally a low surface tension liquid (such as Ethanol) and DI water can etch semiconducting substrates preferentially at the location of a catalyst (such as Ag, Au, Pd, Pt, Ru, Cu, W, TiN, TaN, RuO_2, IrO_2, Graphene etc.). Non-aqueous etchants can also be used if needed. Lithography techniques (such as photolithography, electron beam lithography, double patterning, quad patterning, nanoimprint- lithography etc.) are used to define the catalyst features. The resulting substrate with the catalyst mesh is placed in an etchant solution and etched precisely to a certain depth actively controlled by electrical fields and optical imaging systems that can determine the etch depth based on the electrical and optical properties during etch.

[00218] The final device thus is a finFET with high aspect ratio fins having an aspect ratio > 5:1, where the fin structure is extremely vertical and has an angle of $>89.5^0$ which is measured using a scanning electron microscope (SEM), TEM, AFM, etc. and then using an image analysis software such as ImageJ. The average taper angle is measured using a straight line approximately conformal using a linear-fit algorithm between any difference in the feature size of the top and bottom of the critical feature. The critical dimensions can be the width of the fin or the

width of the trenches between the fins. Since the vertical sidewall angle is greater than 89.5^0 for CICE processes, center-to-center distance between critical features such as the fin spacing and fin width can be sub-20nm, sub-15nm, sub-10nm, etc.

[00219] In the case of lateral nanowire and nanosheet FETs, the fins are composed of alternating layers of material, where one of the layers is selectively removed and a dielectric and gate electrode are conformally deposited to surround the suspended lateral nanowires or nanosheets. The taper of the nanosheet and lateral nanowire FETs are also measured similar to the finFETs.

[00220] Plasma etching for fabrication of fins has a variety of process challenges such as precision etching, etch taper, collapse, erosion and structural integrity, and sidewall damage. This affects device performance of the transistors. High aspect ratio and low sidewall damage for sub-10nm critical dimension fins can be achieved with CICE. The etch taper angle creates further challenges as it limits the maximum height of the fin at a certain fin width. To increase the height of the fin, the width of the fin has to be increased, which reduces the transistor packing density.

[00221] Fig. 27A illustrates a 14nm FinFET with a taper angle of ~85^0, and a physical Half Pitch (HP) of 24nm used in industry. The maximum fin height that can be achieved with such a taper angle is calculated by $Maximum\ fin\ height = 0.5 * HalfPitch * \tan(TaperAngle)$. By improving the taper angle, the maximum fin height can be increased for different fin widths and half pitches (HP). This relationship is plotted in Fig. 27B, showing the maximum height of a fin that can be etched for a given HP vs. the etch taper angle. This shows the scaling potential for etch processes that have no taper, such as CICE. This does not consider the structural stability of fins, which is examined later. 100nm of the fin height is used for Shallow Trench Isolation (STI) and is thus not a part of the active finFETs.

[00222] High aspect ratio fins are susceptible to collapse. Collapse of the fins can be mitigated using connecting links that can be modified or removed once the transistors are made and the fins are embedded in stabilizing material such as an insulator.

[00223] Fig. 28 is a plot illustrating a maximum height of a fin with no taper before lateral collapse along the length of the fin (50nm in this case), without any support/assist features. The critical height of a fin that is unsupported by any connecting links, for a length of 50nm, is shown vs its half pitch in Fig. 28. This is calculated by equating the bending energy of the fin due to collapse with the surface energy required to separate the fins:

$$h_{cr_lengthwise} = (18EI_x w^2/\gamma_{sv} b)\text{^}(1/4)$$

$$h_{cr_widthwise} = (18EI_y w^2/\gamma_{sv} a)\text{^}(1/4)$$

where E is the elastic modulus of the fin, I is the moment of inertia about the bending axis, w is the deflection of the fin, i.e. half the distance between the collapsing fins, γ_{sv} is the surface energy of the fin material, and a and b are the dimensions of the fin perpendicular to the direction of collapse (lengthwise vs widthwise).

[00224] The collapse occurs along the length of the fin at the shortest height, and is thus the height that is depicted in the graph. Although fins can be much longer based on specific circuit designs, the shortest length of a fin is determined by the contact gate pitch (CGP) of the finFET. For a minimum spacer thickness (t_s) ~5nm and source/drain (S/D) contact length (L_C)~15nm, the contact gate pitch CGP= $L_G + 2t_s + L_C$. This shows that scaling of the transistor depends on the gate length L_G which can vary between 10-25nm. An example case of 50nm is considered to determine the maximum height of a fin of different widths before it collapses laterally onto another fin. A fin pitch of double the fin width is taken as some embodiments can shrink the fin pitch due to no etch taper.

[00225] A major limitation to scaling to smaller fin widths is their structural instability. For FinFETs made with bulk silicon, a major portion of their length is utilized for shallow trench isolation (STI). Assuming the minimum height required for STI is 100nm, only fins of width 10nm and above can be used. Further, the active portion of the fins are much shorter than the initial fin height. This can be alleviated in part by using SOI wafers. However, even in case of SOI finFETs there is a limitation to the maximum height achievable for a fin. An etch taper helps in improving the structural stability of a fin to a certain extent, but eventually limits the maximum height possible as was described in Fig. 27.

FinFET Process Flow

[00226] Various embodiments improve the structural stability of the fins by using connecting links between them to stabilize the fins during and after etch. After further processing of the device, the stabilizing structures are removed or modified. In one embodiment, the connecting links can also be used in the circuit design phase to link sources and drains of adjacent finFETs alongside epitaxial S/D contact formation. An example of a process flow for a finFET is shown in Fig. 29.

[00227] An embodiment of the CICE finFET process flow is illustrated in Fig. 29, where the process steps are: a) CICE of connected fins and subsequent catalyst material removal; b) STI (Shallow Trench Isolation) fill and etchback, which may involve using Atomic Layer deposition (ALD) of STI material and etch back of the STI material using Vapor HF, Atomic Layer Etching (ALE) or Reactive Ion Etching (RIE). c) Dummy Gate and Spacer patterning and deposition, where Poly silicon is used as a dummy gate and silicon nitride is used as spacers on either side of the dummy gates; d) Oxide fill using ALD and planarization using Chemical Mechanical Polishing (CMP), cut/etch away connecting features (or links), where the connecting features between the fins are etched away using RIE, ALE, selective oxidation and vapor HF etch, etc. and the lithographic mask for etching away the connecting features can be designed to retain certain connections based on the number of fins per transistor and the transistor circuit design. e) Oxide fill and etch back; f) Source/Drain deposition using epitaxial growth of Si or Si and Ge with in-situ doping; and g) Metal Gate replacement and High-k dielectric deposition, where the dummy gate can then be replaced with high-k dielectrics and metal gates between the spacers to form the final high aspect ratio finFETs.

[00228] In another embodiment, catalyst connecting links may be used in the regions of the fins and the missing portions can be joined using epitaxial growth of silicon. For regions where the connecting links are removed, depending on the location and circuit design, material such as TiN, W, SiO_2, SiN, carbon, Si, Ge, etc. may be deposited based on the required electrical properties of the material, e.g. whether the connection needs to be conducting, insulating, or semiconducting.

[00229] High Aspect Ratio FinFETs fabricated with CICE have connecting links between the fins to prevent collapse. These links have to be removed during the fabrication process (Fig. 29 step (d)) to obtain the required fin design. In one embodiment, the finFET links are removed by first patterning and deposition of dummy gate and spacers after CICE followed by deposition of dielectric in all exposed regions. Photolithography is then done to isolate regions of fin-links that need to be removed, and the fin-links are removed using atomic layer etching, plasma etching etc. Any plasma etch taper that is created during the etch will not affect the fin structures protected by the dummy gate and spacers, and subsequent S/D epitaxy steps may replenish any lost fin material due to plasma etch taper. Alternatively, selective oxidation and removal of the exposed fin-links can be done, and the oxidized fin-links can be removed using vapor HF, plasma etching, wet etching to remove silicon oxide instead of silicon, thereby protecting the silicon fins due to the selective nature of the silicon oxide etch.

[00230] This method has the advantage of very precise overlay of < 2nm, thereby ensuring that excess material is not removed from the fins. Spacer patterning can be used to decrease the width and pitch from a photolithography resolution of 35-40nm line/spaces to 20-25nm line/spaces. To create cuts both parallel to the fins and perpendicular to the fins, two photolithography steps can be used with line/spaces at 90 degrees to each other. EUV lithography can be used to create the same features without additional spacer patterning. Based on the finFET designs for logic devices, the catalyst pattern for etching of the fins and their connecting links will be designed. For example, in Fig. 32, the starting CICE catalyst pattern and the pattern after removal of connecting links is shown.

[00231] Figs. 30A-30E illustrates an example of FinFET process after CICE according to one or more embodiments of the present technology. More specifically, Figs. 30A-30E show a top view of connected fin structures, whose design depends on the application of the finFETs, such as in SRAM and logic circuitry. In Fig. 30A, the structures etched with CICE are connected to prevent collapse. Fig. 30B depictS dummy gate and spacer patterns which are designed to connect multiple fins as needed by the circuit design. In Fig. 30C, lithography is used to expose the portions to be etched away (connecting links). In Fig. 30D, connecting links are then etched away using Atomic Layer Etching or Plasma Etching. Further finFET processing steps (not shown in Fig. 30A-30E) such as Source/Drain epitaxial deposition, gate replacement, and the like can then be performed to get the final device circuitry. Fig. 30E shows a schematic of underlying fins in part D that remain after all the finFETs processing steps.

[00232] Nanosheet FETs are made by etching fins that have alternating layers of semiconductor material and subsequently removing one of the alternating layers, resulting in suspended nanosheets. Nanosheet FETs have better electrostatics than finFETs due to their gate-all-around configuration as opposed to finFET's trigate structure. Similar to the height limitations of fins discussed in the previous section, the critical height of the alternating layers of semiconductor in the nanosheet fins limits the number of layers that can be etched using plasma etching. This limitation is not present in the SiSE process, a subset of CICE which produces nanostructures with alternating layers instead of bulk-Si. An embodiment of the nanosheet layers comprises Si and Si_xGe_{1-x}, wherein the new critical height depends on the modified elastic modulus of the multilayer stacked fins. Considering the thickness of each nanosheet to be 5nm, and the lower region of the fin that is covered by STI to be Si, the effective elastic modulus can be calculated by the "slab" model using the inverse rule of mixtures in composites: $\frac{1}{E_{eff}} = \frac{V_f}{E_f} + \frac{V_m}{E_m}$, where E is the elastic modulus and V is the volume fraction, subscript f denotes the sacrificial

nanosheet material, e.g. Si_xGe_{1-x} or porous Si and m is the remaining nanosheet material, e.g., Si.

[00233] For a volume fraction of Si ~ 75%-95%, the resulting effective elastic modulus is ~ 100-150GPa, and the critical heights for nanosheet fins are similar to those of finFET fins. The change in surface energy depends on the material of the surface at the top of the fins that is in contact. In one embodiment, that material is silicon and the influence of the material of the nanosheet is the same as that of a silicon finFET.

[00234] Alternatively, lateral nanowire FETs can be made in a similar way by reducing the width of the fin. In the SiSE process, the connected fins that are formed for finFETs using lithographic links can also be used on a stack of alternating layers of semiconductors.

[00235] Nanosheet FETs are similar to finFETs with the fins having alternating layers of material instead of bulk silicon. One embodiment comprises alternating layers of Si and Si_xGe_{1-x}, where the Si_xGe_{1-x} layer is removed to give silicon nanosheets. Another embodiment consists of alternating layers of differently doped Si, which produces sacrificial porous Si layers and crystalline Si nanosheets. In a further embodiment, protective layers between the alternating layers are used to ensure the silicon nanosheets are unaffected by sacrificial nanosheet etch, such as by using an alternating stack of low-doped Si/ Si_xGe_{1-x} /high-doped Si/ Si_xGe_{1-x} or low-doped Si/ Ge /high-doped Si/ Ge, where the high-doped Si is converted to porous Si and low-doped Si remains crystalline. SiSE process is tuned to ensure that the morphology changes from porous to non-porous at a specific doping concentration, creating a multilayer stack of porous and non-porous Si. The porous Si can be selectively removed resulting in suspended nanosheets of Si. The etchant composition as well as hole-generation during the process results in alternating films of differing morphologies based on their material and doping concentrations. In another embodiment, the SiSE process is used with a time-varying electric field on bulk Si to create nanosheet fins with alternating layers of porous and non-porous Si. An exemplar process flow is described in Fig. 31.

[00236] Fig. 31 illustrates an example of a process flow for making nanosheet FETs and lateral nanowire FETs with SiSE according to one or more embodiments of the present technology. The steps include a) SiSE of connected fins and removal of catalyst material; b) Dielectric fill to create STI (Shallow Trench Isolation) using Atomic Layer deposition (ALD); c) Cut/etch away connecting features, where the connecting features between the fins are etched away using RIE or ALE, and the lithographic mask for etching away the connecting features can be designed to retain certain connections based on the number of fins per transistor and the transistor circuit

design; d) deposition of stress liner such as silicon nitride in the cut away areas using ALD; e) dielectric (STI) etch back and selective removal of alternating layers to get suspended nanosheets/nanowires; f) dummy gate and spacer patterning and deposition, where poly-silicon is used as a dummy gate and silicon nitride is used as spacers on either side of the dummy gates. A spacer can be deposited around dummy gate, excess spacer material can be patterned/etched and oxide fill and planarization can be performed; g) S/D deposition where Source and Drain regions are then deposited using epitaxial growth of Si or Si and Ge with in-situ doping; and h) metal gate replacement and High-k dielectric deposition.

[00237] In another embodiment of SiSE for nanosheet FETs, time-varying electric fields can be used along with the catalyst etch to create alternating layers of porous and non-porous Si by using bulk Si instead of alternating epitaxial layers of material as the starting substrate.

[00238] The selective removal of alternating layers of the nanosheets is done using a selective etch process. For example, in a stack of Si/ Si_xGe_{1-x} , HCl may be used to selectively remove the Si_xGe_{1-x}. In a stack of Si/Porous-Si, etchants such as HF, TMAH, vapor HF, HF and a weak oxidant such as Hydrogen peroxide, etc. can be used. In stacks with multiple alternating materials such as low-doped Si/ Si_xGe_{1-x} /high-doped (porous after CICE) Si/ Si_xGe_{1-x}, HF can be used to remove the porous Si and then HCl is used to remove the Si_xGe_{1-x}.

[00239] The catalyst is designed for prevention of collapse such that all fins are connected using lithographic links. To further prevent wandering of catalyst in cases where the wandering cannot be suppressed using SiSE and/or electric fields, connected links are made with lithographic links connecting all the catalyst regions while ensuring that all the fins are connected to prevent collapse.

[00240] The critical height of a fin before collapse can be increased by using connecting links at the ends of the fins near the S/D regions. These links can later be removed after stabilizing the fin with gates, spacers and insulating material. Fig. 32 plots the critical heights before lateral collapse for different number of fins along the length and width of the fin structures. For a contact gate pitch (CGP) of 50nm, connecting links of 10nm width are used on both sides of the fins to improve stability. The maximum height of the fins when all of the fins are connected to each other in a square mesh as shown in Fig 32 can be simulated as a thin long plate with 3 fixes sides.

[00241] Fig. 32A provides an illustration of connecting links when number of fins > 1. For N=1, the length b equals the CGP of the finFETs, whereas for N>1 the length b=CGP+2*(link width). In Fig. 32B, the critical heights before collapse along the length of the connected fin

structure is shown for different fin widths f and for number of fins ranging from 1 to 10. In Fig. 32C, the critical heights before collapse along the width of the connected fin structure is shown for different fin widths f and for number of fins ranging from 1 to 10. To prevent wandering of the catalyst in larger blocks of connected fins, a linked mesh can be utilized as shown below for a block of 6x4 fins. Multiple blocks may be completely separated or connected via links of semiconductor. 32D is a plot illustrating the critical heights before collapse along the width of the connected fin structure is shown for different fin widths f and for number of fins ranging from 1 to 10.

[00242] To create devices from the connected fins etched using CICE, one of the critical steps is dielectric etch back to create shallow trench isolation (STI) regions at the base of fins. This step is necessary for all embodiments of this process other than for SOI (silicon-on-insulator) wafers. The dielectric, such as SiOx, can be deposited on the high aspect ratio fins of width < 15nm using conformal deposition methods such as atomic layer deposition. Timed etch back of the dielectric should ideally create ~100nm thick STI at the base of the fins while not affecting the fins themselves. Plasma etching is typically used for this process. However, the physical component of the plasma etching process can damage the fins. Vapor HF can be used for a purely chemical process to etch back the dielectric without damaging the fins. In one embodiment, a separate material (such as silicon nitride) can be deposited using ALD around the fins before the oxide dielectric deposition. This will create an etch stop on the fins and prevent any damage in a selective chemical etch.

[00243] The uniformity of such etch-back processes from center-to edge of the wafer needs to be controlled. This can be done using multiple temperature zones in a vapor HF setup. A “send ahead” wafer can be used to optimized the timed etch and map the various regions with discontinuities in the etch rate and depth. The discontinuities can be smoothened by creating local high and low temperature zones to modify the local etch rate to create uniform etch depths.

[00244] Alternatively, a silicon containing polymer can be dispensed using inkjets precisely on locations with high etch rates, such as the edge of the wafers. The dispensed volumes can be determined using the data from the send-ahead wafers. The substrate is then baked at an optimized temperature to create intentional non-uniform heights of material on the substrate. This will cancel out non-uniform etching by Vapor HF, and thus ensure that the final etch uniformity for creating STI in fins is within specifications.

[00245] In another embodiment, the bulk Si fins in finFETs and the nanosheet fins in nanosheet FETs can be electrically isolated from each other by creating a porous bottom layer

during the SiSE process using electric fields, etchant concentrations and/or doping concentration of the layer to be etched such that the layer becomes porous after the etch. The porous bottom layer may be 100nm thick. The porous layer is then selectively oxidized to create oxidized porous Si at the bottom of the fins which thereby act as Shallow Trench isolation (STI) and electrically isolate the fins. For nanosheet FETs, the alternating porous layers may also be oxidized when the bottom porous layer is oxidized.

[00246] Various embodiments of the present technology provide techniques for manufacturing FinFETs. For example, in some embodiments, the catalyst can be patterned using lithography, depositing a discontinuous catalyst such as Pt, Pd, Ru, Au, etc. and performing Chemical Mechanical Polishing or Lift-off. Alternatively, selective electrodeposition of catalyst can be done after lithography. After the SiSE process, the catalyst material can be removed using wet etching (e.g. with aqua regia) or it can be isolated from the device layers using an insulator. To create an STI layer, an insulator can be deposited and planarized. Lithography and etch of excess fin connecting structures can then be performed. Then, lithography and deposition of stress liner material can be performed. An etch-back to get shallow trench isolation (STI) may be performed if needed using methods such as timed vapor HF etch. For nanosheet transistors, selective removal of alternating layers to get suspended nanosheets is performed. For example, some embodiments may etch Si_xGe_{1-x} selective to Si, and/or etch porous Si selective to Si. A dummy gate can then be patterned. For example, in some embodiments, lithography for dummy gate pattern may be performed and dummy gate material (oxide, poly-Si) may be deposited. A spacer can be deposited around the dummy gate and pattern/etch excess spacer material. An oxide fill and etch back may be performed. In some embodiments, lithography can be used to expose for S/D region. Then, S/D deposition (e.g. doped epi growth) may be performed. The poly-Si dummy gate can be etched away and replaced with a high-k dielectric and metal gate. An insulator, such as silicon oxide can then be deposited and planarized to complete fabrication of the transistor layers. Further processing is then done to create metal layer contacts, thereby creating a working transistor device, and an oxide fill and planarization of the metal layers can be completed.

Conclusion

[00247] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not

limited to." As used herein, the terms "connected," "coupled," or any variant thereof means any connection or coupling, either direct or indirect, between two or more elements; the coupling or connection between the elements can be physical, logical, or a combination thereof. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or," in reference to a list of two or more items, covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[00248] The above Detailed Description of examples of the technology is not intended to be exhaustive or to limit the technology to the precise form disclosed above. While specific examples for the technology are described above for illustrative purposes, various equivalent modifications are possible within the scope of the technology, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative implementations may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified to provide alternative or subcombinations. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed or implemented in parallel, or may be performed at different times. Further any specific numbers noted herein are only examples: alternative implementations may employ differing values or ranges.

[00249] The teachings of the technology provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various examples described above can be combined to provide further implementations of the technology. Some alternative implementations of the technology may include not only additional elements to those implementations noted above, but also may include fewer elements.

[00250] These and other changes can be made to the technology in light of the above Detailed Description. While the above description describes certain examples of the technology, and describes the best mode contemplated, no matter how detailed the above appears in text, the technology can be practiced in many ways. Details of the system may vary considerably in its specific implementation, while still being encompassed by the technology disclosed herein. As noted above, particular terminology used when describing certain features or aspects of the

technology should not be taken to imply that the terminology is being redefined herein to be restricted to any specific characteristics, features, or aspects of the technology with which that terminology is associated. In general, the terms used in the following claims should not be construed to limit the technology to the specific examples disclosed in the specification, unless the above Detailed Description section explicitly defines such terms. Accordingly, the actual scope of the technology encompasses not only the disclosed examples, but also all equivalent ways of practicing or implementing the technology under the claims.

[00251] To reduce the number of claims, certain aspects of the technology are presented below in certain claim forms, but the applicant contemplates the various aspects of the technology in any number of claim forms. For example, while only one aspect of the technology is recited as a computer-readable medium claim, other aspects may likewise be embodied as a computer-readable medium claim, or in other forms, such as being embodied in a means-plus-function claim. Any claims intended to be treated under 35 U.S.C. § 112(f) will begin with the words "means for", but use of the term "for" in any other context is not intended to invoke treatment under 35 U.S.C. § 112(f). Accordingly, the applicant reserves the right to pursue additional claims after filing this application to pursue such additional claim forms, in either this application or in a continuing application.

CLAIMS

What is claimed is

1. A method for improving reliability of catalyst influenced chemical etching, the method comprising:

patterning a catalyst layer on a surface of a semiconducting material, wherein said catalyst layer comprises a plurality of features and lithographic links between two or more of the plurality of features;

exposing said patterned catalyst layer on said surface of said semiconducting material to an etchant, wherein said patterned catalyst layer causes etching of said semiconducting material to form fabricated structures corresponding to the plurality of features and gaps corresponding to the links; and

depositing material sufficient to fill said gaps.

2. The method as recited in claim 1, wherein said lithographic links have connecting lines that join substantially isolated nodes of said catalyst layer.

3. The method as recited in claim 1, wherein said lithographic links in said patterned catalyst layer result in missing portions of high aspect ratio structures, and the method further comprises filling the missing portions with SiO_2, SiN, epitaxial Si, W, TiN, or carbon.

4. The method as recited in claim 1, wherein the material is one of the following:

single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm deposited on a substrate, an SOI (silicon on insulator) wafer, or a layer of epitaxial silicon of thickness greater than 100nm on a substrate.

5. The method as recited in claim 1, wherein the material comprises alternating layers of semiconductor materials of varying doping levels and dopants, highly doped silicon and lightly doped silicon, undoped silicon and doped silicon or germanium, Silicon and Si_xGe_{1-x}, differently doped silicon and/or Si_xGe_{1-x}, differently doped silicon and/or Ge, or Si and Ge.

6. The method as recited in claim 5, wherein the fabricated structures have periodic variations in at least one of porosity, pore size, pore orientation, etch rate, or thermal processing rates.

7. The method as recited in claim 5, wherein a thickness of each alternating layer is between 1nm and 100nm.

8. The method as recited in claim 5, wherein at least one of the alternating layers is selectively removed.
9. The method as recited in claim 8, wherein Si_xGe_{1-x} layers are removed by HCl to create Si nanosheets and/or lateral nanowires.
10. The method as recited in claim 5, wherein one of the doped layers of silicon becomes porous in the presence of the etchant used in CICE.
11. The method as recited in claim 10, wherein the porous Si layers are removed using HF, HF vapor, HF and a weak oxidant, KOH or TMAH.
12. The method as recited in claim 1, wherein said catalyst layer sinks into the semiconducting material in the presence of an etchant.
13. The method as recited in claim 1, wherein said etchant comprises at least two of the following:
fluoride species containing chemicals HF or NH_4F;
oxidants H_2O_2, $KMnO_4$, or dissolved oxygen;
alcohols ethanol, isopropyl alcohol, or ethylene glycol; or
protic, aprotic, polar and non-polar solvents such as DI water, or dimethyl sulfoxide (DMSO).
14. The method of claim 1, wherein the semiconducting material can be Ge, GaAs, GaN, Si, SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.
15. The method of claim 1, wherein the catalyst layer comprises one or more of the following: Au, Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN, RuO_2, IrO_2, or Graphene.
16. The method as recited in claim 1, wherein the fabricated structures have at least one lateral dimension that is less than 100nm; and an aspect ratio of height of features to minimum lateral dimension that is at least 5:1.
17. The method as recited in claim 1, wherein a time varying electric field is used to produce alternating layers of etched nanostructures wherein at least one of the alternating layers is porous.
18. The method as recited in claim 17, wherein the fabricated structures have periodic variations in at least one of the following: porosity, pore size, pore orientation, etch rate and thermal processing rates.
19. The method as recited in claim 17, wherein the porous Si layers are removed using HF, HF vapor, HF and a weak oxidant, KOH or TMAH.
20. The method in claim 1, wherein the resulting structures after modifying the connecting links are used for subsequent formation of finFETs, lateral nanowire FETs or nanosheet FETs.
21. The method in claim 20, wherein a dielectric is deposited and a timed chemical etch is used to create a shallow trench isolation for bulk finFETs or nanosheet FETs.

22. The method as recited in claim 1, wherein said semiconducting structures are used to make DRAM cells.

23. The method as recited in claim 1, wherein said semiconducting structures are used to make 3D NAND Flash.

24. A method for preventing substantial collapse of high aspect ratio semiconducting structures by catalyst influenced chemical etching, the method comprising:

patterning a catalyst layer on a surface of a semiconducting material, wherein said catalyst layer comprises a plurality of features and lithographic gaps between two or more of the plurality of features;

exposing said patterned catalyst layer on said surface of said semiconducting material to an etchant, wherein said patterned catalyst layer causes etching of said semiconducting material to form structures corresponding to the plurality of features and links corresponding to the gaps; and

modifying one or more of said links.

25. The method as recited in claim 24, wherein said lithographic links in said interconnected high aspect ratio structures are selectively modified by one or more of the following methods: oxidation, nitridation, selective etch, lithography with precise alignment and plasma etch of certain portions of the links.

26. The method as recited in claim 24, wherein the material is one of the following:

single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm deposited on a substrate, an SOI (silicon on insulator) wafer, a layer of epitaxial silicon of thickness greater than 100nm on a substrate.

27. The method as recited in claim 24, wherein the material comprises alternating layers of semiconductor materials of varying doping levels and dopants, highly doped silicon and lightly doped silicon, undoped silicon and doped silicon or germanium, Silicon and Si_xGe_{1-x}, differently doped silicon and/or Si_xGe_{1-x}, differently doped silicon and/or Ge, or Si and Ge.

28. The method as recited in claim 24, wherein the material comprises alternating layers of semiconductor material wherein the semiconducting materials have varying doping levels and dopants, highly doped silicon, lightly doped silicon, undoped silicon, doped silicon and germanium, silicon and Si_xGe_{1-x}, differently doped silicon, and/or $S_{ix}Ge_{1-x}$, with differently doped silicon and/or Ge, or Si and Ge.

29. The method as recited in claim 28, wherein the fabricated structures have periodic variations in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal processing rates.
30. The method as recited in claim 28, wherein the thickness of each layer is between 1nm and 100nm.
31. The method as recited in claim 28, wherein at least one of the set of alternating layers is selectively removed.
32. The method as recited in claim 31, wherein Si_xGe_{1-x} layers are removed by HCl to create Si nanosheets and/or lateral nanowires.
33. The method as recited in claim 28, wherein one of the doped layers of silicon becomes porous in the presence of the etchant used in CICE.
34. The method as recited in claim 33 wherein the porous Si layers are removed using HF, HF vapor, HF and a weak oxidant, KOH or TMAH.
35. The method as recited in claim 24, wherein said catalyst layer sinks into the semiconducting substrate in the presence of an etchant.
36. The method as recited in claim 24, wherein said etchant comprises at least two of the following:
    fluoride species including HF or NH4F;
    oxidants including H_2O_2, KMnO4, or dissolved oxygen;
    alcohols including ethanol, isopropyl alcohol, or ethylene glycol; or
    protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).
37. The method of claim 24, wherein the semiconducting material can be Ge, GaAs, GaN, Si, SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.
38. The method of claim 24 where the catalyst layer comprises one or more of the following: Au, Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN, RuO_2, IrO_2, or Graphene.
39. The method as recited in claim 24, wherein the fabricated structures have at least one lateral dimension that is less than 100nm; and an aspect ratio of height of features to minimum lateral dimension that is at least 5:1.
40. The method as recited in claim 24, wherein a time varying electric field is used to produce alternating layers of etched nanostructures wherein at least one of the alternating layers is porous.
41. The method as recited in claim 40, wherein the fabricated structures have periodic variations in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal processing rates.

42. The method as recited in claim 40, wherein the porous Si layers are removed using HF, HF vapor, HF and a weak oxidant, KOH or TMAH.
43. The method in claim 24, wherein the resulting structures after modifying the connecting links are used for subsequent formation of finFETs, lateral nanowire FETs or nanosheet FETs.
44. The method in claim 43, wherein a dielectric is deposited and a timed chemical etch is used to create a shallow trench isolation for bulk finFETs or nanosheet FETs.
45. The method as recited in claim 24, wherein said semiconducting structures are used to make DRAM cells.
46. The method as recited in claim 24, wherein said semiconducting structures are used to make 3D NAND Flash.
47. A method for preventing substantial collapse of high aspect ratio semiconducting structures by catalyst influenced chemical etching, the method comprising:

creating a support structure by depositing a material on either a patterned catalyst layer or across two or more uncollapsed semiconductor structures; and

exposing said support structure to an etchant to form higher aspect ratio semiconductor structures with said material to prevent substantial collapse of said higher aspect ratio said semiconducting structures.

48. The method as recited in claim 47, wherein said uncollapsed semiconductor structures are made from one or more of the following processes: plasma etch, dry etch, chemical etch and catalyst influenced chemical etching.
49. The method as recited in claim 47, wherein a substrate of said structure comprises one or more layers of semiconducting films.
50. The method as recited in claim 47, wherein said material is resistant to etchant material that includes Cr, polymer, carbon, Cr_2O_3, or Al_2O_3.
51. The method of claim 47, where the material is deposited either at the top or along the length of the structures.
52. The method of claim 51, wherein the material deposition location is at a height of L/N from the top of the uncollapsed structures, where L is the height of the said structures and N is a number that is greater than or equal to 1, and is determined by height stability mechanics to avoid collapse.

53. The method as recited in claim 47, wherein said material is made porous either during deposition or after exposure to said etchant.

54. The method as recited in claim 47, wherein the capping material is patterned to ensure etchant flow to catalyst film during CICE.

55. The method as recited in claim 47, wherein voids between said high aspect ratio semiconducting structures are filled with second material.

56. The method in claim 55, wherein the support structure material is selectively removed after further filling with second material.

57. The method as recited in claim 56, wherein said structure is used to make DRAM cells.

58. The method as recited in claim 56, wherein said structure is used to make 3D NAND flash arrays with vertical channels.

59. An apparatus for catalyst influenced chemical etching, comprising:

a process chamber to house a semiconductor wafer which comprises a catalyst on at least one surface of the semiconductor wafer and an etchant;

a plurality of actuators configured to control environmental properties within the process chamber;

a control system to control rate of catalyst influenced etching across the semiconductor wafer by adjusting the one or more environmental properties via the plurality of actuators; and

a rinsing station to remove the etchant.

60. The apparatus as recited in claim 59, wherein environmental properties include temperature, vapor pressure, electric field, etchant concentration, etchant composition and illumination.

61. The apparatus as recited in claim 59, wherein the rinsing station is the same as the process chamber.

62. The apparatus as recited in claim 59, wherein the rinsing occurs in a separate apparatus.

63. The apparatus as recited in claim 59, wherein the rinsing is done using DI water to remove all the etchant chemicals from the substrate after the etch is completed, and the substrate is dried using dry heated nitrogen or clean dry air.

64. The apparatus as recited in claim 59, further comprising a plurality of sensors to detect the etch state.

65. The apparatus as recited in claim 64, wherein said etch state comprises one or more of the following: an etch depth, a material porosity, number of alternating layers etched, electrical conductivity of doped semiconducting material in contact with an etchant, optical properties of features, and electrical properties of features measured during and/or after the etching process.

66. The apparatus in claim 59, further comprising a send ahead wafer that is processed through the equipment and an offline metrology system to sense etch state of the send ahead wafer.

67. The apparatus of claim 66, wherein the offline metrology estimates process excursions noticed in the send ahead wafer.

68. The apparatus as recited in claim 59, further comprising a drying mechanism configured to transfer fluid to enable a surface tension gradient to prevent collapse of high aspect ratio structures.

69. The apparatus as recited in claim 59 wherein the local and/or global etch depth is monitored using one or more of the following:

local electric field measurements based on voltage, current, capacitance, resistance, or inductance;

optical measurements using cameras, optic cables or spectrophotometers and image processing; or

thermal measurements using thermal chucks or micromirrors.

70. The apparatus as recited in claim 69, wherein the optical measurement is performed at IR wavelength that allows process monitoring through the silicon.

71. The apparatus as recited in claim 59 wherein the local and/or global etch depth is controlled using one or more of the following:

local electrodes to apply AC or DC electric fields of desired waveforms, amplitudes, frequencies, with multiple coinciding electric fields to avoid edge effects and leakage;

local illumination of the front or back of the substrate being etched using laser and light sources of desired wavelengths;

temperature changes in local regions to even out etch depth variations using thermal chucks or micromirrors; or

varying local etchant concentrations using inkjets and jetting blocking or enhancing etchant components or air bubbles to modify etch rates locally.

72. The apparatus as recited in claim 54 wherein the local and/or global etchant concentrations are monitored during catalyst influenced chemical etching using:

refractive index measurement of the etchant solution; or

conductance of the etchant solution.

73. The apparatus as recited in claim 59 wherein the local and/or global etchant concentrations are controlled during catalyst influenced chemical etching using:

flow control and circulation of etchant;

spinning of the substrate;

diffuser to create uniform etchant concentrations;

temperature gradients for diffusion of etchants;

local addition of chemicals to drive diffusion of etchants;

acoustic streaming;

jetting of air; or

local addition of depleting components of etchant.

74. The apparatus as recited in claim 59, comprising components for monitoring and control of local and/or global temperature wherein:

micromirrors are used to heat wafers from front or back;

electrodes are used to locally heat the solution above the die; or

individual “wells” for each die which are filled with finite volume of etchant and pumped out/circulated have controlled temperatures.

75. The apparatus in claim 59, wherein the etchant solution is maintained at low temperatures for near-zero etch rate, and local heating is used to start/control/stop etch per die.

76. The apparatus as recited in claim 59, comprising components for monitoring and control of local and/or global electric fields wherein:

an electric field array mechanism configured to control an etching profile in real-time when an electric bias is applied to a semiconductor substrate; and

an inline electrical metrology and electrochemical etch stop mechanism configured to measure current and voltage across said semiconductor substrate as the etch progresses to determine a number of alternating layers etched in a device or as an etch stop indicator for nanostructure etching.

77. The apparatus as recited in claim 59, comprising components for monitoring and control of local and/or global electric fields wherein:

a patterned bottom electrode is used whose design is based on a catalyst pattern;

electric fields are used for making alternating porous/non-porous layers;

global/local electric fields are used to prevent wandering of catalyst;

the electric fields may have square waveforms at a certain wavelength, frequency and duty cycle;

the electrodes are patterned in the tool on the front or backside of the wafer;

the electrodes are patterned on the front, back, or between the front and back surfaces of a wafers, for instance in an SOIOI wafer;

an electrical contact is made to the wafer using a metal brush with contact outside O-ring;

local variations from edge to center are controlled via pulsed electric fields; or

etch uniformity and depth is monitored across wafer by measurement of I, V, R, C in each local electrode.

78. The apparatus as recited in claim 59 wherein inkjets are configured to dispense etchant fluids on a portion of said semiconducting material.

79. The apparatus as recited in claim 78, wherein said inkjets dispense etchant components at locations that require etching.

80. The apparatus as recited in claim 79, wherein said locations that require etching are isolated by walls of etchant resistant material that includes a patterned photoresist, Cr, polymer, or Al_2O_3, that are later removed.

81. The apparatus as recited in claim 59, wherein the catalyst influenced chemical etching process is done by:

alternately pulsing H_2O_2 vapor and HF vapor;

alternately pulsing H_2O_2 liquid and HF liquid;

alternately pulsing H_2O_2 vapor and HF liquid;

alternately pulsing H_2O_2 liquid and HF vapor; or

using stronger oxidant for porous layers and weaker oxidant for non-porous layers.

82. The apparatus as recited in claim 59 wherein the etchants are in vapor or ionic form, the apparatus comprising:

control of local temperatures using a thermal chuck;

monitoring of vapor pressure of each component; and

applying an electric field in the form of a plasma.

83. The apparatus as recited in claim 59, for catalyst influenced chemical etching arranges all the components for monitoring and control such that:

the setup can etch industry standard wafers or wafers that can go through standard CMOS processes;

the setup provides for automated handling of all substrates, etch components and chemicals;

the components are arranged alongside other portions of the tool and include local and/or global components for electric field monitoring and control;

the components are arranged to accommodate electric field components, inkjets and temperature control components; and

the setup is compatible with the etchant chemicals.

84. A method for making alternating multilayer nanostructures, the method comprising:

providing a semiconducting material;

patterning a catalyst layer on a surface of said semiconducting material;

exposing said patterned catalyst layer to an etchant, wherein said patterned catalyst layer and said etchant cause etching of semiconducting material to form vertical nanostructures;

exposing said semiconducting material to a time-varying electric field to produce alternating layers of etched nanostructures wherein at least one of the alternating layers is porous;

filling a second material in at least a portion of the nanostructures; and

selectively processing one of the alternating layers to either change its chemical composition or remove it.

85. The method as recited in claim 84, wherein the material is single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm deposited on a substrate, an silicon on insulator (SOI) wafer, a layer of epitaxial silicon of thickness greater than 100nm on a substrate.

86. The method as recited in claim 84 wherein said catalyst layer comprises an intended design and lithographic links, wherein said lithographic links substantially connect two or more isolated features of said catalyst layer and/or said semiconducting material.

87. The method as recited in claim 86, wherein said lithographic links have connecting lines that join substantially isolated nodes of said catalyst layer.

88. The method as recited in claim 84, wherein the dimensions of the intended design are corrected for thickness of oxide layer during post-processing of the etched material after SiSE.

89. The method in claim 84, where the pattern is designed using a predefined method to generate the connecting links.

90. The method in claim 84, where the patterns can be lines and spaces, circles, and arbitrary linked patterns.

91. The method in claim 84, that are fabricated using one or more of the following: electron beam lithography, imprint lithography, photolithography, directed self-assembly.

92. The method in claim 91, wherein different electron beam patterns are aligned by photolithography or imprint lithography to form a master pattern.

93. The method in claim 92, wherein the master pattern is replicated onto the semiconducting substrates using imprint lithography.

94. The method in claim 84, wherein the pattern is designed based on 3D NAND Flash cell array architectures.

95. The method in claim 84, wherein the resulting structures with alternating layers are used for subsequent formation of lateral nanowire FETs or nanosheet FETs.

96. The method of claim 86, wherein the links in interconnected high aspect ratio structures are modified by one or more of the following: oxidation, nitridation and selective etch; to provide substantially free-standing semiconducting structures without collapse.

97. The method of claim 87, wherein additional material is filled around the interconnected high aspect ratio structures to make high aspect ratio isolated trenches.

98. The method as recited in claim 84 further comprising:

designing a catalyst pattern to substantially prevent process excursions, wherein said process excursions comprise a collapse of high aspect ratio nanostructures and wandering of isolated catalyst.

99. The method as recited in claim 84, wherein said catalyst layer sinks into the semiconducting substrate in the presence of an etchant.

100. The method as recited in claim 84, wherein said etchant comprises at least two of the following:

fluoride species containing chemicals HF or NH_4F;

oxidants including H_2O_2, $KMnO_4$ or dissolved oxygen;

alcohols including ethanol, isopropyl alcohol, or ethylene glycol; or

protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).

101. The method of claim 84, wherein the semiconducting material can be Ge, GaAs, GaN, Si, SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.

102. The method of claim 84, wherein the catalyst material comprises one or more of the following: Au, Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN, RuO_2, IrO_2, or Graphene.

103. The method as recited in claim 84, wherein an electric field on the semiconducting substrate with modulated current densities as well as a catalyst layer cause periodic portions of the semiconducting substrate to become porous in the presence of the etchant.

104. The method as recited in claim 84, wherein at least one of the alternating layers has a porosity less than 10%.

105. The method as recited in claim 84, wherein at least one of the alternating layers has a porosity less than 1%.

106. The method as recited in claim 84, wherein at least one of the alternating layers has a porosity less than 0.1%.

107. The method as recited in claim 84, wherein the catalyst layer causes periodic portions of the semiconducting substrate adjacent to the catalyst to become porous in the presence of an etchant.

108. The method as recited in claim 84, wherein the porous portions of the semiconducting substrate enhance diffusion of the etchant reactants and products.

109. The method as recited in claim 84, wherein the fabricated structures have at least one lateral dimension that is less than 100nm.

110. The method as recited in claim 84, wherein the fabricated structures have periodic variations in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal processing rates.

111. The method as recited in claim 84, wherein the alternating multilayers have a total thickness greater than 100nm.

112. The method of claim 84, wherein non-collapsing alternating multilayer nanostructures are used for 3D NAND Flash.

113. The method of claim 84, wherein the porous alternating layers have porosities that enable thermal processing without substantial stresses.

114. The method as recited in claim 113 further comprising:

oxidizing said etched material stack such that porous layers of said two or more layers of alternating semiconducting films become completely oxidized and non-porous layers of said two or more layers of alternating semiconducting films develop a thin oxide wall.

115. The method as recited in claim 114, where the non-porous alternating layers have a porosity less than 10%.

116. The method as recited in claim 115, wherein the non-porous layers are resistant to thermal processing with respect to porous layers.

117. The method as recited in claim 115, wherein the non-porous layers are resistant to etchant chemicals used to selectively remove porous layers.

118. The method of claim 113, where the porous alternating layers have porosities that enable oxidation without substantial increase in volumes.

119. The method of claim 113, where the porous alternating layers have porosities that enable nitridation without substantial increase in volumes.

120. The method of claim 113, where material is deposited in specific regions of the high aspect ratio nanostructures by lithography, deposition and etching.

121. The method of claim 120, wherein one of the alternating layers is selectively removed, with an etch selectivity greater than 10:1.

122. The method of claim 120, wherein one of the alternating layers is selectively removed, with an etch selectivity greater than 50:1.

123. The method of claim 120, where a material is deposited to replace the alternating layer that was selectively removed.

124. The method as recited in claim 123, wherein said deposited material for conducting lines comprises one or more of the following: tantalum nitride, tungsten, titanium, cobalt, copper and nickel.

125. The method as recited in claim 123, wherein said deposited material for insulating lines comprises one of the following: silicon dioxide, silicon nitride, low-k dielectrics.

126. The method of claim 120, wherein the alternating layers are of porous and non-porous silicon, and the porous silicon layers are removed using alkaline etchants including TMAH and KOH, or fluoride based chemistries or with fluoride based chemistries and mild oxidants.

127. The method of claim 124, wherein the alternating layers are of a conducting material and non-porous silicon, and the non-porous silicon layers are removed using alkaline etchants including TMAH and KOH, or with fluoride-based chemistries and oxidants.

128. The method of claim 117, wherein the alternating layers are of a porous silicon oxide and non-porous silicon, and the porous silicon oxide layers are removed using fluoride-based etchants in liquid or vapor form, including HF and buffered HF.

129. The method as recited in claim 126 further comprising:

selectively depositing gate and conducting line materials on said non-porous layers and annealed to form silicides for conducting lines.

130. The method as recited in claim 129, wherein said gate and conducting line materials comprise one of the following: tantalum nitride, tungsten, titanium, cobalt and nickel.

131. The method as recited in claim 115 further comprising:

depositing memory film and oxide core filler in channel while protecting word line slits.

132. The method as recited in claim 131, wherein said memory film comprises a tri-layer of silicon oxide, silicon nitride and silicon oxide, and a core of polysilicon with or without doping, and an insulator such as silicon oxide.

133. A method for making substantially non-collapsing alternating multi-layer stacked nanostructures, the method comprising:

creating a material stack comprising two or more layers of alternating semiconducting films, wherein each of said two or more layers of alternating semiconducting films is different from another in at least one of the following properties: material, doping concentration and dopant material;

etching said material stack by catalyst influenced chemical etching such that layers differing in said properties produce etched nanostructures differing in at least one of the following: morphology, porosity, etch rates and thermal processing rates;

filling a second material in at least a portion of the nanostructures; and

selectively processing one of the alternating layers to either change a chemical composition or remove one of the alternating layers.

134. The method of claim 133, wherein the material comprises alternating layers of semiconductor materials, wherein the semiconducting materials have varying doping levels and dopants, highly doped silicon, lightly doped silicon, undoped silicon, doped silicon and germanium, silicon and Si_xGe_{1-x}, differently doped silicon and/or Si_xGe_{1-x}, differently doped silicon and/or Ge, or Si and Ge.

135. The method of claim 133 wherein said catalyst layer comprises an intended design and lithographic links, wherein said lithographic links substantially connect one or more isolated features of said catalyst layer and/or said semiconducting material.

136. The method of claim 135, wherein said lithographic links have connecting lines that join substantially isolated nodes of said catalyst layer.

137. The method of claim 133, wherein the dimensions of the intended design are corrected for thickness of oxide layer during post-processing of the etched material after SiSE.

138. The method of claim 133, wherein the pattern is designed using a predefined method to generate the connecting links.

139. The method of claim 133, wherein the patterns can be lines and spaces, circles, and arbitrary linked patterns.

140. The method of claim 133, that are fabricated using one or more of the following: electron beam lithography, imprint lithography, photolithography, directed self-assembly.

141. The method of claim 140, wherein different electron beam patterns are aligned by photolithography or imprint lithography to form a master pattern.

142. The method of claim 141, wherein the master pattern is replicated onto the semiconducting substrates using imprint lithography.

143. The method of claim 133, wherein the pattern is designed based on 3D NAND Flash cell array architectures.

144. The method of claim 133, wherein the resulting structures with alternating layers are used for subsequent formation of lateral nanowire FETs or nanosheet FETs.

145. The method of claim 135, wherein the links in interconnected high aspect ratio structures are modified by one or more of the following: oxidation, nitridation and selective etch; to provide substantially free-standing semiconducting structures without collapse.

146. The method of claim 136, wherein additional material is filled around the interconnected high aspect ratio structures to make high aspect ratio isolated trenches.

147. The method of claim 133 further comprising:

designing a catalyst pattern to substantially prevent process excursions, wherein said process excursions comprise a collapse of high aspect ratio nanostructures and wandering of isolated catalyst.

148. The method of claim 133, wherein said catalyst layer sinks into the semiconducting substrate in the presence of an etchant.

149. The method of claim 133, wherein said etchant comprises at least two of the following:

fluoride species containing chemicals including HF or NH4F;

oxidants including H_2O_2, $KMnO_4$, or dissolved oxygen;

alcohols including ethanol, isopropyl alcohol, or ethylene glycol; or

protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).

150. The method of claim 133, wherein the semiconducting material can be Ge, GaAs, GaN, Si, SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.

151. The method of claim 133, wherein the catalyst material comprises one or more of the following: Au, Pt, Pd, Ag, Cu, Ni, W, TiN, or Graphene.

152. The method as recited in claim 133, wherein an electric field is used to improve process control and etch uniformity across the substrate.

153. The method of claim 133, wherein at least one of the alternating layers has a porosity less than 10%.

154. The method of claim 133, wherein at least one of the alternating layers has a porosity less than 1%.

155. The method of claim 133, wherein at least one of the alternating layers has a porosity less than 0.1%.

156. The method of claim 133, wherein the catalyst layer causes periodic portions of the semiconducting substrate adjacent to the catalyst to become porous in the presence of an etchant.

157. The method of claim 133, wherein the porous portions of the semiconducting substrate enhance diffusion of the etchant reactants and products.

158. The method of claim 133, wherein the fabricated structures have at least one lateral dimension that is less than 100nm.

159. The method of claim 133, wherein the fabricated structures have periodic variations in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal processing rates.

160. The method of claim 133, wherein the alternating multilayers have a total thickness greater than 100nm.

161. The method of claim 133, where non-collapsing alternating multilayer nanostructures are used for 3D NAND Flash.

162. The method of claim 133, where the porous alternating layers have porosities that enable thermal processing without substantial stresses.

163. The method of claim 162 further comprising:

oxidizing said etched material stack such that porous layers of said two or more layers of alternating semiconducting films become completely oxidized and non-porous layers of said two or more layers of alternating semiconducting films develop a thin oxide wall.

164. The method of claim 163, where the non-porous alternating layers have a porosity less than 10%.

165. The method of claim 164, wherein the non-porous layers are resistant to thermal processing with respect to porous layers.

166. The method of claim 164, wherein the non-porous layers are resistant to etchant chemicals used to selectively remove porous layers.

167. The method of claim 162, where the porous alternating layers have porosities that enable oxidation without substantial increase in volumes.

168. The method of claim 162, where the porous alternating layers have porosities that enable nitridation without substantial increase in volumes.

169. The method of claim 162, where material is deposited in specific regions of the high aspect ratio nanostructures by lithography, deposition and etching.

170. The method of claim 169, wherein one of the alternating layers is selectively removed, with an etch selectivity greater than 10:1.

171. The method of claim 169, wherein one of the alternating layers is selectively removed, with an etch selectivity greater than 50:1.

172. The method of claim 169, where a material is deposited to replace the alternating layer that was selectively removed.

173. The method of claim 172, wherein said deposited material for conducting lines comprises one of the following: tantalum nitride, tungsten, titanium, cobalt, copper and nickel.

174. The method of claim 172, wherein said deposited material for insulating lines comprises one of the following: silicon dioxide, silicon nitride, low-k dielectrics.

175. The method of claim 169, where the alternating layers are of porous and non-porous silicon, and the porous silicon layers are removed using alkaline etchants including TMAH and KOH, with fluoride-based chemistries or with fluoride based chemistries and mild oxidants.

176. The method of claim 173, where the alternating layers are of a conducting material and non-porous silicon, and the non-porous silicon layers are removed using alkaline etchants including TMAH and KOH, or with fluoride-based chemistries and oxidants.

177. The method of claim 166, where the alternating layers are of a porous silicon oxide and non-porous silicon, and the porous silicon oxide layers are removed using fluoride-based etchants in liquid or vapor form, including HF or buffered HF.

178. The method of claim 175, further comprising:

selectively depositing gate and conducting line materials on said non-porous layers and annealed to form silicides for conducting lines.

179. The method of claim 178, wherein said gate and conducting line materials comprise one of the following: tantalum nitride, tungsten, titanium, cobalt and nickel.

180. The method of claim 163 further comprising:

depositing memory film and oxide core filler in channel while protecting word line slits.

181. The method of claim 180, wherein said memory film comprises a tri-layer of silicon oxide, silicon nitride and silicon oxide, and a core of polysilicon with or without doping, and an insulator such as silicon oxide.

182. A method for making alternating multilayer structures, the method comprising:

providing a semiconductor substrate;

etching a semiconductor substrate at taper with an angle less than 80 degrees;

further, catalyst influenced chemical etching of the semiconductor substrate to create alternating layers with different porosities; and

etching said taper to reveal one of said two or more alternating layers while etching part of another layer to create a staircase structure.

183. The method of claim 182, wherein said staircase structure is used to create contacts to conducting layers of a 3D NAND flash device.

184. The method of claim 182, wherein the material is one of the following:
a single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm deposited on a substrate, an silicon on insulator (SOI) wafer, or a layer of epitaxial silicon of thickness greater than 100nm on a substrate.

185. The method of claim 182, wherein the material comprises alternating layers of semiconductor materials and wherein the semiconducting materials include varying doping levels and dopants, two or more layers of alternating semiconducting films comprise silicon and germanium, highly doped silicon/lightly doped silicon or undoped silicon/ doped silicon/germanium.

186. The method of claim 182, wherein the semiconductor material is etched along a crystal plane using a crystallographic dependent etch with an etchant comprising one of the following: KOH, TMAH, NH4OH, EDP.

187. The method of claim 182, wherein the semiconductor material is etched with plasma at an angle to the substrate using faraday cages.

188. The method of claim 182, wherein said staircase structure is used to create contacts to conducting layers of a 3D NAND flash device.

189. The method of claim 182, wherein the minimum thickness of at least one set of the alternating layers is defined by the requirements of lithographic overlay, resistance of the contacts, and lithographic resolution.

190. The method of claim 189, wherein the thickness of the insulating layers is 3 times more than the thickness of the conducting layer.

191. The method of claim 167, wherein the thickness of the insulating layers is 2 times more than the thickness of the conducting layer.

192. A method for improving reliability of catalyst influenced chemical etching, the method comprising:

patterning a catalyst layer on a surface of a semiconducting material, wherein said catalyst layer comprises a plurality of features;

exposing said patterned catalyst layer on said surface of said semiconducting material to a preprocessing step, wherein the preprocessing step is used to modify surface properties of the catalyst surface, the semiconductor surface, and the interface between the catalyst and the semiconductor surface; and

exposing said preprocessed substrate to an etchant, wherein said patterned catalyst layer causes etching of said semiconducting material to form structures corresponding to the plurality of features.

193. The method of claim 192, wherein the preprocessing step comprises exposing the surfaces to one or more of the following chemicals in various dilutions: Vapor HF, Piranha solution, Buffered Oxide Etch, Hydrofluoric acid, Acetone, or Ethanol.

194. The method of claim 192, wherein the preprocessing step comprises exposing the surfaces to a plasma such as oxygen plasma, carbon dioxide plasma, hydrogen plasma, argon or helium plasma.

195. The method of claim 192, wherein the surface properties include surface energy, surface wettability measured by contact angle, interfacial energy.

196. The method of claim 192, wherein the preprocessing step improves the uniformity of the etch by improving surface energy of the catalyst and semiconductor interface.

197. A 3D flash memory device, comprising:

at least twenty layers of active memory arrays;

a gate or a channel with a wall angle greater than 89.5 degrees; and

isolating trenches between blocks of memory wherein the trenches also have a wall angle greater than 89.5 degrees.

198. The 3D flash device of claim 197, wherein the wall angle is measured with respect to the critical feature dimension on the top and bottom of one or more of the following: gate, channel, and isolating trenches.

199. The 3D flash device of claim 198, wherein the critical feature dimension is extracted from a metrology technique including Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), or Atomic Force Microscopy (AFM).

200. A 3D flash memory device, comprising:

at least twenty layers of active memory arrays; and

vertical gates or channels that have a center-to-center distance of less than 120nm.

201. A 3D flash memory device, comprising:

at least twenty layers of active memory arrays; and

vertical gates or channels that have a center-to-center distance of less than 100nm.

202. A 3D flash memory device, comprising:

at least twenty layers of active memory arrays; and

vertical gates or channels that have a center-to-center distance of less than 80nm.

203. A high aspect ratio finFET array, comprising:

fins that have at least an aspect ratio of at least 5:1;

wherein the fins have a wall angle that is greater than 89.5 degrees; and

a base of the fins is surrounded by a dielectric for shallow trench isolation.

204. The high aspect ratio finFET array of claim 203, wherein the fin wall angle is measured with respect to the critical feature dimension on the top of the fin and at the bottom of the fin.

205. The high aspect ratio finFET array of claim 204, wherein the critical feature dimension is extracted from a metrology technique such as Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), or Atomic Force Microscopy (AFM).

206. A high aspect ratio nanosheet FET array, comprising:

fins that have at least an aspect ratio of at least 5:1;

wherein the fin wall angle is greater than 89.5 degrees; and

a base of the nanosheet FET is a fin surrounded by a dielectric for shallow trench isolation.

207. The high aspect ratio nanosheet finFET array of claim 206, wherein the fins comprise lateral layers of semiconducting materials with all around dielectric and gate metals.

208. The high aspect ratio nanosheet finFET array of claim 206, wherein the structure is also defined as nanosheet FETs or lateral nanowire FETs.

209. The high aspect ratio nanosheet finFET array of claim 206, wherein the fin wall angle is measured with respect to the critical feature dimension on the top of the fin and at the bottom of the fin.

210. The high aspect ratio nanosheet finFET array as recited in claim 209, wherein the critical feature dimension is extracted from a metrology technique such as Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), or Atomic Force Microscopy (AFM).

211. A high aspect ratio finFET array, comprising:

fins having a center-to-center distance of 30nm and a height of at least 500nm; and

a base of the fins is surrounded by a dielectric for shallow trench isolation.

212. The high aspect ratio finFET array of claim 211, wherein the fins have a fin wall angle that is greater than 89.5 degrees.

213. The high aspect ratio finFET array of claim 212, wherein the critical feature dimension is extracted from a metrology technique such as Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), or Atomic Force Microscopy (AFM).

214. A method of creating high aspect ratio trenches using catalyst influenced chemical etching, the method comprising:

providing a semiconductor substrate;

catalyst influenced chemical etching of the semiconductor substrate to create high aspect ratio semiconductor holes with a top non-porous layer and one or more bottom porous layers;

depositing material to seal the one or more bottom porous layers; and

depositing material to fill the high aspect ratio holes.

215. The method of claim 214, wherein the top porous layer has a thickness of less than 100nm, and one bottom porous layer has a thickness of more than 200nm.

216. The method of claim 214, wherein the one or more bottom porous layers are selectively oxidized.

217. The method of claim 216, wherein the pores are sealed using silicon oxide deposited using atomic layer deposition.

218. The method of claim 214, wherein the one or more bottom porous layers enable diffusion of etchants between the high aspect ratio holes during CICE.

219. The method of claim 216, wherein the structure is used to make DRAM cells with trench capacitors.

220. The method of claim 216, wherein the structure is used to make FinFETs with the top non-porous structure as the active portion of the fin and the oxidized porous bottom structure acting as shallow trench isolation (STI).

221. The method of claim 216, wherein the structure is used to make Nanosheet FETs with the top structure comprising more than one non-porous and oxidized porous layers, and with the oxidized porous bottom structure acting as shallow trench isolation (STI).