

A NEW DESIGN CONCEPT FOR SRAM READ MARGIN

ABSTRACT

A new method to improve the reading margin in a SRAM memory array is achieved. The method comprises providing an array of SRAM cells. Each SRAM cell has a power supply terminal. A first voltage is forced on the power supply terminal of a first SRAM cell that is selected for reading. A second voltage is forced on the power supply terminal of a second SRAM cell that is not selected for reading. The first voltage does not equal the second voltage. A new SRAM device featuring this method is disclosed.

FIG. 5