

14

1
DYNAMIC MEMORY

2175476

The present invention relates to a dynamic memory.

Japanese Patent Publication No. 39073/1980 discloses a dynamic random-access memory (hereinafter referred to as a DRAM) having folded bit lines.

A system has been proposed for a DRAM in which data is read from memory cells by use of dummy memory cells (also known as dummy cells) of a capacitance approximately half that of the memory cells, i.e., by using dummy cells which have reference capacitors of a capacitance about half that of capacitors used for storing data, (such cells will hereinafter be referred to as half-size dummy cells).

With a memory circuit of this type, a data bit stored in the memory cell is detected by a differential sense amplifier which compares potentials which vary according to the quantity of electric charge stored in the memory cell and the dummy cell.

However, studies conducted by the inventors of the present invention, have shown that it is virtually impossible to manufacture half-size dummy cells with the same precision as that of the memory cells, so that there is a problem of accuracy. On the other hand, it has been found desirable that the dummy cells should be of the same size as the memory cells, i.e., each of the dummy cells should be provided with a reference capacitor of a capacitance substantially equal to that

of the capacitor used for storing data in a memory cell (such cells hereinafter being referred to as full-size dummy cells).

5 A variety of memories have been proposed employing full-size dummy cells, but these waste large quantities of power in the resetting of the dummy cells, and their sensing speed is low.

The present invention seeks to provide a dynamic memory which permits the use of full-size memory cells,
10 but which need not consume as much power as the known dynamic memories with full-size memory cells.

(6)

-3-

According to . . . the present invention there is provided a dynamic memory comprising:

first and second capacitors, a first reference voltage being impressed between electrodes of each
5 capacitor during a first period to store a reference electric charge therein;

a first switching element connected in series with the first capacitor, which is turned on during a second period after the first period has ended, and
10 which remains on during a third period after the second period has ended;

a first node which, when the first switching element is turned on during the second period, is

impressed with a first reference potential corresponding to the reference electric charge from the first capacitor;

5 a second node forming a pair with the first node, and which is impressed with a potential that is to be detected during at least the second period;

a first circuit which applies potentials of complementary levels to the first and second nodes during the third period;

10 a second switching element connected in series with the second node together with the second capacitor, and which is turned on during the third period;

a third node which is impressed with a second reference voltage which is substantially equal to the
15 first reference voltage; and

a switching circuit between the first and second capacitors and the third node, and which connects the first and second capacitors to the third node during a fourth period after the third period
20 has ended;

wherein voltages between the electrodes of the first and second capacitors are set to the first reference voltage by the operation of the switching circuit.

25 Embodiments of the present invention will now be described in detail, by way of example, with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram of dummy memory cells according to a first embodiment of the present invention;

Fig. 2 is a block diagram of a memory array
5 and related circuits;

Fig. 3 is a circuit diagram of a specific configuration of a memory cell, sense amplifier, active-restore circuit, and precharging circuit;

Fig. 4 is a timing chart of the reading
10 operation of the memory;

Fig. 5 is a plan view of the layout of dummy memory cells for use in the first embodiment of the present invention;

Figs. 6 and 7 are sectional views through the
15 dummy cell of Fig. 5, taken along the lines A-A' and B-B' respectively;

Fig. 8 is a circuit diagram of dummy cells according to a second embodiment of the present invention; and

20 Fig. 9 is a plan view of the layout of the dummy cells of the second embodiment.

Embodiment 1:

In the following description, the insulated gate field effect transistors (hereinafter referred to
25 as MOSFETs) used are all of the enhancement type unless stated otherwise. In the drawings, identical or corresponding parts are denoted by the same reference

symbols.

Fig. 1 is a circuit diagram of dummy memory cells according to a first embodiment of the present invention, having a pair of complementary bit lines BLI and $\overline{\text{BLI}}$, and a pair of dummy word lines DWL1 and DWL2. Also shown are n-channel MOSFETs T1 and T2 for reading information from the memory, capacitors C1 and C2 forming dummy memory cells, an n-channel MOSFET T3 for short-circuiting the dummy capacitors (dummy cells) C1 and C2, and nodes A and B.

Preferably a folded bit line system is employed for a memory array MARY shown which will be described in more detail later.

The pair of bit lines BL1 and $\overline{\text{BLI}}$ extend parallel to each other, and are formed as a unitary structure together with bit lines of the memory array MARY.

A first dummy memory cell DS1 connected to the bit line BL1 is formed by the MOSFET T1 and the capacitor C1, and a second dummy memory cell DS2 connected to the bit line $\overline{\text{BLI}}$ is formed by the MOSFET T2 and the capacitor C2.

The dummy memory cells DS1 and DS2 form a pair. The capacitors C1 and C2 have capacitances that are substantially equal to those of the capacitors of the memory cells. The circuit is shown schematically in Fig. 1. It should be understood that, the plates of

the capacitors C1 and C2 which are not connected to nodes A and B, i.e., plates P2 and P4, are connected to earths as shown in Fig. 1. However, earthing the plates P2 and P4 means that they are maintained at a predetermined constant potential. According to a structure that will be described later with reference to Figs. 5 to 7, the plates P2 and P4 of the capacitors C1 and C2 are maintained at the level of the power-source voltage.

10 In Fig. 2, a memory array MARY consists of a plurality of pairs of bit lines BL1 to $\overline{\text{BL}}2$ that extend parallel to one another, a plurality of word lines WL1 to WL4 that extend at right angles to the bit lines, and a plurality of memory cells ML1 to ML8.

15 The memory array MARY has a folded bit line construction and a word line, for example word line WL1, crosses both lines of a pair of bit lines, e.g., crosses both lines of the pair of bit lines BL1 and $\overline{\text{BL}}1$. One memory cell, for example memory cell ML1, is
20 arranged at one of the two intersection points between the word line WL1 and the pair of bit lines BL1 and $\overline{\text{BL}}1$. Preferably the bit lines are formed by electrically-conductive layers that extend over element-forming regions on top of an insulating film and data
25 input/output terminals of two neighbouring memory cells are constructed in common, and are connected to the data line corresponding thereto in order to maximize

the element-forming regions on the semiconductor substrate or reduce the area of the semiconductor substrate. Therefore the memory cells are arranged as shown in Fig. 2. This structure helps to reduce the number of contacts required between the memory cells and the data lines.

Equal numbers of memory cells are connected to each pair of bit lines, in order to make the parasitic capacitance of each bit line the same. Therefore, when one word line is selected, unwanted potential variations or noise imparted to each of the bit lines through the parasitic capacitance between the selected word line and the bit lines that intersect that word line is kept at the same level. In a memory having folded bit lines, the noise imparted to the pairs of bit lines when a word line is selected is virtually ignored by the sense amplifier, since the noise is common mode noise.

Sense amplifiers SA1, SA2, active-restore circuits (or active pull-up circuits) AR1, AR2, and precharging circuits PC1 and PC2, are connected to the pairs of bit lines BL1, $\overline{BL1}$, BL2 and $\overline{BL2}$, respectively, as shown in Fig. 2. Column switches CSW1 and CSW2 are provided between the pairs of bit lines and common bit lines CBL and $\overline{CBL}$, respectively.

The circuit of Fig. 2 is formed on a semiconductor substrate together with various other

circuits (not shown). The result is a memory on the semiconductor substrate.

The memory of this embodiment is of an address multiplex type. Therefore, in addition to the circuits shown in Fig. 2, the semiconductor substrate also supports address buffers, a row address decoder, a word driver which receives an output from the row address decoder and forms word line select signals that are supplied to the word lines WL1 to WL4, a column address decoder which forms select signals that are supplied to the column switches CSW1 and CSW2, a main amplifier which amplifies data signals transmitted via the common bit lines CBL and $\overline{\text{CBL}}$, an output buffer which receives an output from the main amplifier, and dummy word line select circuits which form dummy word line select signals that are supplied to the dummy word lines DWL1 and DWL2. There also is a timing generator which receives a $\overline{\text{RAS}}$ (row address strobe) signal, a $\overline{\text{CAS}}$ (column address strobe) signal, and a $\overline{\text{WE}}$ (write enable) signal, and which forms various timing signals to control the operations of all these circuits. Most of these circuits can be formed in substantially the same manner as those of the memory of a known address multiplex system, it is unnecessary to describe these circuits in detail.

The timing of changes in select signals applied to the dummy word lines DWL1, DWL2 of this

embodiment is slightly different from that of a conventional memory, as will be obvious from the timing chart of Fig. 7. One of the two dummy word lines DWL1 and DWL2 attains the select level at the same time as one of the word lines in the memory array MARY attains the select level, and the other dummy word line attains the select level after the sense amplifiers SA1 and SA2 are operated by the timing signal ϕ_{pa} . The dummy word line select signals can be generated by slightly modifying a delay circuit that receives timing signals ϕ_{pa} , and by slightly modifying the dummy word line select circuit.

Fig. 3 is a circuit diagram of a sense amplifier and memory cells used for reading a dynamic memory according to the first embodiment, having n-channel MOSFETs T6 to T15, complementary bit lines BL1 and $\overline{BL1}$, and capacitors CB1 and CB2 for boosting the bit lines. Also shown are a sense amplifier control signal ϕ_{pa} , a precharging signal ϕ_{pc} , and an active-restore control signal ϕ_{res} compensating for any drop in level of a high-level bit line due to the sensing operation.

The sense amplifier SA1 consists of a pair of MOSFETs T6 and T7 whose gate and drain electrodes are connected in a cross-coupled manner. The operation of the sense amplifier SA1 is controlled by MOSFET T15, the gate of which receives the sense amplifier control signal ϕ_{pa} .

24

The active-restore circuit AR1 consists of MOSFETs T8, T9, T11, T13, and boosting capacitors CB1 and CB2. The boosting capacitors CB1 and CB2 are constructed in substantially the same manner as the MOSFETs, so that each of the boosting capacitors CB1 and CB2 has an electrode (hereinafter referred to as the first electrode) that corresponds to the gate of the MOSFET and an electrode (hereinafter referred to as the second electrode) that corresponds to the source and drain electrodes of the MOSFET. The first electrodes of the capacitors CB1 and CB2 are connected to the MOSFETs T8, T11, T9 and T13, as shown in Fig.

3.

Since the capacitors CB1 and CB2 are constructed in the same manner as the MOSFETs, the capacitors CB1 and CB2 effectively act as variable capacitors. The capacitance between each pair of first and second electrodes is very small if the first electrode is at a low level close to zero. In this case, since the mutual coupling between the first and second electrodes is weak, there is little change in the potential of the first electrode, even when the control signal ϕ_{res} is applied to the second electrode. The capacitance between the first and second electrodes rises to a relatively large value if the first electrode is at a potential which is higher than a threshold voltage thereof. In this case, the potential of the first

electrode changes in response to the control signal ϕ_{res} when it is applied to the second electrode. This means that a selective bootstrap voltage can be formed.

The precharging circuit PC1 consists of pre-
5 charging MOSFETs T12 and T14 between a power-source terminal V_{CC} and bit lines BL1, $\overline{BL1}$, respectively and an equalizing MOSFET T10 provided between the bit line BL1 and the bit line $\overline{BL1}$.

Each of the memory cells ML1 and ML3 consists
10 of an n-channel MOSFET Q_M for selecting the address, and a capacitor C_M for storing data. Electrodes controlled by a selection signal or drain electrodes E1 and E2 of the address selecting MOSFETs, are connected to the bit line BL1 or $\overline{BL1}$, and the gate
15 electrodes are connected to the word line WL3 or WL1. The gate electrodes of the address-selecting MOSFETs act as select terminals of the memory cells, and the electrodes E1 and E2 act as data input/output terminals of the memory cells. In this embodiment, the capacitor
20 C1 of Fig. 1 and the capacitor C_M in the memory cell occupy approximately the same area so that they have approximately the same capacitance. The capacitor C1 in the dummy memory cell and the capacitor C_M in the memory cell are manufactured by the same manufacturing
25 steps, as in a conventional dynamic RAM. This structure enables the capacitors C1 and C_M to have a high degree of relative accuracy.

As is well known, capacitors of an integrated circuit are obtained by repeating a selective processing technique a plurality of times, utilizing a masking film such as photoresist film. In this case, however, the effective electrode areas of the capacitors C_1 and C_M are subject to unwanted variations, depending upon errors in the alignment of the mask. If the size of capacitor C_1 in the dummy memory cell is smaller than that of capacitor C_M , any variation in the capacitance of capacitor C_1 due to a masking error is greater than that of capacitor C_M , so that the relative accuracy of the capacitors C_1 and C_M decreases. On the other hand, when the capacitors C_1 and C_M have nearly the same size, any variation in the capacitance of capacitor C_1 is approximately equal to a similar variation in the capacitance of capacitor C_M , so that the relative accuracy of the capacitors C_1 and C_M is increased sufficiently.

When data is to be read out from the dynamic memory cell, which in this embodiment has one MOSFET per cell, the potential of one of the pair of bit lines is set according to the data stored in the selected memory cell. The potential of the bit line is determined by the distribution of electric charge between the bit line and the selected memory cell. The bit lines of this embodiment have a parasitic capacitance that is much greater than the capacitance of capacitors C_M of the memory cells, as in an

ordinary dynamic RAM. Therefore the selected memory cell imparts only a very small potential change of very small reading voltage amplitude to the bit line. In order to distinguish between high-level and low-level voltages of such small amplitude, the dummy memory cell applies a reference voltage to the other bit line of the pair of bit lines. Thus, the pair of bit lines are precharged by the initial operation of the precharging circuit so that they have the same potential. Then, a small voltage corresponding to the data stored in the memory cell is applied between the pair of bit lines in accordance with starting of selection of the memory cell and the dummy memory cell, and this small voltage is amplified by the sense amplifier.

The reference voltage is determined by the distribution of electric charge between the capacitor in the dummy cell and a bit line to which the capacitor is connected. The reference voltage must be as accurate as possible so that the difference in levels of the pair of bit lines can be amplified sufficiently, and the difference in levels of the pair of bit lines can increase to a predetermined difference within a short period of time when the sense amplifier is operated, or in other words, so that the data can be read out without error at high speed.

Therefore the relative accuracy of the

capacitor in the dummy memory cell and the capacitor in the memory cell must be sufficiently high.

Fig. 4 is a timing chart of the memory circuit of the present invention. The operation of the memory of this embodiment (refer to Figs. 1, 2 and 3) will be described below with reference to the timing chart of Fig. 4.

In the following description, it is assumed for convenience that a word line WL1 supplies a selection address signal to the memory. In other words, an address signal is supplied to select memory cell ML1 connected to bit line BL1. Therefore, when that word line is selected, dummy word line DWL1 is selected such that the reference potential is applied to bit line BL1.

A discharge signal (dummy cell short-circuit signal) $\overline{\phi}_{dc}$ rises when the row address strobe signal $\overline{RAS}$ rises to a high level which is nearly equal to the power-source voltage V_{CC} , so that the switch T_3 in Fig. 1 is turned on. At the same time, the charge stored in the capacitors C1, C2 becomes exactly half that stored in the corresponding memory cell storing a datum of "1", as will be described later. The precharge signal ϕ_{pc} rises to a high level because the $\overline{RAS}$ signal is at a high level. Therefore, the precharging circuits PC1, PC2 operate, and the bit line BL1 or BL2 is precharged to a high level, V_{prc} ,

as shown in Fig. 4G. The precharge level V_{prc} can be considered to be virtually equal to V_{CC} (where V_{CC} is the power-source voltage).

When the RAS signal falls, as shown in Fig. 4A, the precharge signal ϕ_{pc} also falls, so that the operation of the precharging circuits PC1, PC2 stops. In other words, MOSFETs T12, T13 and T10 of Fig. 3 are turned off.

The dummy cell short-circuit signal $\bar{\phi}_{dc}$ falls in synchronism with the fall of the $\overline{RAS}$ signal, as shown in Fig. 4B, turning the switching MOSFET T3 off.

A dummy word line select circuit (not shown) starts to operate in synchronism with the fall of the $\overline{RAS}$ signal. Part of the address signal is supplied to the dummy word line select circuit as a discrimination signal for the memory cell that will be connected to a pair of bit lines. Therefore, when the address signal specifies word line WL1, the potential of the dummy word line DWL1 rises in synchronism with the fall of the $\overline{RAS}$ signal, as shown in Fig. 4C. Since the switching MOSFET T1 is now in the on state, the capacitor C1 in dummy memory cell DS1 is connected to bit line BL1 which has been precharged to a high level. As a result, the potential of the bit line BL1 changes from the precharge level V_{prc} to a reference potential level V_{ref} .

as shown in Fig. 4G.

The timing for selecting the word line WL1 is virtually the same as the timing for selecting the dummy word line DWL1. Therefore, when word line WL1 reaches a high level, the capacitor C_M in the memory cell corresponding to the data line $\overline{BLI}$, which is to be read out, is connected to the data line $\overline{BLI}$ which has been precharged to the high level, V_{prc} . If the data bit written into capacitor C_M of the memory cell ML1 is "0", a read voltage $VR1$ applied to bit line $\overline{BLI}$ drops, when word line WL1 is selected out, as shown in Fig. 4G. Conversely, if the data bit is "1", there is no significant change in potential of the bit line $\overline{BLI}$ from the precharge level V_{prc} .

As will be described later, the voltage previously applied to capacitor $C1$ of dummy memory cell DS1 is equal to $V_{CC}/2$, so that the reference potential V_{ref} has a value which lies between the precharge level V_{prc} and the voltage $VR1$.

After the potentials of the word line WL1 and the dummy word line DWL1 reach a high level, the sense amplifier control signal rises as shown in Fig. 4D. This turns on the sense amplifier power switch $T15$, and the sense amplifier SA1 starts its sensing operation. When this sensing operation starts, the potential of the data line $\overline{BLI}$ rapidly drops to a low level as shown in Fig. 4G, and the potential of the

data line BL1 drops slightly due to the initial sensing operation. In other words, it is preferable that the pair of MOSFETs T6 and T7 of the sense amplifier SA1 are not completely turned on and off immediately after the start of the sensing operation, because the potential difference between the pair of bit lines BL1 and $\overline{BL1}$ is not yet sufficiently great. When this happens the electric charge on the bit line that reaches a high level is discharged through the sense amplifier SA1, and this is undesirable. This unwanted discharge stops when the pair of MOSFETs T6 and T7 are turned on or off completely by the amplification of the potential difference between the pair of bit lines. The active-restore circuit AR1 compensates for any unwanted voltage drop in the bit lines. The potentials of bit lines BL1 and $\overline{BL1}$ are applied to the boosting capacitors CB1 and CB2 in the active-restore circuit AR1 through cutting MOSFETs T11 and T13.

Preferably the restore signal ϕ_{res} and the potential of the dummy word line DWL2 rise almost simultaneously after the sense amplifier control signal ϕ_{PA} rises, as shown in Figs. 4F and 4E.

The boosting capacitor CB1 provides a boosting function since its first electrode is at a high level in response to the rise in potential of the bit line BL1. Therefore, when the restore signal ϕ_{res} is

generated, the potential of the first electrode of the boosting capacitor CB1 rises to a high level that exceeds the power-source voltage V_{CC} . The MOSFET T8 is turned on sufficiently by the boosted voltage
5 applied through the boosting capacitor CB1, so that the potential of the bit line BL1 is restored to a level close to the power-source voltage, as shown in Fig. 4G.

On the other hand, the boosting capacitor CB2
10 has substantially no boosting function since its first electrode is at a low level in response to the low level of the bit line $\overline{BL1}$. There is no significant change in the gate potential of the MOSFET T9, even when the restore signal ϕ_{res} is generated, but remains
15 at low level. Therefore, the potential of bit line $\overline{BL1}$ remains at a low level as shown in Fig. 4G.

The MOSFET T2 in the dummy memory cell DS2 is turned on when the potential of the dummy word line DWL2 rises, as shown in Fig. 4E, so that the
20 capacitor C2 in dummy memory cell DS2 is discharged in response to the potential of the bit line $\overline{BL1}$ having a low level which is close to zero volts. Hence the potential of capacitor C2 (node B of Fig. 1) changes as shown in Fig. 4I, and the potential of capacitor
25 C1 (node A) changes as shown in Fig. 4H.

The potentials of the dummy word line DWL1, the sense amplifier control signal ϕ_{pa} , the dummy

word line DWL2, the word lines corresponding to the selected memory cells, and the restore signal ϕ_{res} fall when the $\overline{RAS}$ signal rises as shown in Fig. 4A. At the same time, the precharging signal ϕ_{pc} rises so
5 that it is ready to perform the next sensing operation.

It is desirable that the dummy cell short-circuit signal $\overline{\phi}_{dc}$ rises in synchronism with the rise of the $\overline{RAS}$ signal after the data read-out, and after the signals on the dummy word lines DWL1 and DWL2
10 have fallen, as shown in Fig. 4B. The short-circuiting MOSFET T3 between the dummy memory cells DS1 and DS2 is turned on when the signal $\overline{\phi}_{dc}$ rises, and in response thereto, the capacitors C1 and C2 in the dummy memory cells DS1 and DS2 are short-circuited. The capacitors
15 C1 and C2 have been charged to a high level which is close to the power-source voltage V_{CC} and to a low level which is close to zero according to the potentials of the bit lines BL1 and $\overline{BL1}$, during the period in which the MOSFETs T1 and T2 were on. Therefore, when the MOSFET T3 is turned on, a charge
20 exactly equal to the precharged $\frac{1}{2}V_{CC}$ is stored in the capacitors C1 and C2.

Repeating this cycle ensures that the dummy capacitors always store a charge which is equal to
25 half the power-source voltage V_{CC} precharged by the preceding reading cycle. In other words, the result is the same as that when a dummy cell of capacity

half that of the memory capacitor is precharged to V_{CC} , i.e., when a half-size dummy cell is precharged to V_{CC} .

Fig. 5 is a diagram which specifically
5 illustrates the layout of the dummy cell. Figs. 6 and 7 are a section taken along the line A-A' of Fig. 5, and a section taken along the line B-B' of Fig. 5, respectively. It is preferable that the device of this embodiment is produced by selective oxidation and
10 self-alignment techniques using polycrystalline silicon layers.

In Figs. 5 to 7, dummy word lines 1a and 1b are formed by parts of a second level polycrystalline silicon layer 7. Also shown are a LOCOS oxide film
15 2, a first level polycrystalline silicon layer 3 that forms one electrode of a capacitor, aluminium layers 4a and 4b that form data lines, a diffusion layer or active region 5, and contacts 6 between the diffusion layer 5 and the aluminium data lines 4a and
20 4b. Another part 7 of the second level polycrystalline silicon layer forms the gate electrode of the short-circuiting MOSFET T3.

The field oxide film 2 has a relatively large thickness and is formed on the main surface of a
25 semiconductor substrate 100 composed of p-type single crystalline silicon where no active region 5 is formed. In Fig. 5, the pattern of the active region 5 is

indicated by broken lines. An insulating film 101 having a small thickness is formed on the surface of the semiconductor substrate 100 where the active region 5 will be formed, to form a gate insulating film for the MOSFETs and a dielectric film for the various capacitors. The first level polycrystalline silicon layer 3, has the pattern indicated by the one dot chain line in Fig. 5, and is formed over the field insulating film 2 and the insulating film 101.

10 A thin oxide film 102 is formed on the surface of the polycrystalline silicon layer 3 by the oxidation thereof, to act as an insulating film. The second level polycrystalline silicon layers 1a, 1b and 7, have patterns indicated by the solid lines in Fig. 5,

15 and are formed on the semiconductor substrate 100. N-type semiconductor regions 103a to 103d are formed on the surface of the semiconductor substrate 100 where the active region 5 will be formed, but at places that are not covered by the first and second

20 level polycrystalline silicon layers, to form source and drain regions for the MOSFETs. These n-type semiconductor regions are formed by implanting impurity ions, using the first and second level polycrystalline silicon layers as masks for the

25 introduction of the impurities.

A silicon oxide film 104 which will act as an intermediate insulating film is also formed on the

main surface of the semiconductor substrate 100.

Aluminium wiring layers 4a and 4b having patterns indicated by the two dotted chain lines in Fig. 5 are formed on the silicon oxide film 104. The aluminium wiring layers 4a and 4b are electrically connected to the n-type semiconductor regions through contact holes 6 formed in the silicon oxide film 104 and the oxide film 101.

In this embodiment, the capacitor in each dummy memory cell consists of the first polycrystalline silicon layer 3, the thin oxide film 101 formed thereunder, and an inversion layer (not shown) that is induced on the surface of the semiconductor substrate 100 when the power-source voltage V_{CC} is applied to the polycrystalline silicon layer 3, in the same way as in the capacitor in a memory cell.

Embodiment 2.

Fig. 8 is a circuit diagram of dummy memory cells in a dynamic memory according to a second embodiment of the present invention. The dummy memory cells have reading n-channel MOSFETs T4 and T5, and there is a feeder line $\frac{1}{2}V_{CC}$ which supplies a potential of half the power-source voltage V_{CC} .

A short-circuiting circuit consisting of the MOSFETs T4, T5 for short-circuiting the dummy cells DS1 and DS2 and the capacitors C1, C2 in the dummy memory cells, according to this embodiment, is

designed so that the memory can be cold-started. A sense amplifier (not shown) may be formed in the same manner as that of the first embodiment, so that Figs. 3 and 4 should be consulted for details of the sense amplifier and the timing chart.

The operation of the memory of the second embodiment of the present invention will be described below in conjunction with these figures. However, the operation of this embodiment is nearly the same as that of the first embodiment, and hence only differences in the operation will be described in detail. When a power-source circuit is closed, a voltage is applied from the $\frac{1}{2}V_{CC}$ feeder line to the dummy capacitors C1, C2 through two separate short-circuiting MOSFETs T4 and T5. The reading operation is initiated in synchronism with the fall of the $\overline{RAS}$ signal. In the second and subsequent reading operations, an electric charge equal to the precharge of $\frac{1}{2}V_{CC}$ has already been stored in the dummy capacitors C1, C2 of Fig. 2 by the preceding reading operation. Therefore virtually no current flows thereto from the $\frac{1}{2}V_{CC}$ feeder line.

The voltage $\frac{1}{2}V_{CC}$ supplied to the $\frac{1}{2}V_{CC}$ line is formed by a voltage generator circuit (not shown) which receives the power-source voltage V_{CC} .

Preferably the voltage generator circuit is formed on the semiconductor substrate together with the various circuits described with reference to the

embodiment of Fig. 1, in order to prevent an increase in the number of external terminals of the memory.

The voltage generator circuit may include, for example, a voltage divider which consists of resistance

5 elements connected in series between the power-source terminal and the ground terminal, and an impedance converter circuit consisting of a source-follower MOSFET which receives the output of the voltage divider.

When a sufficiently low output impedance is
10 required for the voltage generator circuit, there must be a corresponding increase in the size of the MOSFET of the impedance converter circuit.

According to this second embodiment, the precharge level $\frac{1}{2}V_{CC}$ required for the ordinary
15 operational cycles of the memory is obtained by substantially short-circuiting the dummy capacitors C1 and C2 by the MOSFETs T4 and T5. During the ordinary operational cycles of the memory, therefore, the voltage generator circuit needs to produce
20 virtually no driving power. The voltage generator circuit should have a driving power sufficient to precharge the dummy capacitors to the $\frac{1}{2}V_{CC}$ level over a relatively long period of time, between the time when the power-source circuit is closed to the time
25 when the memory starts to operate, so that the voltage generator circuit may have a relatively high output impedance. In other words, the MOSFET of the voltage

generator circuit need have only a relatively small size.

Fig. 9 is a plan view of the layout of dummy cells that corresponds to Fig. 8, reference numerals 1 to 7 denoting the same components as those of Fig. 3. Also shown in Fig. 9 is a diffusion layer 8 that acts as semiconductor wiring for supplying a voltage of $\frac{1}{2}V_{CC}$.

In Fig. 9, active regions 5 have a pattern as indicated by the broken lines. Second level polycrystalline silicon layers 7a and 7b receive the dummy cell short-circuiting signal $\bar{\phi}_{dc}$. First level polycrystalline silicon layers 3a and 3b are not formed over the semiconductor surface between the polycrystalline silicon layers 7a and 7b, so that the n-type semiconductor layer 8 is formed on the surface in the active region 5.

According to this second embodiment, aluminium layers 4a, 4b forming the bit lines are integral with aluminium layers that form bit lines of a memory array (not shown), and are spaced apart by the same pitch as that of those aluminium layers. As shown in Fig. 9, the main portions of the dummy capacitors C_1 and C_2 have a pattern resembling a baseball home base. The pattern of these main portions is substantially the same, and has the same size as that of the memory cells, which are not shown.

Effects

Since the pair of full-size dummy cells connected to the complementary bit lines are short-circuited, each memory capacitor and dummy capacitor may have the same size. Therefore, any capacitance error between the two capacitors can be reduced, regardless of any variations in the capacitors due to the manufacturing process, so that it is possible to provide a memory device of a smaller size.

10 The electric charge stored in the capacitor of the dummy cell during the preceding reading operation may be utilized for the precharging operation of the next reading operation. Such a memory consumes less power than memory devices in which the bit lines are precharged to a level V_{CC} to read data, and then the dummy memory cells are all discharged to a level $\frac{1}{2}V_{CC}$.

20 The sense amplifier responds without delay since the bit lines are precharged to V_{CC} . Therefore, data can be read at a higher speed than in memory devices in which the bit lines are precharged to $\frac{1}{2}V_{CC}$.

25 Since the memory cells and dummy cells are of substantially the same size, the minimum dimensions of the memory may be determined using the memory cells as a reference, and a memory with a high degree of integration may be designed with ease. In other words, when half-size dummy cells are used and an attempt is

41

made to obtain dummy cells of a shape analogous to that of the memory cells, the minimum size is determined by the dummy cells. Therefore, the memory cells must have a large size, reducing the degree of integration.

5 The shape of dummy cells is usually designed using a minimum size which is the same as that of the memory cells. Despite this, it is very difficult to achieve the same variations during the manufacturing process as those affecting the memory cells.

10 Since the capacitance of dummy cells varies only slightly, i.e., since any difference in capacitance relative to a memory cell is small, there is no need to provide a margin to compensate for errors. Therefore the data can be read out at high speed.

15 No additional time is required since the full-size dummy cells are precharged during the restoring of memory cells that are at "1", i.e., since two dummy cells are short-circuited a half charge is distributed during the restoration of memory cells which are holding
20 a data bit "1". Therefore it is possible to provide a memory device that reads data at high speed.

Since a voltage of $\frac{1}{2}V_{CC}$ is always supplied to the dummy cells, no extra reading cycle (dummy cycle) initializing the dummy cells is required when the
25 power-source circuit is closed, so that this dynamic memory device operates normally as soon as the power-source circuit is closed.

The pair of dummy capacitors coupled to the pair of complementary bit lines are short-circuited so that they have a precharge level of $\frac{1}{2}V_{CC}$, and thus almost no current flows to the $\frac{1}{2}V_{CC}$ feeder line during
5 the actual reading operations (the second and subsequent reading cycles after the power-source circuit has been closed). Therefore the areas occupied by the feeder circuit and its wiring may be reduced. For the same reason, almost no current flows to set the
10 initial conditions of the dummy cells, so that the memory device is free from the problem of potential variations in the power-source line due to intermittent currents.

As shown in Fig. 9, the layout of dummy cells
15 may be made almost the same as that of the memory cells, to minimize variations due to the manufacturing process. In the embodiment of Fig. 5, the corresponding dummy cells are arranged aslant for layout reasons, so that their shape is markedly different from that of the
20 memory cells.

The present invention is not limited to the embodiments discussed above, but may be modified in many ways. For instance, the invention can be applied to a dynamic memory having grooves in the memory cells
25 to utilize the MOS capacity of the side surfaces thereof. Also to ensure that the memory devices are not affected by any variations in the manufacturing

43

process, it is desirable that the capacitors C₁ and C₂ in each dummy cell have the same structure as the capacitor C_M in the corresponding memory cell. Preferably all these capacitors are MOS capacitors.

- 5 The present application is divided from UK Patent Application No. 8422521 (published under No. 2149250A) and describes matter which is also described in that application. Attention is therefore drawn to Application No. 8422521.

(44)



CLAIMS:

1. A dynamic memory comprising:
first and second capacitors, a first reference
voltage being impressed between electrodes of each
5 capacitor during a first period to store a reference
electric charge therein;
a first switching element connected in series with
the first capacitor, which is turned on during a second
period after the first period has ended, and which remains
10 on during a third period after the second period has ended;
a first node which, when the first switching element
is turned on during the second period, is impressed with a
first reference potential corresponding to the reference
electric charge from the first capacitor;
15 a second node forming a pair with the first node,
and which is impressed with a potential that is to be
detected during at least the second period;
a first circuit which applies potentials of comple-
mentary levels to the first and second nodes during the
20 third period;
a second switching element connected in series with
the second node together with the second capacitor, and
which is turned on during the third period;
a third node which is impressed with a second
25 reference voltage which is substantially equal to the first
reference voltage; and
a switching circuit between the first and second



45

capacitors and the third node, and which connects the first and second capacitors to the third node during a fourth period after the third period has ended;

wherein voltages between the electrodes of the first
5 and second capacitors are set to the first reference voltage by the operation of the switching circuit.

2. A dynamic memory according to claim 1, wherein the first switching element is between the first node and the first capacitor, and the second switching element is
10 between the second node and the second capacitor.

3. A dynamic memory according to claim 1 or claim 2, wherein the first capacitor and the second capacitor have substantially equal capacitances.

4. A dynamic memory according to any one of the
15 preceding claims, wherein the first circuit has a sense amplifier which amplifies the potential difference between the potential that is to be detected and the first reference potential that is applied to the first and second nodes.

20 5. A dynamic memory according to any one of the preceding claims, wherein the switching circuit has a third switching element between the first capacitor and the third node, and a fourth switching element between the second capacitor and the third node.

25 6. A dynamic memory according to any one of the preceding claims, wherein a plurality of memory cells are provided, each consisting of a third capacitor and a fifth



switching element between the third capacitor and the second node, wherein a potential that is to be detected is applied to the second node from the memory cell.

7. A dynamic memory according to claim 6, wherein the first, second and third capacitors have substantially equal capacitances.

8. A dynamic memory according to claim 6 or claim 7, wherein said first, second and fifth switching elements are insulated gate field-effect transistors.

9. A dynamic memory according to any one of the preceding claims, wherein a precharging circuit is provided to precharge the first and second nodes to the same potential during the first period.

10. A dynamic memory according to claim 9, wherein the precharging circuit has a sixth switching element between a power-source terminal and the first node, and a seventh switching element between the power-source terminal and the second node.

11. A dynamic memory according to claim 9 or claim 10, wherein the precharging circuit has an eighth switching element between the first and second nodes.

12. A dynamic memory according to any one of the preceding claims, wherein an active-restore circuit is connected to the first and second nodes.
