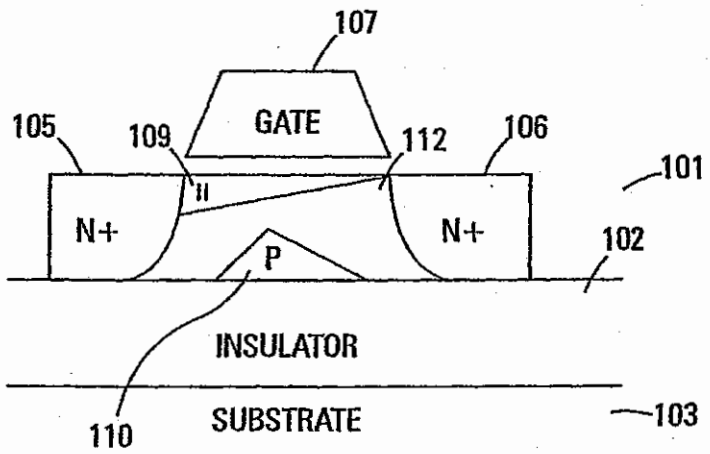


Fig. 1
Prior Art

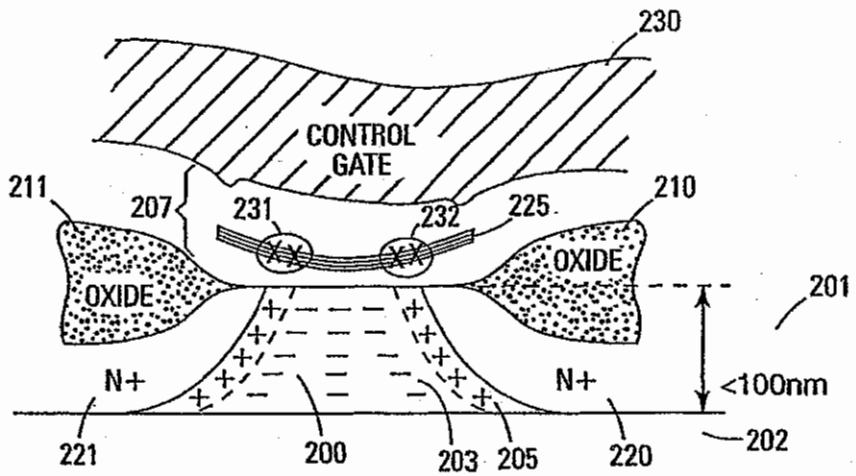

230
CONTROL GATE
211
207
231
232
225
210
OXIDE
OXIDE
201
N+
N+
<100nm
221
200
203
205
220
202

Fig. 2

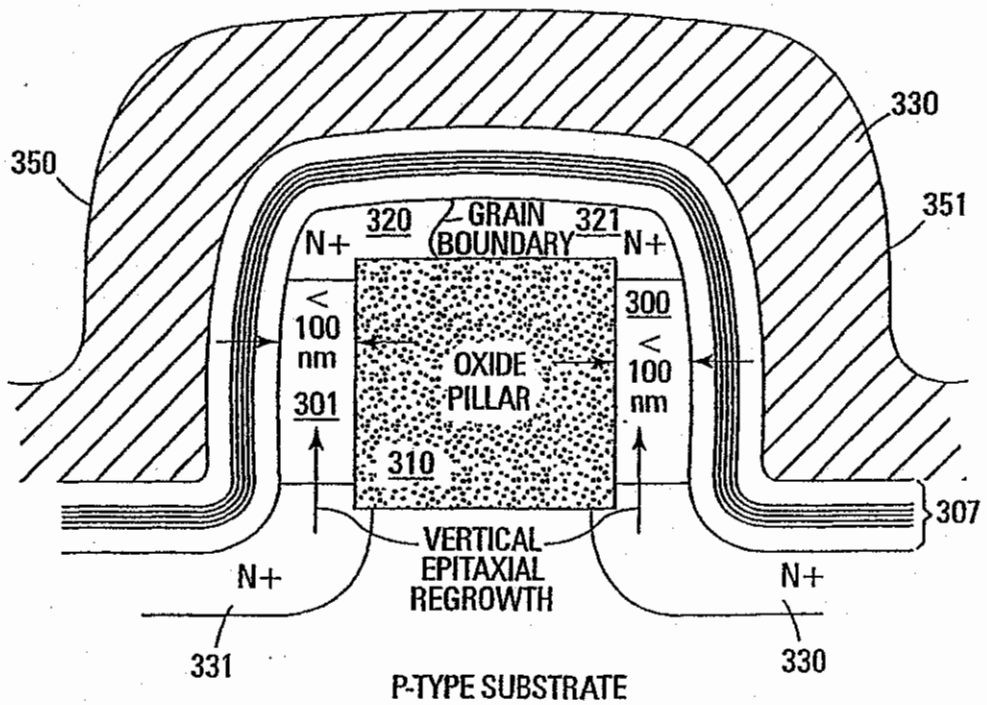

330
350
351
320
GRAIN BOUNDARY
321
N+
N+
300
< 100 nm
OXIDE PILLAR
< 100 nm
301
310
307
VERTICAL EPITAXIAL REGROWTH
N+
N+
331
330
P-TYPE SUBSTRATE

Fig. 3

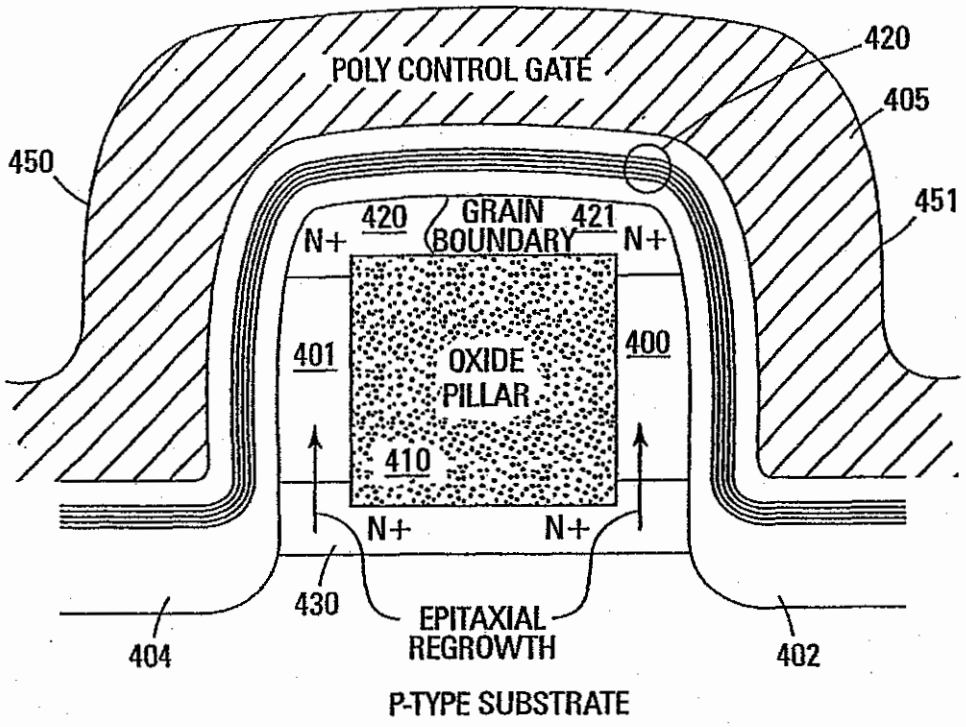

POLY CONTROL GATE
420
405
450
451
N+
420
GRAIN BOUNDARY
421
N+
401
OXIDE PILLAR
400
410
N+
N+
430
EPITAXIAL REGROWTH
404
402
P-TYPE SUBSTRATE

Fig. 4

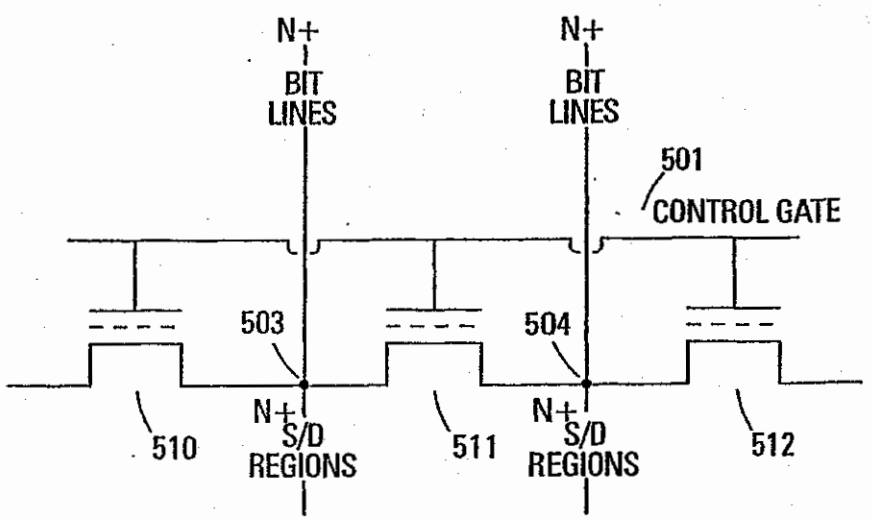

N+
BIT LINES
N+
BIT LINES
501
CONTROL GATE
503
504
510
N+ S/D REGIONS
511
N+ S/D REGIONS
512

Fig. 5

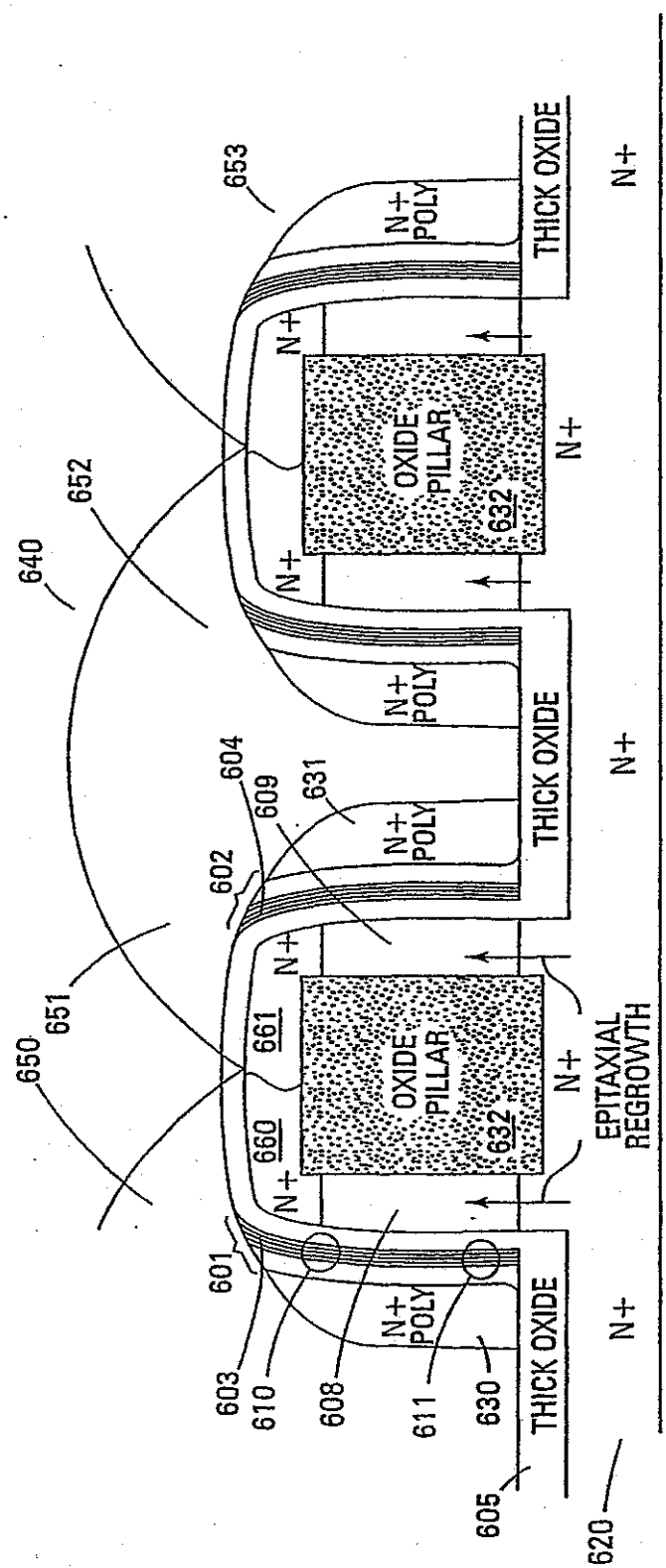

653
652
640
650
651
601
602
603
604
605
608
609
610
611
620
630
631
632
660
661
N+
N+ POLY
THICK OXIDE
OXIDE PILLAR
EPITAXIAL REGROWTH

Fig. 6

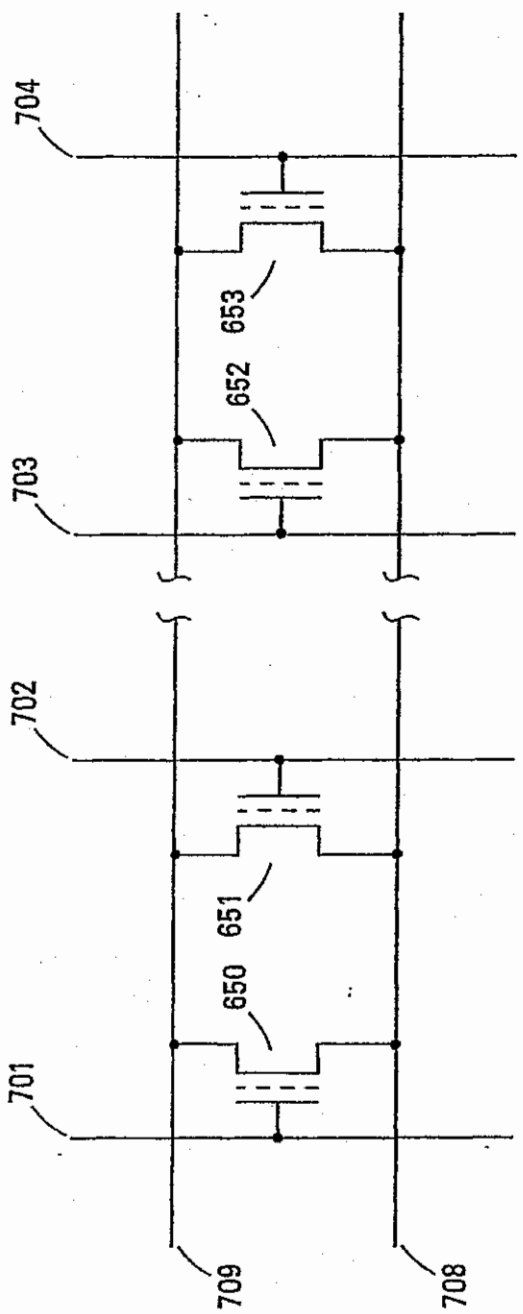


Fig. 7

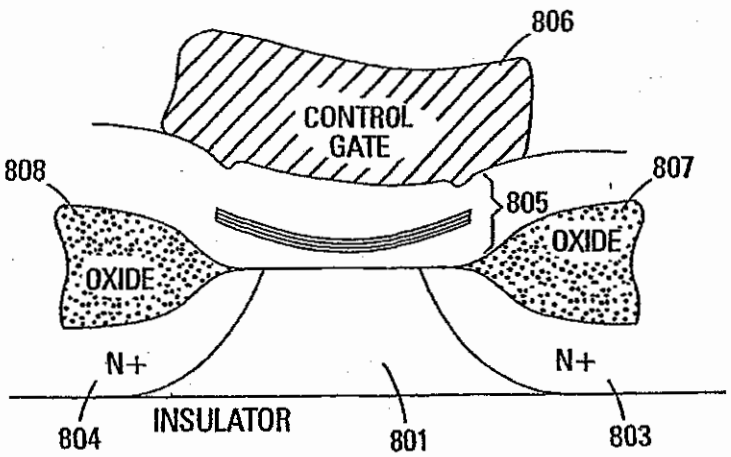

806
CONTROL GATE
808
807
805
OXIDE
OXIDE
N+
N+
INSULATOR
804
801
803

Fig. 8

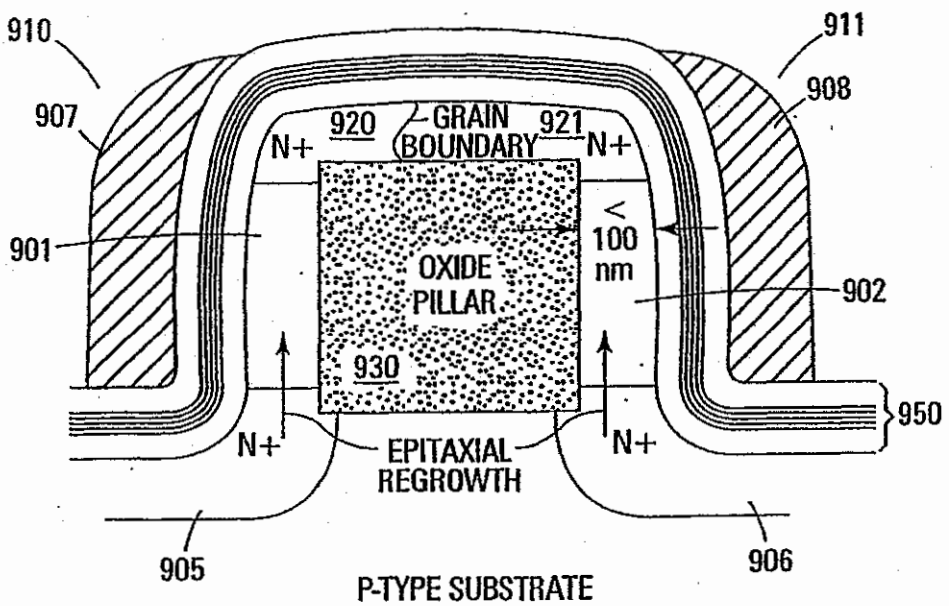

910
911
907
908
920
GRAIN BOUNDARY
921
N+
N+
901
< 100 nm
OXIDE PILLAR
902
930
950
N+
EPITAXIAL REGROWTH
N+
905
906
P-TYPE SUBSTRATE

Fig. 9

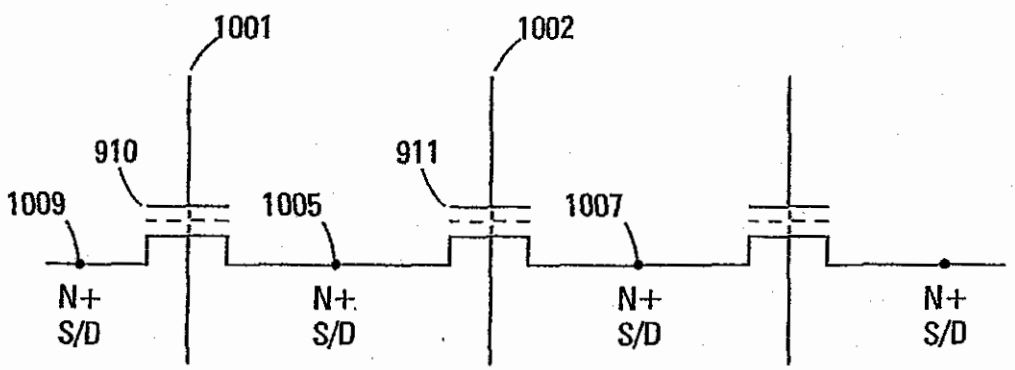


Fig. 10

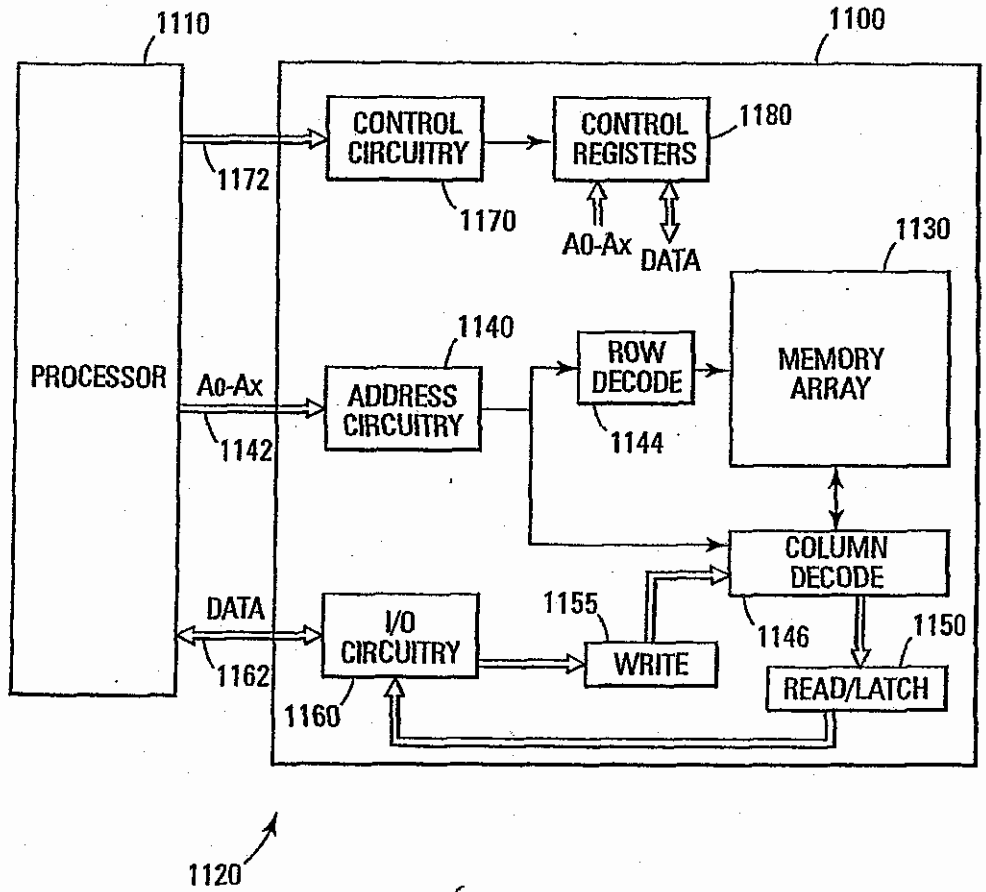

1110
1100
PROCESSOR
CONTROL CIRCUITRY
1172
1170
CONTROL REGISTERS
1180
A0-Ax
DATA
1130
MEMORY ARRAY
1140
A0-Ax
ADDRESS CIRCUITRY
1142
ROW DECODE
1144
COLUMN DECODE
1146
1150
DATA
I/O CIRCUITRY
1162
1160
1155
WRITE
READ/LATCH
1120

Fig. 11