

**AMORPHOUS LAYER EXTREME ULTRAVIOLET LITHOGRAPHY BLANK,
AND MANUFACTURING AND LITHOGRAPHY SYSTEMS THEREFOR**

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of U.S. Provisional Patent Application serial number 61/778,351, filed March 12, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0002] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,307, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0003] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,415, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0004] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,457, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0005] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,507, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

TECHNICAL FIELD

[0006] The present invention relates generally to extreme ultraviolet lithograph blanks, and manufacturing and lithography systems for such extreme ultraviolet lithograph blanks.

BACKGROUND

[0007] Extreme ultraviolet lithography (EUV, also known as soft x-ray projection lithography) is a contender to replace deep ultraviolet lithography for the manufacture of 0.13 micron, and smaller, minimum feature size semiconductor devices.

[0008] However, extreme ultraviolet light, which is generally in the 5 to 40 nanometer wavelength range, is strongly absorbed in virtually all materials. For that reason, extreme

ultraviolet systems work by reflection rather than by transmission of light. Through the use of a series of mirrors, or lens elements, and a reflective element, or mask blank, coated with a non-reflective absorber mask pattern, the patterned actinic light is reflected onto a resist-coated semiconductor wafer.

[0009] The lens elements and mask blanks of extreme ultraviolet lithography systems are coated with reflective multilayer coatings of materials such as molybdenum and silicon. Reflection values of approximately 65% per lens element, or mask blank, have been obtained by using substrates that are coated with multilayer coatings that strongly reflect light essentially at a single wavelength within a extremely narrow ultraviolet bandpass; e.g., 12 to 14 nanometer bandpass for 13 nanometer ultraviolet light.

[0010] There are various classes of defects in semiconductor processing technology which cause problems. Opaque defects are typically caused by particles on top of the multilayer coatings or mask pattern which absorb light when it should be reflected. Clear defects are typically caused by pinholes in the mask pattern on top of the multilayer coatings through which light is reflected when it should be absorbed. And phase defects are typically caused by scratches and surface variations beneath the multilayer coatings which cause transitions in the phase of the reflected light. These phase transitions result in light wave interference effects which distort or alter the pattern that is to be exposed in the resist on the surface of the semiconductor wafer. Because of the shorter wavelengths of radiation which must be used for sub-0.13 micron minimum feature size, scratches and surface variations which were insignificant before now become intolerable.

[0011] While progress has been made in reducing or eliminating particle defects and work has been done on repair of opaque and clear defects in masks, to date nothing has been done to address the problem of phase defects. For deep ultraviolet lithography, surfaces are processed to maintain phase transitions below 60 degrees. Similar processing for extreme ultraviolet lithography is yet to be developed.

[0012] For an actinic wavelength of 13 nanometers, a 180 degree phase transition in the light reflected from the multilayer coating may occur for a scratch of as little as 3 nanometers in depth in the underlying surface. This depth gets shallower with shorter wavelengths. Similarly, at the same wavelength, surface variations more abrupt than one (1) nanometer rise over one hundred (100) nanometers run may cause similar phase transitions. These phase transitions can cause a phase defect at the surface of the semiconductor wafer and irreparably damage the semiconductor devices.

[0013] In the past, mask blanks for deep ultraviolet lithography have generally been of glass but silicon or ultra low thermal expansion materials have been proposed as alternatives for extreme ultraviolet lithography. Whether the blank is of glass, silicon, or ultra low thermal expansion material, the surface of the mask blank is made as smooth as possible by such processes a chemical mechanical polishing, magneto-rheological finishing, or ion beam polishing. The scratches that are left behind in such a process are sometimes referred to as "scratch-dig" marks, and their depth and width depend upon the size of the particles in the abrasive used to polish the mask blank. For visible and deep ultraviolet lithography, these scratches are too small to cause phase defects in the pattern on the semiconductor wafer. However, for extreme ultraviolet lithography, scratch-dig marks are a significant problem because they will appear as phase defects.

[0014] Due to the short illumination wavelengths required for EUV lithography the pattern masks used must be reflective mask instead of the transmissive masks used in current lithography. The reflective mask is made up of a precise stack of alternating thin layers of molybdenum and silicon, which creates a Bragg refractor or mirror. Because of the nature of the multilayer stack and the small feature size, any imperfections in the surface of the substrate on which the multilayer stack is deposited will be magnified and impact the final product. Imperfections on the scale of a few nanometers can show up as printable defects on the finished mask and need to be eliminated from the surface of the mask blank before deposition of the multilayer stack.

[0015] Mask blanks are a critical item for the adoption of EUV lithography. The main hurdles relate to defectivity and the reflectance of the mask blank. The mask has a Bragg reflector of 80 alternating layers of molybdenum (Mo) and silicon (Si) deposited on it. The roughness of this layer stack is critical and relates to line edge roughness on the printed wafer.

[0016] The need to reduce costs, improve efficiencies and performance, and meet competitive pressures adds an even greater urgency to the critical necessity for finding answers to these problems.

[0017] Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

SUMMARY

[0018] An embodiment of the present invention provides an integrated extreme ultraviolet blank production system includes: a vacuum chamber for placing a substrate in a vacuum; a deposition system for depositing a multi-layer stack without removing the substrate from the vacuum; and a treatment system for treating a layer on the multi-layer stack to be deposited as an amorphous metallic layer.

[0019] An embodiment of the present invention provides a physical vapor deposition chamber for manufacturing extreme ultraviolet mask blanks includes: a target, comprising molybdenum alloyed with boron.

[0020] An embodiment of the present invention provides an extreme ultraviolet lithography system includes: an extreme ultraviolet light source; a mirror for directing light from the extreme ultraviolet light source; a reticle stage for placing an extreme ultraviolet mask blank with a multi-layer stack having an amorphous metallic layer; and a wafer stage for placing a wafer.

[0021] An embodiment of the present invention provides an extreme ultraviolet blank includes: a substrate; a multi-layer stack having an amorphous metallic layer; and capping layers over the multi-layer stack.

[0022] Certain embodiments of the invention have other elements in addition to or in place of those mentioned above. The steps or element will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] FIG. 1 is an integrated extreme ultraviolet (EUV) mask production system.

[0024] FIG. 2 is a EUV mask blank in accordance with an embodiment of the present invention.

[0025] FIG. 3 is the EUV mask blank in an intermediate stage of manufacture.

[0026] FIG. 4 is the EUV mask blank in an intermediate stage of manufacture.

[0027] FIG. 5 is an optical train for a EUV lithography system.

[0028] FIG. 6 is a EUV lithography system.

DETAILED DESCRIPTION

[0029] The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention. It is to be understood that other embodiments would be evident based on the present disclosure, and that system, process, or mechanical changes may be made without departing from the scope of the present invention.

[0030] In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known circuits, system configurations, and process steps are not disclosed in detail.

[0031] The drawings showing embodiments of the system are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the drawing FIGs. Similarly, although the views in the drawings for ease of description generally show similar orientations, this depiction in the FIGs. is arbitrary for the most part. Generally, the invention can be operated in any orientation.

[0032] Where multiple embodiments are disclosed and described having some features in common, for clarity and ease of illustration, description, and comprehension thereof, similar and like features will be described with similar reference numerals.

[0033] For expository purposes, the term “horizontal” as used herein is defined as a plane parallel to the plane or surface of a mask blank, regardless of its orientation. The term “vertical” refers to a direction perpendicular to the horizontal as just defined. Terms, such as “above”, “below”, “bottom”, “top”, “side” (as in “sidewall”), “higher”, “lower”, “upper”, “over”, and “under”, are defined with respect to the horizontal plane, as shown in the figures. The term “on” indicates that there is direct contact between elements.

[0034] The term “processing” as used herein includes deposition of material or photoresist, patterning, exposure, development, etching, cleaning, and/or removal of the material or photoresist as required in forming a described structure.

[0035] Embodiments of the present invention use various established techniques for depositing silicon, silicon oxide, and related layers of compatible thermal expansion coefficient by CVD, PVD, ALD, and flowable CVD to fill the pits and bury the defects. Once deposited, the layer's surface maybe smooth and flat enough for further multilayer stack deposition, or may then be smoothed further using a variety of established smoothing or polishing techniques, including CMP, annealing, or ion beam polishing.

[0036] Referring now to FIG. 1, therein is shown an integrated extreme ultraviolet (EUV) mask blank production system 100. The integrated EUV mask blank production system 100 includes a mask blank loading and carrier handling system 102 into which mask blanks 104 are loaded. An airlock 106 provides access to a wafer handling vacuum chamber 108. In the embodiment shown, the wafer handling vacuum chamber 108 contains two vacuum chambers, a first vacuum chamber 110 and a second vacuum chamber 112. Within the first vacuum chamber 110 is a first wafer handling system 114 and in the second vacuum chamber 112 is a second wafer handling system 116.

[0037] The wafer handling vacuum chamber 108 has a plurality of ports around its periphery for attachment of various other systems. The first vacuum chamber 110 has a degas system 118, a first physical vapor deposition system 120, a second physical vapor deposition system 122, and a preclean system 124.

[0038] The second vacuum chamber 112 may have various treatment systems, such as a first multi-cathode source 126, a flowable chemical vapor deposition (FCVD) system 128, a cure system 130, and a second multi-cathode source 132, connected to it.

[0039] The first wafer handling system 114 is capable of moving wafers, such as a wafer 134, among the airlock 106 and the various systems around the periphery of the first vacuum chamber 110 and through slit valves in a continuous vacuum. The second wafer handling system 116 is capable of moving wafers, such as a wafer 136, around the second vacuum chamber 112 while maintaining the wafers in a continuous vacuum.

[0040] Referring now to FIG. 2, therein is shown a EUV mask blank 200 in accordance with an embodiment of the present invention. The EUV mask blank 200 has an ultra-low thermal expansion substrate 202 of glass, silicon, or other ultra-low thermal expansion material. The ultra-low thermal expansion materials include fused silica, fused quartz, calcium fluoride, silicon carbide, silicon oxide-titanium oxide alloy, or other material having a thermal coefficient of expansion within the range of these materials.

[0041] The top surface of the ultra-low expansion substrate 202 has imperfections 203, such as pits, scratches, and particles, which result from chemical mechanical polishing (CMP) with an abrasive. The scratches that are left behind in such a process are sometimes referred to as "pits" and/or "scratch-dig" marks, and their depth and width depend upon the size of the particles in the abrasive used to polish the EUV mask blank 200.

[0042] It has been discovered that the imperfections in the EUV mask blank 200 can be eliminated by deposition of a planarization layer 204. The planarization layer 204, or

flowable film, can be formed by depositing a flowable CVD film or depositing silicon, silicon oxide, or related films by CVD, PVD, or similar processes over the ultra-low expansion substrate 202. This step buries particles and other defects that are on the ultra-low expansion substrate 202.

[0043] In the case of flowable CVD films, no further processing may be required to achieve an acceptably smooth, flat surface 205 over the ultra-low expansion substrate 202. For silicon, silicon oxide, or related films, smoothing after deposition may be required. This smoothing can be done by a variety of polishing methods including, but not limited to CMP, chemical polishing, ion beam polishing or annealing. These smoothing techniques can also be applied to the flowable CVD film if further smoothing is required.

[0044] A multi-layer stack 206 is formed above the planarization layer 204 to form a Bragg reflector. Due to the transmissive nature of the optics and illuminating wavelengths used in EUV, reflective optics are used and the multi-layer stack 206 may be made of alternating layers of high-Z and low-Z materials, such as molybdenum and silicon, which form a reflector.

[0045] A capping layer 208 is formed above the multi-layer stack 206. The capping layer can be a material such as ruthenium (Ru) or a non-oxidized compound thereof to help protect the multi-layer stack 206 from oxidation and any chemical etchants to which the EUV mask blank 200 may be exposed during mask processing. Other material such as titanium nitride, boron carbide, silicon nitride, ruthenium oxide, and silicon carbide may also be used in the capping layer 208.

[0046] An absorber layer 210 is placed over the capping layer 208. The absorber layer 210 is of a material having a high absorption coefficient for a particular frequency of EUV light (about 13.5 nm) and may be a material such chromium, tantalum or nitrides thereof.

[0047] An anti-reflective coating (ARC) 212 is deposited over the absorber layer 210. The ARC 212 can be of a material such as tantalum oxynitride or tantalum boron oxide.

[0048] A backside chucking layer 214 is formed over the rear surface of the ultra-low expansion substrate 202 for chucking the substrate on or with an electrostatic chuck (not shown).

[0049] Referring now to FIG. 3, therein is shown the EUV mask blank 200 in an intermediate stage of manufacture.

[0050] During deposition of the multi-layer stack 206, the metallic layer 300 can be alloyed. It has been discovered that an alloyed deposition 302 can prevent the metallic layer 300 from

being deposited as a polycrystalline layer. Instead, the metallic layer 300 can be maintained as an amorphous metallic layer 300.

[0051] For example, the alloyed deposition 302 can be performed in the second vacuum chamber 112 of FIG. 1 where the first multi-cathode source 126 is a boron alloyed molybdenum target and the second multi-cathode source 132 is a silicon target. The first multi-cathode source 126 and the second multi-cathode source 132 are angled with respect to a rotatable pedestal adapted to receive the substrate 202. Boron alloying will maintain the molybdenum in an amorphous state. By maintaining an amorphous phase in the metallic layer 300, the overall roughness of the multi-layer stack 206 is improved by having better EUV reflectivity with less flare than without the molybdenum in the amorphous state.

[0052] In an alternative method, it has been discovered that a gas 304, such as nitrogen, can be added to the sputter gas to disrupt the structure of the deposited molybdenum to also form an amorphous phase in the metallic layer 300.

[0053] Referring now to FIG. 4, therein is shown the EUV mask blank 200 in an intermediate stage of manufacture. The EUV mask blank 200 is held on a treatment system, such as an electrostatic chuck 404 with cooling passages 406. The electrostatic chuck 404 is the rotatable pedestal adapted to receive the substrate 202.

[0054] An ion beam, plasma, or magnetron sputtering tool 132 is used to deposit the multi-layer stack over the substrate. The silicon layer is deposited as an amorphous layer, while the molybdenum layer is polycrystalline. This morphology causes higher surface roughness of the molybdenum layer which then propagates through the stack. To achieve the required smoothness of the film stack ion beam polishing is at times employed to decrease roughness. This is a cumbersome process flow that does not meet the productivity requirements.

[0055] It has been shown in Magnetic RAM (MRAM) that B-alloying can prevent a CoFe layer from depositing as a polycrystalline layer. The B-alloyed layer also exhibits lower roughness.

[0056] It has been found that the same concept may be applied to the molybdenum deposition by using an alloyed molybdenum target. By maintaining an amorphous phase in the molybdenum layer the overall roughness of the multi-layer stack improves and leads to better EUV reflectivity with less flare. Examples of such alloying materials are boron and carbon. Another possibility is to add a small amount of nitrogen to the sputter gas to disrupt the structure of the deposited molybdenum.

[0057] Another technique that has been found that can be employed to suppress grain growth in the molybdenum layer is to cool the substrate to low temperatures. This can be accomplished by pre-cooling the substrate prior to deposition and actively cooling the substrate during the deposition process using water or gas cooling.

[0058] By maintaining an amorphous phase in the molybdenum layer the overall roughness of the multi-layer stack is improved and leads to better EUV reflectivity with less flare. An example of such alloying is boron. Another possibility is to add a small amount of nitrogen to the sputter gas to disrupt the structure on the deposited molybdenum layer.

[0059] Another technique that can be employed to suppress grain growth in the molybdenum layer is to cool the substrate to low temperatures. This can be accomplished by pre-cooling the substrate prior to deposition and actively cooling the substrate during the deposition process.

[0060] The resulting method and system is straightforward, cost-effective, uncomplicated, highly versatile and effective, can be surprisingly and unobviously implemented by adapting known technologies, and are thus readily suited for efficiently and economically manufacturing EUV mask blanks.

[0061] An advantage of this method is that it is substrate independent and so it can be used on a variety of substrates and qualities of substrates. It has the potential to make it possible to use glass substrates that have the required properties for EUV blanks but do not have atomically flat, smooth surfaces after polishing. This independence makes it possible to use different substrate suppliers and minimizes the impact of unexpected changes to the substrate preparation and polishing by the suppliers.

[0062] Embodiments of the invention provide an atomically flat, low defect, smooth surface for an EUV mask blank. However, embodiments of the invention could also be used to manufacture other types of blanks, such as for mirrors. Over a glass substrate, embodiments of the invention can be used to form an EUV mirror. Further, embodiments of the invention can be applied to other atomically flat, low defect, smooth surface structures used in UV, DUV, e-beam, visible, infrared, ion-beam, x-ray, and other types of semiconductor lithography. Embodiments of the invention can also be used in various size structures that can range from wafer-scale to device level and even to larger area displays and solar applications.

[0063] Another important aspect of the present invention is that it valuably supports and services the historical trend of reducing costs, simplifying systems, and increasing performance.

[0064] These and other valuable aspects of the present invention consequently further the state of the technology to at least the next level.

[0065] It has been discovered that an amorphous phase can be formed in the metallic layer 400 by cooling the ultra-low expansion substrate 202 during deposition of the multilayer stack 206. The cooling of the multi-layer stack 206 suppresses grain growth in the molybdenum layer. This grain growth is suppressed by precooling the ultra-low expansion substrate 202 and actively cooling the ultra-low expansion substrate 202 during the deposition process using water.

[0066] Referring now to FIG. 5, therein is shown an optical train 500 for a EUV lithography system. The optical train 500 has a plasma source 502 for creating the EUV light and collecting it in a collector 504. The collector 504 provides the light to a field facet mirror 508 which is part of an illuminator system 506 which further includes a pupil facet mirror 510. The illuminator system 506 provides the EUV light to a reticle 512 (which is the fully processed version of the mask blank 104 of FIG. 1), which reflects the EUV light through projection optics 514 and onto a wafer 516.

[0067] Referring now to FIG. 6, therein is shown a EUV lithography system 600. The EUV lithography system 600 includes a EUV light source area 602, a reticle stage 604 and a wafer stage 606 as adjuncts to the optical train 600. The reticle stage 604 supports the reticle 512 of FIG. 5, which is the fully processed version of the mask blank 104 of FIG. 1.

[0068] It has been found that the EUV mirror 508 and the EUV mask blank 104 permit the EUV lithography system 600 to overcome many of the hurdles facing the production of ultra-miniaturized integrated circuits on die and wafers.

[0069] While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the scope of the included claims. All matters hithertofore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

CLAIMS

1. An integrated extreme ultraviolet blank production system comprising:
a vacuum chamber for placing a substrate in a vacuum;
a deposition system for depositing a multi-layer stack without removing the substrate from the vacuum; and
a treatment system for treating a layer on the multi-layer stack to be deposited as an amorphous metallic layer.
2. The system as claimed in claim 1 wherein the treatment system includes an alloyed deposition of the amorphous metallic layer.
3. The system as claimed in claim 1 wherein the treatment system provides a gas to disrupt a crystalline structure of the amorphous metallic layer.
4. The system as claimed in claim 1 wherein the treatment system cools the multi-layer stack to suppress grain growth of the amorphous metallic layer.
5. The system as claimed in claim 1 wherein the deposition system includes a magnetron for sputtering the multi-layer stack.
6. The system as claimed in claim 1 further comprising a second deposition system is for depositing additional layers to form an extreme ultraviolet mask blank.
7. The system as claimed in claim 1 further comprising a second deposition system is for depositing additional layers to form an extreme ultraviolet mirror.
8. A physical vapor deposition chamber for manufacturing an extreme ultraviolet blank comprising:
a target, comprising molybdenum alloyed with boron.
9. The chamber of claim 8 further comprising:
a second target, comprising silicon.
10. The chamber of claim 9 wherein the target and the second target are angled with respect to a pedestal adapted to receive a substrate.

11. The chamber of claim 8 further comprising a rotating pedestal adapted to receive a substrate.
12. An extreme ultraviolet lithography system comprising:
an extreme ultraviolet light source;
a mirror for directing light from the extreme ultraviolet light source;
a reticle stage for placing an extreme ultraviolet mask blank with a multi-layer stack
having an amorphous metallic layer; and
a wafer stage for placing a wafer.
13. The system as claimed in claim 12 wherein the amorphous metallic layer is alloyed to form the amorphous metallic layer.
14. The system as claimed in claim 12 wherein the amorphous metallic layer has a disrupted crystalline structure to form the amorphous metallic layer.
15. The system as claimed in claim 12 wherein the amorphous metallic layer has suppressed grain growth to form the amorphous metallic layer.
16. A method of making an extreme ultraviolet blank comprising:
providing a substrate;
forming a multi-layer stack having an amorphous metallic layer over the substrate; and
forming capping layers over the multi-layer stack.
17. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer forms an alloyed amorphous metallic layer.
18. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer deposits the amorphous metallic layer by sputtering the metal with an alloy.
19. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer deposits the amorphous metallic layer by sputtering while cooling the substrate.
20. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer forms the amorphous metallic layer alloyed with boron, nitrogen, or carbon.

21. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer forms the amorphous metallic layer of amorphous molybdenum.

22. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer forms the amorphous metallic layer of a disrupted crystalline structure.

23. The method as claimed in claim 16 wherein forming the multi-layer stack having the amorphous metallic layer forms the amorphous metallic layer having suppressed grain growth.

24. The method as claimed in claim 16 wherein forming the multi-layer stack forms an extreme ultraviolet mask blank.

25. The method as claimed in claim 16 wherein forming the multi-layer stack forms an extreme ultraviolet mirror.

26. The method as claimed in claim 16 wherein providing the substrate provides a substrate of an ultra-low thermal expansion material.

27. The method as claimed in claim 16 wherein providing the substrate provides a substrate of glass.