address A0 is initiated at time T0, data D0 is obtained at time T3 after three clock cycles. In the next clock cycle T4, the address A1 of the next node is obtained according to the data D0, a read command is initiated, and then it still takes another three clock cycles to obtain the next piece of data D1. In FIG. 2, one piece of data is read every four clock cycles on average. Such performance is not enough for many designs with high bandwidth requirements. In these designs, it usually requires reading one piece of data in one clock cycle. The system clock of 1GHz and the data width of 512bits are taken as an example. If one piece of data is read every four clock cycles, the system bandwidth is only 128Gbps; if one piece of data is read every one clock cycle, the system bandwidth may reach 512Gbps.

SUMMARY

[0005] The purpose of the present invention is to provide a linked list data structure and a data processing method thereof, a computer-readable storage medium, and an electronic device.

[0006] In order to achieve the above purpose, according to the first aspect of the present invention, a linked list data structure is provided, including: a Random Access Memory (RAM), a free address management unit, and a multi-head linked list; the multi-head linked list comprises a control unit, a write operation sub-link indicator unit, a read operation sub-link indicator unit, and n sub-links, where n is a positive integer greater than or equal to 2; the n sub-links each comprise a sub-link length unit, a write pointer unit, and a read pointer unit; the RAM comprises a plurality of data units, and a plurality of pointer storage units corresponding to the plurality of data units in a one-to-one correspondence, wherein one data unit and one corresponding pointer storage unit share one address in the RAM;

[0007] the plurality of data units are configured to store data;

[0008] the plurality of pointer storage units are configured to store addresses, in which one data unit is configured to store the *i*-th piece of data of one sub-link, one pointer storage unit corresponding to the one data unit is configured to store an address of a data unit where the (*i*+1)-th piece of data of the one sub-link is located;

[0009] the free address management unit is configured to manage free addresses in the RAM, and output one free address to the control unit when receiving a free address reading request from the control unit;

CLAIMS

1. A linked list data structure, comprising: a Random Access Memory (RAM), a free address management unit, and a multi-head linked list; wherein

the multi-head linked list comprises a control unit, a write operation sub-link indicator unit, a read operation sub-link indicator unit, and *n* sub-links, where *n* is a positive integer greater than or equal to 2; the *n* sub-links each comprise a sub-link length unit, a write pointer unit, and a read pointer unit; the RAM comprises a plurality of data units, and a plurality of pointer storage units corresponding to the plurality of data units in a one-to-one correspondence, wherein one data unit and one corresponding pointer storage unit share one address in the RAM;

the plurality of data units are configured to store data;

the plurality of pointer storage units are configured to store addresses, wherein one data unit is configured to store the *i*-th piece of data of one sub-link, one pointer storage unit corresponding to the one data unit is configured to store an address of a data unit where the (*i*+1)-th piece of data of the one sub-link is located;

the free address management unit is configured to manage free addresses in the RAM, and output one free address to the control unit when receiving a free address reading request from the control unit;

the write operation sub-link indicator unit is configured to store a sub-link number of a write target sub-link, wherein the write target sub-link is a sub-link into which to-be-written data is to be written;

the read operation sub-link indicator unit is configured to store a sub-link number of a read target sub-link, wherein the read target sub-link is a sub-link where the to-be-read data is located;

the sub-link length unit is configured to store sub-link length information, wherein the sub-link length information indicates the number of pieces of data currently stored in a sub-link;

the write pointer unit is configured to store an address of a piece of data in the RAM which is currently written into the multi-head linked list;

the read pointer unit is configured to store an address of a next piece of data in the RAM which is to be read from the multi-head linked list; and

the control unit is configured to: determine the write target sub-link according to the sub-link number stored in the write operation sub-link indicator unit when receiving a data writing request;

perform a data writing operation according to the free address, sub-link length information stored in a sub-link length unit of the write target sub-link, and an address stored in the write pointer unit; determine a read target sub-link according to the sub-link number stored in the read operation sub-link indicator unit when receiving a data reading request; and perform a data reading operation according to an address stored in a read pointer unit of the read target sub-link.

2. The linked list data structure according to claim 1, wherein the free address management unit is a First Input First Output (FIFO) device, wherein when an address in the RAM is free, the free address is written into the FIFO device.

3. The linked list data structure according to claim 1, wherein the write operation sub-link indicator unit, the read operation sub-link indicator unit, and the sub-link length unit are all registers.

4. A data processing method, applied to the linked list data structure of any one of claims 1 to 3, the method comprising: performing a data writing operation when the control unit receives a data writing request; wherein

performing the data writing operation comprises:

acquiring to-be-written data according to the data writing request;

reading a sub-link number stored in the write operation sub-link indicator unit, determining a write target sub-link according to the sub-link number stored in the write operation sub-link indicator unit, and acquiring sub-link length information stored in a sub-link length unit of the write target sub-link, and an address stored in a write pointer unit of the write target sub-link;

transmitting a free address reading request to the free address management unit, and receiving a free address returned by the free address management unit;

writing the to-be-written data into a data unit in the RAM corresponding to the free address;

determining whether to write the free address into a pointer storage unit in the RAM corresponding to the address stored in the write pointer unit of the write target sub-link according to the sub-link length information stored in the sub-link length unit of the write target sub-link;

updating the sub-link number stored in the write operation sub-link indicator unit to a sub-link number of a next write target sub-link;

updating the address stored in the write pointer unit of the write target sub-link to the free address;

updating the sub-link length information stored in the sub-link length unit of the write target sub-link according to the number of pieces of data currently stored in the write target sub-link.

5. The data processing method according to claim 4, wherein determining whether to write the free address into the pointer storage unit in the RAM corresponding to the address stored in the write pointer unit of the write target sub-link according to the sub-link length information stored in the sub-link length unit of the write target sub-link comprises:

determining whether the to-be-written data is the first piece of data written to the write target sub-link according to the sub-link length information stored in the sub-link length unit of the write target sub-link; determining that the pointer storage unit in the RAM corresponding to the address stored in the write pointer unit of the write target sub-link is empty when the to-be-written data is the first piece of data written to the write target sub-link; or writing the free address into the pointer storage unit in the RAM corresponding to the address stored in the write pointer unit of the write target sub-link when the to-be-written data is not the first piece of data written to the write target sub-link.

6. The data processing method according to claim 4, wherein

when the write target sub-link into which the to-be-written data is to be written is the i-th sub-link among the n sub-links, the next corresponding write target sub-link is the (i+1)-th sub-link, where $1 \leq i \leq n-1$;

when the write target sub-link into which the to-be-written data is to be written is the n-th sub-link among the n sub-links, the next corresponding write target sub-link is the 1st sub-link.

7. A data processing method, applied to the linked list data structure of any one of claims 1 to 3, the method comprising: performing a data reading operation when the control unit receives a data reading request; wherein

performing the data reading operation comprises:

determining a read target sub-link according to a sub-link number stored in the read operation

sub-link indicator unit, and acquiring an address stored in the read pointer unit of the read target sub-link;

reading out data in the data unit in the RAM corresponding to the address stored in the read pointer unit, and an address in the pointer storage unit;

outputting the data read out;

updating the sub-link number stored in the read operation sub-link indicator unit to a sub-link number of a next read target sub-link;

updating an address stored in the read pointer unit to the address read out.

8. The data processing method according to claim 7, wherein performing the data reading operation further comprises:

when a piece of data in a data unit corresponding to one address and the address in the pointer storage unit in the RAM are read out, writing the address read out into the free address management unit.

9. The data processing method according to claim 7, wherein

when the read target sub-link where the to-be-read data is located is the *i*-th sub-link among the *n* sub-links, the next corresponding read target sub-link is the (*i*+1)-th sub-link, with $1 \leqslant i \leqslant$ n-1;

when the read target sub-link where the to-be-read data is located is the *n*-th sub-link among the *n* sub-links, the next corresponding read target sub-link is the 1st sub-link.

10. A computer-readable storage medium, on which a computer program is stored, wherein the computer program, when executed by a processor, causes the processor to implement the data processing method of any one of claims 4 to 9.

11. An electronic device, comprising a processor and a memory storing a computer program executable by the processor, wherein the processor, when executing the computer program, implements the data processing method of any one of claims 4 to 9.

12. A chip, comprising a processor and a memory, wherein

the processor is configured to invoke and execute a computer program from the memory, to cause a device equipped with the chip to implement the data processing method of any one of claims 4 to 9.

13. A computer program product, comprising involved program instructions, wherein the involved program instructions, when executed by a processor, cause the processor to implement the data processing method of any one of claims 4 to 9.

14. A computer program, comprising program instructions, wherein the program instructions, when executed on an electronic device, cause the computer device to implement the data processing method of any one of claims 4 to 9.

15. A device, comprising at least one processor, wherein involved program instructions, when executed by the at least one processor, cause the device to implement the data processing method of any one of claims 4 to 9.