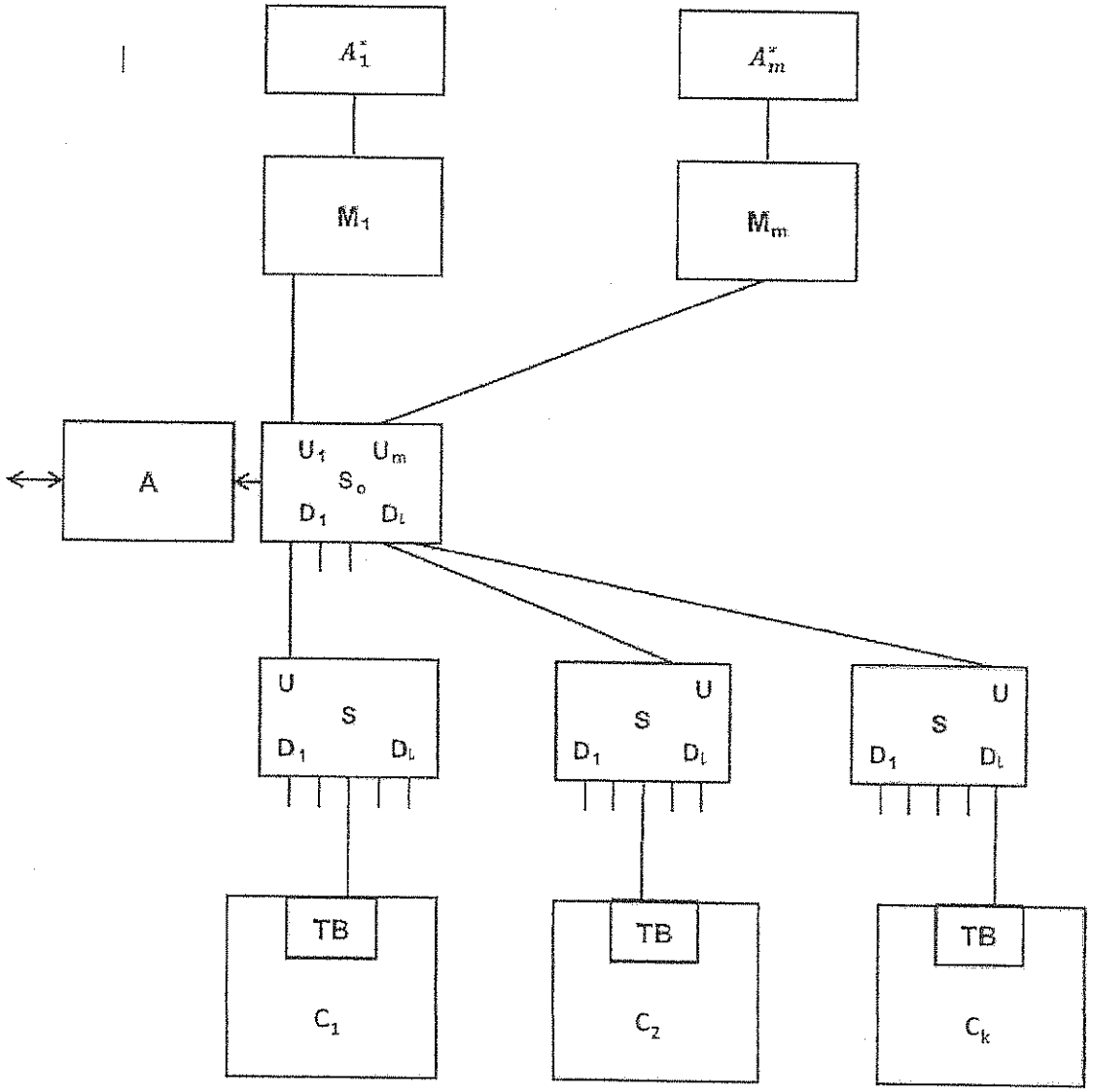


Fig. 1

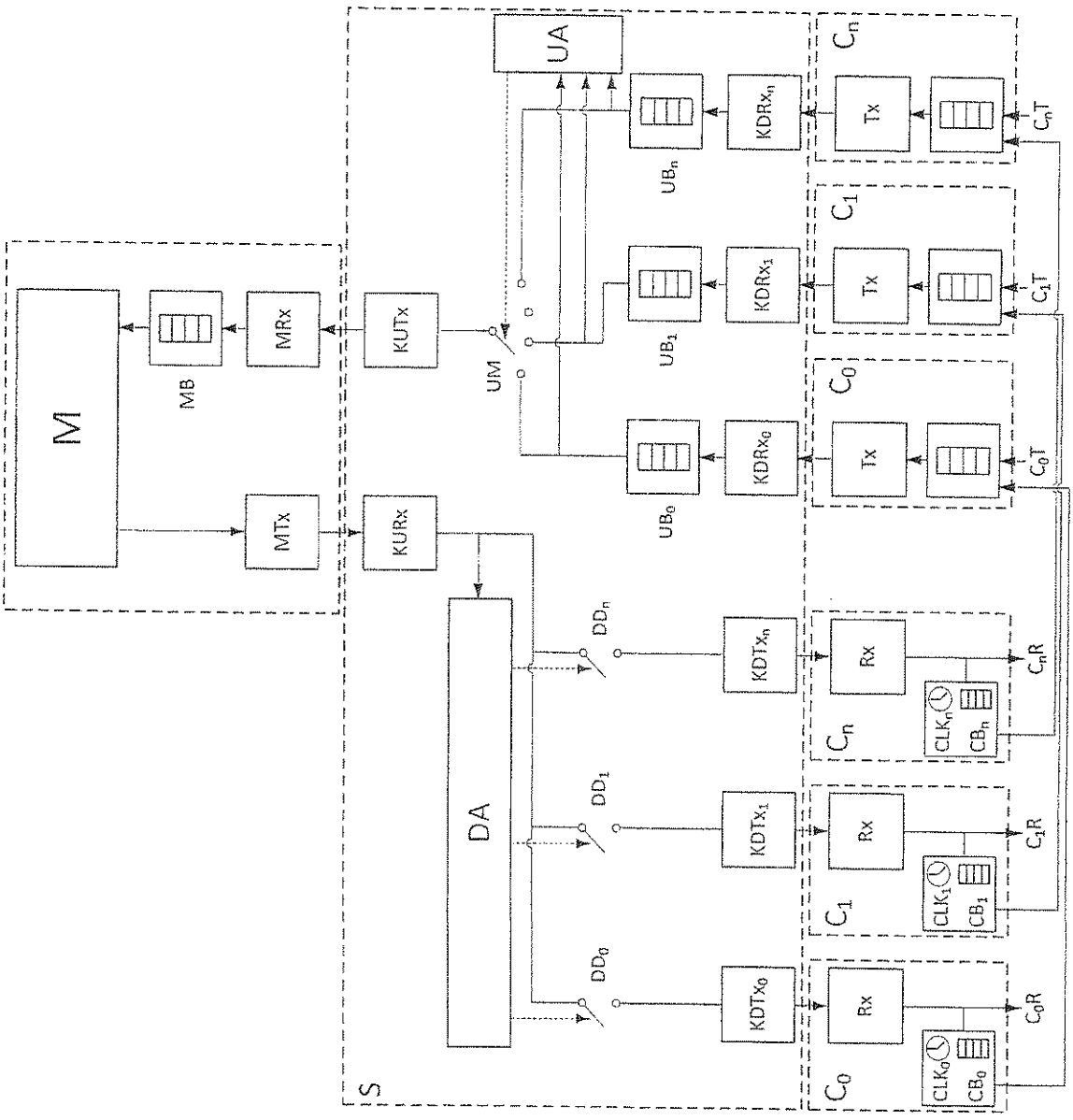

M
MB
MRx
MTx
KUTx
KURx
UM
UA
UB$_n$
UB$_1$
UB$_0$
KDRx$_n$
KDRx$_1$
KDRx$_0$
C$_n$
C$_1$
C$_0$
Tx
C$_n$T
C$_1$T
C$_0$T
DA
DD$_n$
DD$_1$
DD$_0$
KDTx$_n$
KDTx$_1$
KDTx$_0$
Rx
C$_n$R
C$_1$R
C$_0$R
CLK$_n$
CLK$_1$
CLK$_0$
CB$_n$
CB$_1$
CB$_0$
S

Fig. 2

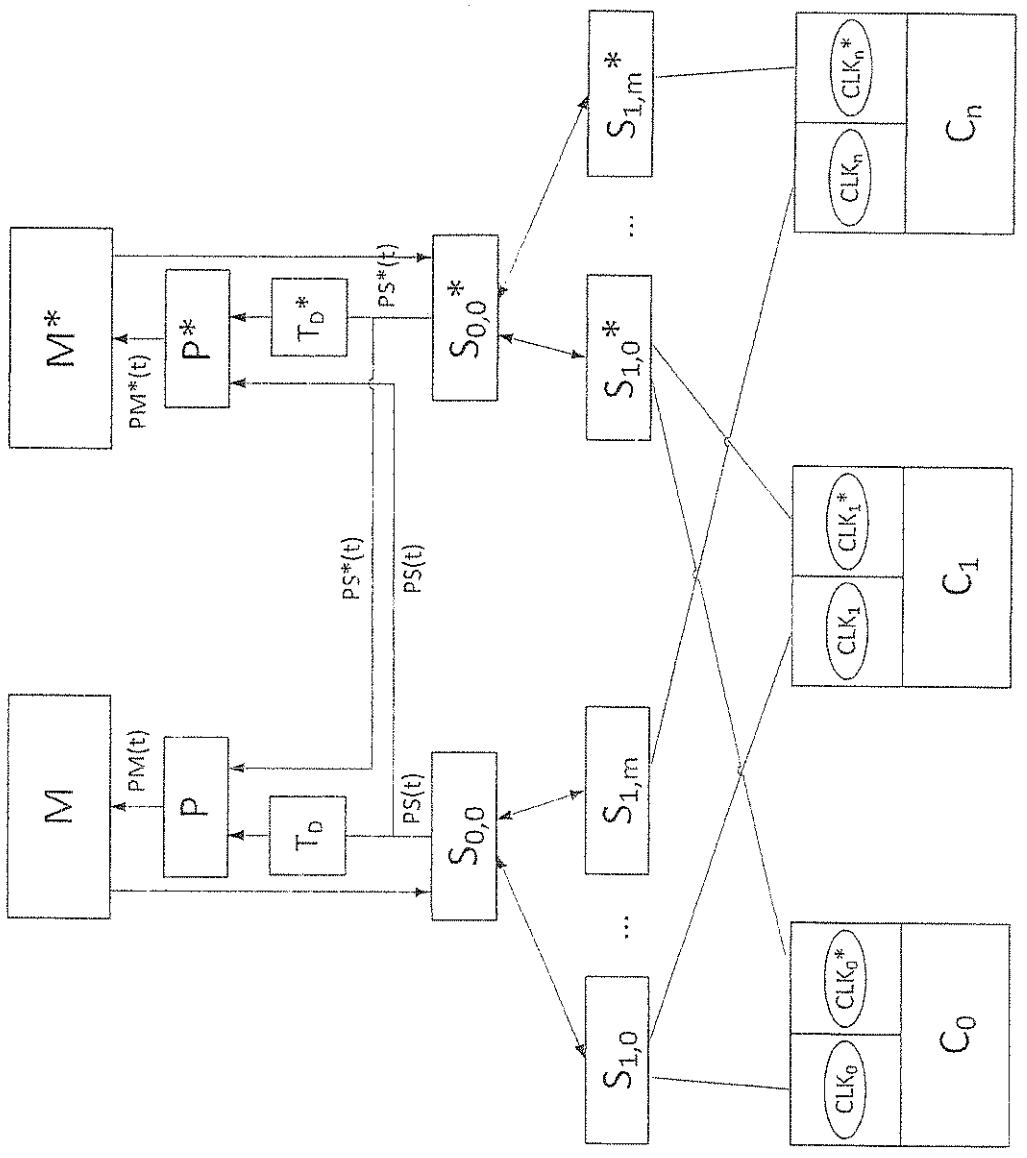

M*
P*
T_D*
PM*(t)
PS*(t)
S_0,0*
S_1,0*
S_1,m*
M
P
T_D
PM(t)
PS(t)
PS*(t)
PS(t)
S_0,0
S_1,m
S_1,0
CLK_n
CLK_n*
C_n
CLK_1
CLK_1*
C_1
CLK_0
CLK_0*
C_0

Fig. 3

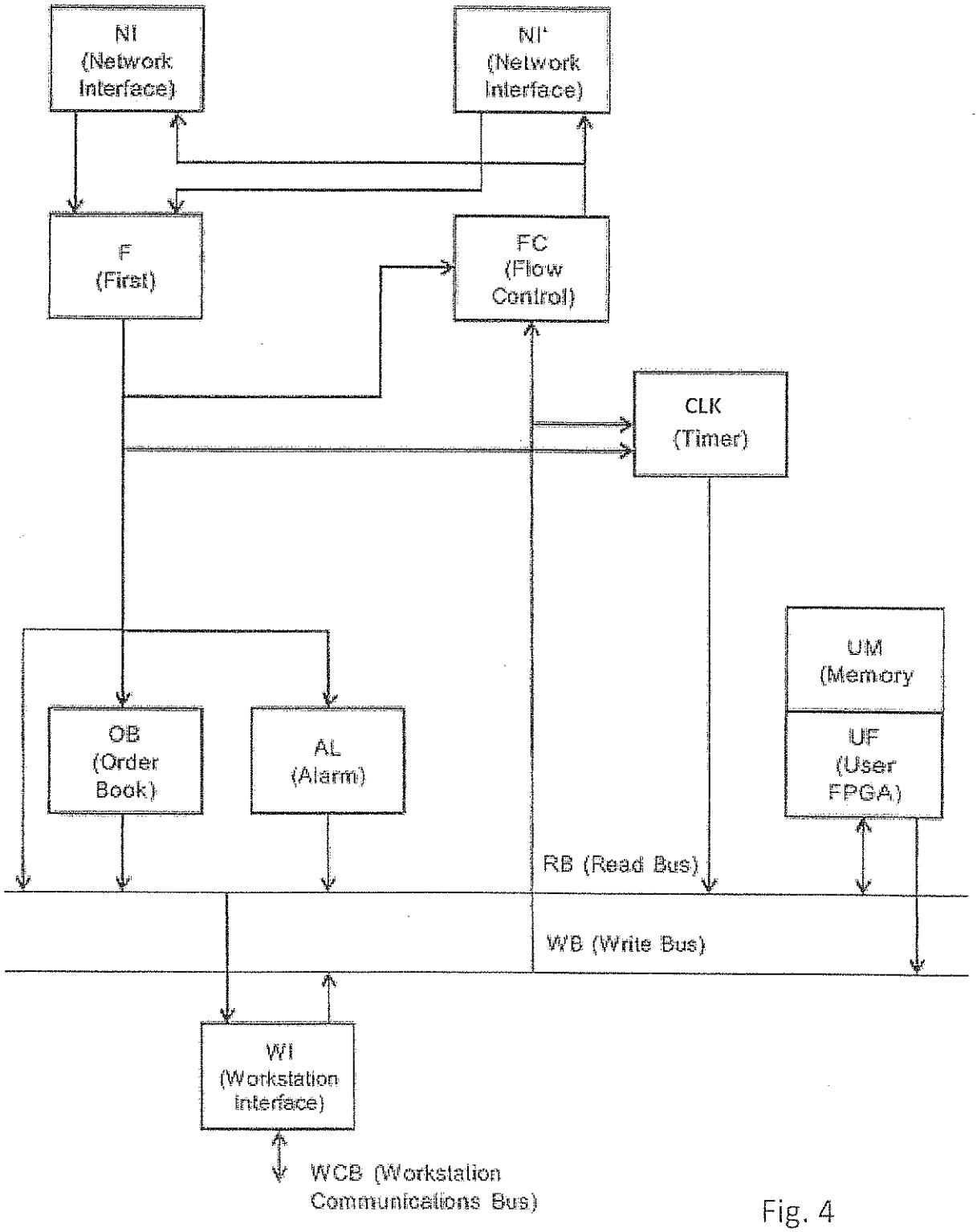

NI
(Network
Interface)
NI'
(Network
Interface)
F
(First)
FC
(Flow
Control)
CLK
(Timer)
UM
(Memory
UF
(User
FPGA)
OB
(Order
Book)
AL
(Alarm)
RB (Read Bus)
WB (Write Bus)
WI
(Workstation
Interface)
WCB (Workstation
Communications Bus)

Fig. 4

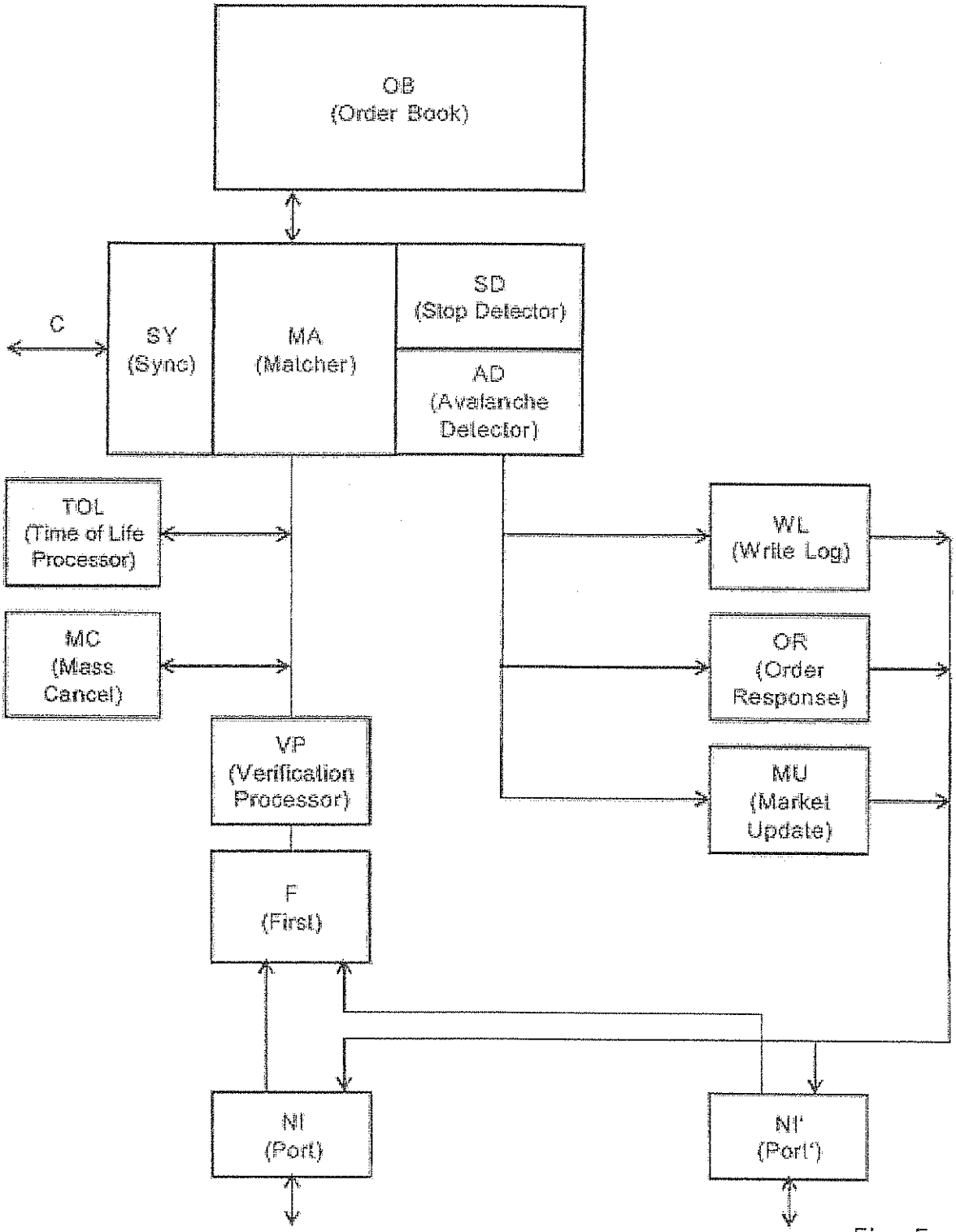

OB
(Order Book)
C
SY
(Sync)
MA
(Matcher)
SD
(Stop Detector)
AD
(Avalanche
Detector)
TOL
(Time of Life
Processor)
MC
(Mass
Cancel)
VP
(Verification
Processor)
F
(First)
NI
(Port)
WL
(Write Log)
OR
(Order
Response)
MU
(Market
Update)
NI'
(Port')

Fig. 5

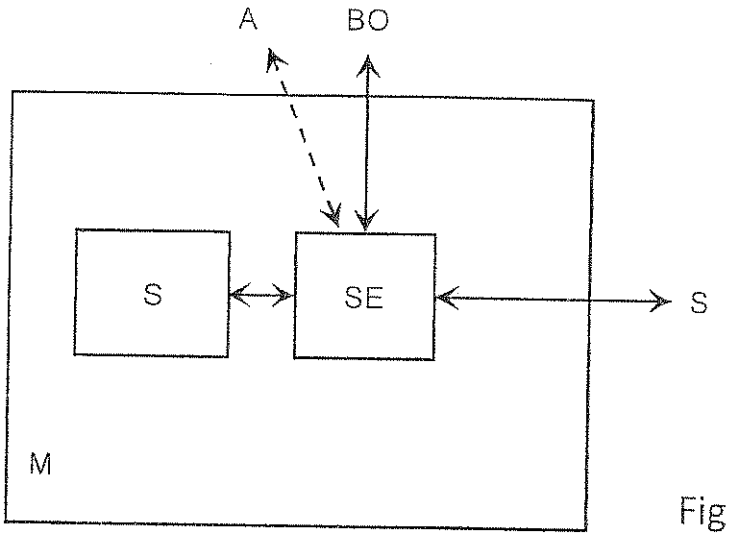


Fig. 6