

A SOLDER INTERCONNECTION HAVING A LAYERED BARRIER STRUCTURE AND METHOD FOR FORMING SAME

Technical Field

5 The present invention relates to solder interconnections and, in particular, relates to a solder interconnection having a layered barrier structure which inhibits reaction between a solder material and a substrate, and a method for forming the solder interconnection.

10 Background Art

Solder interconnections are commonly used in electronic components to provide conductivity paths, mechanical interconnection and means for thermal energy dissipation.

15 One of the more common solder compositions used today is tin-lead (SnPb) eutectic solder. It is important that the solder joint interconnections have good electrical conductivity, mechanical strength and are relatively easy to manufacture.

20 However, one factor which damages the electrical conductivity and mechanical strength of a solder joint is the reaction which occurs between the tin in the solder material and the electronic components in the component or chip being made.

This reaction results in the formation of intermetallic compounds in the solder interconnections which lead to weakened solder joint strength.

25 With the drive towards reducing lead content in electronic products, lead-free solder materials with a high percentage of tin content are being developed for solder interconnection. In order to properly form the lead-free solder materials, higher solder processing temperatures are also required. The higher tin content and the higher solder processing temperatures result in faster and stronger reactions between the tin in the solder and the metal underneath.

These reactions result in even weaker solder joint due to the rapid formation of undesirable intermetallic compounds.

It is therefore desirable to provide a barrier between the solder material and the underlying chip or component substrate which substantially inhibits the
5 reaction between the solder material and the substrate.

Disclosure of Invention

In a first aspect, the present invention provides a method for forming a solder interconnection having a layered barrier structure, the method
10 comprising the steps of:

- (a) depositing a first metallic layer on a substrate;
- (b) depositing a second metallic layer on the first metallic layer, wherein the first and second metallic layers are substantially formed from different materials;
- 15 (c) depositing a solder material having a defined melting point on the second metallic layer;
- (d) heating the layers and solder material at a temperature above the melting point of the solder material, thereby causing the second metallic layer to react with the solder material and form a non-continuous
20 intermetallic layer on the first metallic layer; and
- (e) treating the layers and solder material at a temperature below the melting point of the solder material, thereby converting the non-continuous intermetallic layer into a substantially continuous intermetallic layer,
- 25 the first metallic layer and the substantially continuous intermetallic layer comprising the layered barrier structure of the interconnection, the substantially continuous intermetallic layer being capable of substantially inhibiting an adverse reaction between the solder material and the first metallic layer and between the solder material and the substrate.

Preferably, the first metallic layer at least partially comprises a first metallic material and the second metallic layer at least partially comprises a second metallic material.

5 Preferably, one or both of the first and second metallic materials are metals or metal alloys.

Preferably, the second metallic material is copper (Cu) or Palladium (Pd) and the solder material at least partially comprises tin (Sn).

10 Preferably, the first metallic material at least partially comprises Nickel (Ni) or a Nickel alloy. More preferably, the Nickel alloy comprises Nickel Vanadium.

Preferably, the second metallic layer comprises one or more metallic layers.

Preferably, the non-continuous intermetallic layer at least partially comprises intermetallic materials selected from the group consisting of:

- 15 (a) Cu_6Sn_5 ;
(b) Cu_3Sn ;
(c) PdSn_4 ; and
(d) PdSn_3

20 Preferably, the continuous intermetallic layer at least partially comprises intermetallic materials selected from the group consisting of:

- (a) Cu_6Sn_5 ; and
(b) PdSn_4 .

Preferably, the continuous intermetallic layer comprises an undulating continuous intermetallic layer.

25 Preferably, the step of heating the layers and solder material at a temperature above the melting point of the solder material comprises heating the layers and solder material at a first prescribed temperature range for a first prescribed time period.

Preferably, the first prescribed temperature range comprises temperatures ranging from the melting point of the solder material up to about 100°C above the melting point of the solder material. More preferably, the first prescribed temperature range comprises temperatures ranging from the melting point of the solder material up to about 50°C above the melting point of the solder material.

Preferably, the first prescribed time period comprises time periods ranging from about 1 second to 100 seconds. More preferably, the first prescribed time period comprises time periods ranging from about 30 to 70 seconds.

Preferably, the step of treating the layers and solder material at a temperature below the melting point of the solder material comprises treating the layers and solder material at a second prescribed temperature range for a second prescribed time period.

Preferably, the second prescribed temperature range comprises temperatures ranging from about 100°C below the melting point of the solder material up to the melting point of the solder material. More preferably, when the solder material comprises eutectic SnPb solder, the second prescribed temperature range comprises temperatures ranging from about 100°C up to about 183°C, just below the melting point of the solder material.

Preferably, the second prescribed time period comprises time periods ranging from 1 hour to several hundred hours. More preferably, when the solder material comprises eutectic SnPb solder, the second prescribed time period comprises about four hours and the second prescribed temperature range comprises about 175°C.

Preferably, the substrate comprises one or more of:

- (a) a circuit;
- (b) an electronic component;
- (c) a chip;
- (d) a chip pad; and

- (e) a substrate pad.

In a second aspect, the present invention provides a solder interconnection having a layered barrier structure, formed by the method
5 according to the first aspect of the present invention.

In a third aspect, the present invention provides a solder interconnection having a layered barrier structure comprising:

- 10 (a) a first metallic layer having lower and upper surfaces and being joined at its lower surface to a substrate;
- (b) a substantially continuous intermetallic layer having lower and upper surfaces and being joined at its lower surface to the metallic layer's upper surface; and
- 15 (c) a solder material having lower and upper surfaces and being joined at its lower surface to the intermetallic layer's upper surface,

wherein the substantially continuous intermetallic layer is formed by:

- (i) depositing a second metallic layer on the first metallic layer, wherein the first and second metallic layers are formed from different materials;
- 20 (ii) depositing the solder material having a defined melting point on the second metallic layer;
- (iii) heating the layers and solder material at a temperature above the melting point of the solder material, thereby causing the second metallic layer to react with the solder material and form a non-continuous intermetallic layer on the first metallic layer; and
- 25 (iv) treating the layers and solder material at a temperature below the melting point of the solder material, thereby converting the non-continuous intermetallic layer into a substantially continuous intermetallic layer,

the first metallic layer and the substantially continuous intermetallic layer comprising the layered barrier structure of the interconnection, the substantially continuous intermetallic layer being capable of substantially inhibiting an adverse reaction between the solder material and the metallic layer and
5 between the solder material and the substrate.

Preferably, the substantially continuous intermetallic layer at least partially comprises an intermetallic material. More preferably, the intermetallic material comprises Cu_6Sn_5 or PdSn_4 .

Preferably, the metallic layer at least partially comprises a metal or a
10 metal alloy. More preferably, the metallic layer at least partially comprises Nickel (Ni) or a Nickel alloy.

In a fourth aspect, the present invention provides a layered barrier structure for a solder interconnection comprising:

- 15 (a) a first metallic layer having lower and upper surfaces and being joined at its lower surface to a substrate; and
- (b) a substantially continuous intermetallic layer having lower and upper surfaces and being joined at its lower surface to the metallic layer's upper surface and at its upper surface to a solder material;

20 wherein the substantially continuous intermetallic layer is formed by:

- (i) depositing a second metallic layer on the first metallic layer, wherein the first and second metallic layers are formed from different materials;
- (ii) depositing the solder material having a defined melting point on the second metallic layer;
- 25 (iii) heating the layers and solder material at a temperature above the melting point of the solder material, thereby causing the second metallic layer to react with the solder material and form a non-continuous intermetallic layer on the first metallic layer; and
- (iv) treating the layers and solder material at a temperature below the
30 melting point of the solder material, thereby converting the non-

continuous intermetallic layer into a substantially continuous intermetallic layer,

the first metallic layer and the substantially continuous intermetallic layer comprising a layered barrier structure for a solder interconnection, the
5 substantially continuous intermetallic layer being capable of substantially inhibiting an adverse reaction between the solder material and the metallic layer and between the solder material and the substrate.

Throughout this specification, unless the context requires otherwise, the
10 word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Any discussion of documents, acts, materials, devices, articles or the like
15 which has been included in the present specification is solely for the purpose of providing a context for the present invention. It is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

20 In order that the present invention may be more clearly understood, preferred forms will be described with reference to the following drawings and examples.

Brief Description of the Drawings

25 Figure 1 is a flow diagram illustrating the method for forming a solder interconnection having a layered barrier structure according to the invention;

Figures 2-7 are sequential cross-sectional side views of a solder interconnection being formed according to the method of the present invention; and

Figure 8 is a cross-sectional side view of a further embodiment of a solder interconnection having a layered barrier structure according to the invention.

5 Detailed Description

The preferred embodiment of the method for forming a solder interconnection having a layered barrier structure is illustrated in the flow diagram of Figure 1. The steps illustrated in Figure 1 are also described in detail below with reference to Figures 2-7.

10 Referring firstly to Figure 2, the first step involves providing a substrate 1 upon which the solder interconnection is to be formed. The substrate may take the form of a circuit, an electronic component, a chip, a chip pad or a substrate pad.

 The next step shown in Figures 1 and 3 involves depositing 2 a first
15 metallic layer 3 on the substrate 1. This first metallic layer is a metal or metal alloy and is preferably nickel (Ni) or a nickel alloy such as nickel vanadium.

 As shown in Figures 1 and 4, the next step involves depositing 4 a
 second metallic layer 5 on the first metallic layer 3. The first and second
 metallic layers are preferably formed of different materials. The second
20 metallic layer should be a metal or metal alloy and is preferably copper (Cu) or
 palladium (Pd) deposited by sputtering.

 As shown in Figures 1 and 5, the next step involves depositing 6 a
 solder material 7 on the second metallic layer 5. The solder material has a
 defined melting point and is at least partially made from tin (Sn). Preferably,
25 the solder material is a tin lead (SnPb) alloy.

 As shown in Figures 1 and 6, the next step involves heating 8 the layers
 and solder material at a temperature above the melting point of the solder
 material. This heating step causes the second metallic layer 5 to react with the
 solder material 7 and to form a non-continuous intermetallic layer 9 on the first
30 metallic layer 3. When the second metallic layer is made of Cu and the solder
 material includes Sn, the non-continuous intermetallic layer 9 is made up of

Cu_6Sn_5 and/or Cu_3Sn . When the second metallic layer 5 is made of Pd and the solder material includes Sn, the non-continuous intermetallic layer is made up of PdSn_4 and PdSn_3 .

As shown in Figure 6, during this heating step 8, the non-continuous intermetallic layer takes the form of a series of scallop-shaped formations 10.

This heating step 8 is performed at a first prescribed temperature range for a first prescribed time period. When eutectic SnPb solder is used, the first prescribed temperature should be around 220°C (40°C above the solder melting point). Other temperatures above the solder melting point sufficient to induce reaction between the second metallic layer 5 and the solder material 7 may also be used. The inventors have found that an effective first prescribed time period is 40 to 60 seconds. Other time periods may also be effective.

Because the non-continuous intermetallic layer 9 is not continuous there are points of contact 11 between the solder 8 and the first metallic layer 3. If the interconnection was left in this state further reaction could occur between the solder material 7 and the first metallic layer 3, and even the substrate 1. If left in this state, such reactions could occur during the manufacturing process or during use of the component and would lead to a weakening of the solder joint. However, the intermetallic layer is not left in this non-continuous state, but is transformed into a continuous intermetallic layer by the steps described below.

Referring to Figures 1 and 7, the next step in the preferred method involves treating the layers and solder material at a temperature below the melting point of the solder material. This step flattens out the non-continuous intermetallic layer 9 into a substantially continuous intermetallic layer 13.

Depending upon whether the second metallic layer contained Cu or Pd, this continuous intermetallic layer 13 will include either Cu_6Sn_5 or PdSn_4 . As shown in Figure 7, the continuous intermetallic layer 13 is an undulating continuous intermetallic layer without any points of contact between the solder material 7 and the first metallic layer 3.

The first metallic layer 3 and the substantially continuous intermetallic layer 13 make up a layered barrier structure 14.

The continuous intermetallic layer 13 in the layered barrier structure 14 is capable of substantially inhibiting an adverse reaction between the solder material 7 and the first metallic layer 3. It also is capable of substantially inhibiting an adverse reaction between the solder material 7 and the substrate 1.

The step of treating 12 the layers and solder material at a temperature below the melting point of the solder material preferably involves treating at temperatures ranging from about 100°C below the melting point of the solder material up to the melting point of the solder material. When eutectic SnPb solder is used, the heating temperature for this step is preferably about 150 to 175°C. This treating step 12 may be performed at times ranging from about 1 hour to several hundred hours. When eutectic SnPb solder is used, the inventors have found that treating step 12 is effective for times ranging from 1 hour to several hundred hours, depending upon the temperature used. One suitable example time and temperature range would be treating for four hours at 175°C.

It will be appreciated from the foregoing discussion that the layered barrier structure is able to substantially inhibit undesirable reactions between the Sn in the solder material and both the first metallic layer and the chip circuit metallurgy in the substrate beneath that layer. A solder interconnection formed according to this method will continue to have good electrical conductivity and maintain its mechanical strength for longer periods than prior art solder interconnections.

As shown in Figure 7, a solder interconnection having a layered barrier structure which is formed according to above-described method will have a number of features. The interconnection will have a first metallic layer 3 having lower 16 and upper 17 surfaces and will be joined at its lower surface 16 to the substrate 1. The interconnection will have a substantially continuous intermetallic layer 13 which also has lower 18 and upper 19 surfaces and is joined at its lower surface 18 to the upper surface 17 of the metallic layer 3.

The interconnection will also have a solder material 7 having lower 20 and upper 21 surfaces, the solder material being joined at its lower surface 20 to the upper surface 19 of the intermetallic layer 13. In this form, the metallic layer 3 and the substantially continuous intermetallic layer 13 comprise the
5 layered barrier structure 14 of the interconnection. The substantially continuous intermetallic layer 13 is able to substantially inhibit an adverse reaction between the solder material 7 and the metallic layer 3 and between the solder material 7 and the substrate 1.

It will be appreciated by persons skilled in the art that numerous
10 variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. For example, in the alternative embodiment shown in Figure 8 the solder interconnection may include an adhesion layer 15 between the substrate 1 and the first metallic layer 2. This adhesion layer 15 will
15 normally be applied to the substrate 1 before performing the step of depositing 2 the first metallic layer 3 on the substrate 1. Furthermore, the second metallic layer 5 may take the form of one, two or more metallic layers, as long as they are suitable for reacting with the solder material 7 to form the intermetallic materials which make up the non-continuous 9 and continuous 13
20 intermetallic layers. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

Claims:

1. A method for forming a solder interconnection having a layered barrier structure, the method comprising the steps of:
 - (a) depositing a first metallic layer on a substrate;
 - 5 (b) depositing a second metallic layer on the first metallic layer, wherein the first and second metallic layers are substantially formed from different materials;
 - (c) depositing a solder material having a defined melting point on the second metallic layer;
 - 10 (d) heating the layers and solder material at a temperature above the melting point of the solder material, thereby causing the second metallic layer to react with the solder material and form a non-continuous intermetallic layer on the first metallic layer; and
 - 15 (e) treating the layers and solder material at a temperature below the melting point of the solder material, thereby converting the non-continuous intermetallic layer into a substantially continuous intermetallic layer,

the first metallic layer and the substantially continuous intermetallic layer comprising the layered barrier structure of the interconnection, the substantially

 - 20 continuous intermetallic layer being capable of substantially inhibiting an adverse reaction between the solder material and the first metallic layer and between the solder material and the substrate.
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2. The method according to claim 1 wherein the first metallic layer at least
25 partially comprises a first metallic material and the second metallic layer at least partially comprises a second metallic material.
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3. The method according to claim 2 wherein one or both of the first and second metallic materials are metals or metal alloys.

4. The method according to claim 3 wherein the second metallic material is copper (Cu) or Palladium (Pd) and the solder material at least partially comprises tin (Sn).

5 5. The method according to claim 3 or claim 4 wherein the first metallic material at least partially comprises Nickel (Ni) or a Nickel alloy.

6. The method according to claim 5 wherein the Nickel alloy comprises Nickel Vanadium.

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7. The method according to any one of the preceding claims wherein the second metallic layer comprises one or more metallic layers.

8. The method according to any one of the preceding claims wherein the
15 non-continuous intermetallic layer at least partially comprises intermetallic materials selected from the group consisting of:

(a) Cu_6Sn_5 ;

(b) Cu_3Sn ;

(c) PdSn_4 ; and

20 (d) PdSn_3

9. The method according to any one of the preceding claims wherein the continuous intermetallic layer at least partially comprises intermetallic materials selected from the group consisting of:

25 (a) Cu_6Sn_5 ; and

(b) PdSn_4 .

10. The method according to any one of the preceding claims wherein the continuous intermetallic layer comprises an undulating continuous intermetallic layer.

5 11. The method according to any one of the preceding claims wherein the step of heating the layers and solder material at a temperature above the melting point of the solder material comprises heating the layers and solder material at a first prescribed temperature range for a first prescribed time period.

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12. The method according to claim 11 wherein the first prescribed temperature range comprises temperatures ranging from the melting point of the solder material up to 100°C above the melting point of the solder material.

15 13. The method according to claim 12 wherein the first prescribed temperature range comprises temperatures ranging from the melting point of the solder material up to 50°C above the melting point of the solder material.

20 14. The method according to any one of claims 11 to 13 wherein the first prescribed time period comprises time periods ranging from 1 second to 100 seconds.

15. The method according to claim 14 wherein the first prescribed time period comprises time periods ranging from 30 to 70 seconds.

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16. The method according to any one of the preceding claims wherein the step of treating the layers and solder material at a temperature below the melting point of the solder material comprises treating the layers and solder material at a second prescribed temperature range for a second prescribed time period.

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17. The method according to claim 16 wherein the second prescribed temperature range comprises temperatures ranging from about 100°C below the melting point of the solder material up to the melting point of the solder material.

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18. The method according to claim 16 or claim 17 wherein the second prescribed time period comprises time periods ranging from about 1 hour to several hundred hours.

10 19. The method according to any one of the preceding claims wherein the substrate comprises one or more of:

- (a) a circuit;
- (b) an electronic component;
- (c) a chip;
- 15 (d) a chip pad; and
- (e) a substrate pad.

20. A solder interconnection having a layered barrier structure, formed by the method according to any one of claims 1 to 19.

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21. A solder interconnection having a layered barrier structure comprising:

- (a) a first metallic layer having lower and upper surfaces and being joined at its lower surface to a substrate;
- (b) a substantially continuous intermetallic layer having lower and upper
25 surfaces and being joined at its lower surface to the metallic layer's upper surface; and
- (c) a solder material having lower and upper surfaces and being joined at its lower surface to the intermetallic layer's upper surface,

wherein the substantially continuous intermetallic layer is formed by:

- (i) depositing a second metallic layer on the first metallic layer, wherein the first and second metallic layers are formed from different materials;
- (ii) depositing the solder material having a defined melting point on the second metallic layer;
- (iii) heating the layers and solder material at a temperature above the melting point of the solder material, thereby causing the second metallic layer to react with the solder material and form a non-continuous intermetallic layer on the first metallic layer; and
- (iv) treating the layers and solder material at a temperature below the melting point of the solder material, thereby converting the non-continuous intermetallic layer into a substantially continuous intermetallic layer,

the first metallic layer and the substantially continuous intermetallic layer comprising the layered barrier structure of the interconnection, the substantially continuous intermetallic layer being capable of substantially inhibiting an adverse reaction between the solder material and the first metallic layer and between the solder material and the substrate.

22. The solder interconnection according to claim 21 wherein the substantially continuous intermetallic layer at least partially comprises an intermetallic material.

23. The solder interconnection according to claim 22 wherein the intermetallic material comprises Cu_6Sn_5 or PdSn_4 .

24. The solder interconnection according to any one of claims 21 to 23 wherein the first metallic layer at least partially comprises a metal or a metal alloy.

25. The solder interconnection according to claim 24 wherein the first metallic layer at least partially comprises Nickel (Ni) or a Nickel alloy.

26. A layered barrier structure for a solder interconnection comprising:

- 5 (a) a first metallic layer having lower and upper surfaces and being joined at its lower surface to a substrate; and
- (b) a substantially continuous intermetallic layer having lower and upper surfaces and being joined at its lower surface to the metallic layer's upper surface and at its upper surface to a solder material;

10 wherein the substantially continuous intermetallic layer is formed by:

- (i) depositing a second metallic layer on the first metallic layer, wherein the first and second metallic layers are formed from different materials;
- (ii) depositing the solder material having a defined melting point on the second metallic layer;
- 15 (iii) heating the layers and solder material at a temperature above the melting point of the solder material, thereby causing the second metallic layer to react with the solder material and form a non-continuous intermetallic layer on the first metallic layer; and
- (iv) treating the layers and solder material at a temperature below the
20 melting point of the solder material, thereby converting the non-continuous intermetallic layer into a substantially continuous intermetallic layer,

the first metallic layer and the substantially continuous intermetallic layer comprising a layered barrier structure for a solder interconnection, the
25 substantially continuous intermetallic layer being capable of substantially inhibiting an adverse reaction between the solder material and the first metallic layer and between the solder material and the substrate.