

SEMICONDUCTOR PROCESSING APPARATUS

ABSTRACT

The present disclosure discloses a semiconductor processing apparatus, which is configured to perform processing on a wafer. The disclosed semiconductor processing apparatus includes a vacuum interlock chamber, a plurality of apparatus bodies, the apparatus body including a transfer platform, and at least two reaction chambers being arranged along a circumferential direction of the transfer platform, and a temporary storage channel, any two neighboring apparatus bodies being communicated through the temporary storage channel, and the temporary storage channel being configured to temporarily store the wafer. One of the plurality apparatus bodies is connected to the vacuum interlock chamber. The transfer platform is configured to transfer the wafer between the vacuum interlock chamber and the reaction chamber, between the temporary storage channel and the vacuum interlock chamber, and between the temporary storage channel and the reaction chamber. With the above solution, the problem that the productivity of the semiconductor processing apparatus is low is solved.

Fig. 1