

PATENT SPECIFICATION

(11) 1 271 896

DRAWINGS ATTACHED



- (21) Application No. 26488/70 (22) Filed 2 June 1970
(31) Convention Application No. 831 883, (32) Filed 10 June 1969 in
(33) United States of America (US)
(45) Complete Specification published 26 April 1972
(51) International Classification H01L 5/00 9/00
(52) Index at acceptance

H1K 211 238 271 227 306 312 353 413 41Y 422 441 511
52Y 54Y 552 555 55Y 574 578 579 581 583 596
597 618 61Y 638 63Y 650

(54) SEMICONDUCTOR RECTIFYING JUNCTION DEVICE

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor rectifying junction devices. More particularly, the invention relates to N+/P+ zener diodes, useful in monolithic integrated circuits.

Heretofore, many zener diodes in monolithic integrated circuits have been fabricated by diffusing a first region of one type high conductivity into the integrated circuit, and then diffusing a second region of opposite type high conductivity into a part of the first region; usually by diffusing an N+ region into a diffused P+ region. The impurity concentration of both regions has been very high, and the N+/P+ junction between them has been at a shallow depth, usually less than one micrometer. However, the shallowness of the N+/P+ junction has caused many of the diodes to become leaky or shorted out when electrical contacts were alloyed to the diode. Aluminum was generally used for the electrical contacts, and when the aluminum was heated to a temperature sufficient to alloy it to the semiconductor material, it would penetrate the surface spiking into the semiconductor body. In particular, the aluminum would spike through the second region and across the shallow N+/P+ junction, thereby shorting the device and degrading the production yield.

According to the invention we provide a semiconductor device comprising a body of semiconductor material having a surface, a zener diode in said body comprising a first region of one conductivity type containing two diffused portions, one of said portions having a high maximum impurity concen-

tration and having a boundary at a predetermined depth with respect to said surface and the other portion having a significantly lower maximum impurity concentration and a boundary at a significantly lesser depth than said one portion, said first region containing a second region of opposite type conductivity connected to both portions of said first region and separated from each by a PN junction, at least a part of the PN junction between said second region and said one portion being within the zones of maximum impurity concentration of each, a part of the PN junction between said second region and said other portion of said first region being at a significantly greater depth than the PN junction between said second region and said one portion of said first region, and an electrical contact to said second region only where it overlies said other portion of said first region where the PN junction is at a significantly greater depth.

In the accompanying drawing:

Figure 1 is a cross-sectional schematic view of a part of a monolithic integrated circuit which includes the improved zener diode;

Figures 2 through 6 are cross-sectional schematic views illustrating several stages in a preferred fabrication process for the improved zener diode; and

Figure 7 is a graph which illustrates the diffusion profiles for the improved zener diode.

EXAMPLE

Figure 1 is a cross-sectional schematic view of a part of a monolithic integrated circuit which includes the improved zener diode 10. The integrated circuit comprises a semiconductor substrate 12 and an epitaxial layer 14 disposed thereon and separated by a junction 16. In Figure 1, the substrate 12 is of P type conductivity, and may include an N+ pocket 18 adjacent the junction 16, as is well known in the prior-art. The epitaxial layer 14 is of N type conductivity

and has an exposed surface 20. A P+ collar 22 surrounds a part of the epitaxial layer 14 forming an N boat region 24 isolated from the remainder of the epitaxial layer 14. The N region 24 is electrically insulated from the remainder of the epitaxial layer 14 and usually contains one or more electrical devices; such as in Figure 1, where the N region 24 contains the improved zener diode 10 adjacent the surface 20.

The improved zener diode 10 includes a first region 26 of one type conductivity having two portions 28 and 30 laterally connected together and adjacent the surface 20; however, the portion 28 has a significantly higher conductivity and impurity dopant concentration than the other portion 30. In Figure 1, the region 26 is of P type conductivity and comprises a P+ portion 28 and a P portion 30. The portion 28 also has a substantially greater depth than the portion 30. A second region 32 of opposite type high conductivity is connected to both portions 28 and 30 of the first region 26, and is also adjacent the surface 20. In Figure 1, the second region 32 is of N+ conductivity and is disposed with both portions 28 and 30, forming an N+/P+ junction 34 with the P+ portion 28 and an N+/P junction 36 with the P portion 30. The N+/P junction 36 between the second region 32 and the lower impurity portion 30 is at a significantly greater depth than the N+/P+ junction 34 between the second region 32 and the high impurity portion 28. Electrical connection is made by electrical contacts 38 and 40 which are alloyed to the surfaces of the N+ region 32 and the P+ region 28, respectively. The electrical contact 38 to the N+ region 32 is made only above the P portion 30 where the N+/P junction 36 is at a significantly greater depth.

Figures 2 through 6 illustrate several stages in a preferred fabrication process for the improved zener diode 10 in a typical monolithic integrated circuit. Figure 2 shows a part of the integrated circuit before the improved zener diode 10 is fabricated in it. The substrate 12 and the epitaxial layer 14 are made of monocrystalline silicon and have resistivities of 25—50 ohm-cm and 1—6 ohm-cm, respectively. The epitaxial layer 14, is grown to a thickness of 10 to 14 micrometers and has an impurity dopant concentration of about 5×10^{15} atoms/cm³. The N+ pocket 18 and the P+ collar 22 may be formed by diffusion methods well known in the prior-art.

The first step in fabricating the improved zener diode 10 is to diffuse the P+ portion 28 of the region 26 into the N boat region 24. As shown in Figure 3, the surface 20 is coated with a passivating layer 42, and a

part of the passivating layer is removed to expose a part of the surface 20 above the N boat 24. Usually, this is done by depositing a layer of silicon dioxide to a thickness of 5,000—10,000 Å and removing a part thereof by standard photoresist methods, as is well known in the prior-art. A P+ diffusion is then performed by exposing the surface 20 to boron nitride for 45 minutes at 1150°C and then to steam for 45 minutes at 1165°C. The resulting P+ portion 28 diffuses deeply into the N region 24 to a depth of about 4.5 micrometers before its impurity concentration falls below that of the N region 24.

The P portion 30 of the first region 26 is then formed by diffusion. The oxide coating 42 is stripped away and a new oxide coating 44 is laid down and opened up to expose another part of the surface 20. As shown in Figure 4, the oxide coating 44 is removed in the area adjacent the P+ portion 28 and a part of the N region 24 laterally connected to it, so that the following P diffusion forms laterally connected P and P+ portions 30 and 28 adjacent the surface 20. The P diffusion is performed by exposing the surface 20 to boron nitride for 40 minutes at 950°C, and then to a dry atmosphere for 50 minutes and to a wet atmosphere for 50 minutes at 1100°C. The same gas boron nitride, is used in both the P and P+ diffusions, but the lower deposition and diffusion temperatures for the P diffusion result in the P portion 30 having a significantly lower impurity concentration and diffusion depth. The P portion 30 only diffuses to a depth of about 2.0 micrometers before its impurity concentration falls below that of the N region 24. Usually, this P diffusion is made at the same time the base and resistor diffusions are made in other parts of the integrated circuit, and thus eliminates the need for an additional diffusion step.

The N+ region 32 is then formed by diffusion. The oxide coating 44 is removed and a new oxide coating 46 is laid down and opened up to expose another part of the surface 20. As shown in Figure 5, the oxide coating 46 is removed in part of the area adjacent both the P+ portion 28 and the P portion 30 of the region 26. The N+ diffusion may then be performed by exposing the surface 20 to POCl₃ for 18 minutes at 1050°C and then to steam for 45 minutes at 945°C. The resulting N+ region 32 is disposed within both portions of the first region 26, forming the rectifying junctions 34 and 36 with the portions 28 and 30, respectively. The junction depths and diffusion profiles resulting from the above diffusions are discussed below.

Figure 7 illustrates the impurity concentration as a function of depth for both por-

tions of the first region 26 and the second region 32. As shown by curve 50, the P+ portion 28 has a high surface impurity concentration of about 8×10^{19} atoms/cm³ and diffuses deeply into the N region 24. As shown by the curve 52, the P portion 30 has a significantly lower surface impurity concentration of about 5×10^{18} atoms/cm³ and does not diffuse as deeply into the N region 24. The N+ region 32, which is diffused into both portions of the first region 26, forms a rectifying junction at a different depth in each portion depending upon the depth at which their respective impurity concentrations equalize. As shown by the curve 54, the N+ region 32 has the highest surface impurity concentration of about 1.2×10^{21} atoms/cm³ but does not diffuse very deeply. The N+ impurity concentration 54 quickly falls below that of the P+ concentration 50, forming the N+/P+ junction 34 at their intersection. The junction 34 is similar to that formed in prior-art zener diodes; and is shown by dotted line 56, it is formed at the intersection of the curves 50 and 54 at a shallow depth of about 0.7 micrometers. However, the P impurity concentration 52 is substantially lower than that of the P+ concentration 50; and consequently, the N+ impurity concentration 54 remains above that of the P concentration 52 for a greater depth, forming the N+/P junction 36 at the greater depth of about 1.4 micrometers, as shown by the dotted line 58.

Electrical connection is then made to the improved zener diode 10 by the electrical contacts 38 and 40. As shown in Figure 6, a new oxide coating 48 is laid down and opened up to expose a part of the surface 20 adjacent the N+ region 32 and another part of the surface 20 adjacent the P+ portion 28. The surface 20 adjacent the N+ region 32 is exposed only in the area where the N+ region 32 is disposed within the P portion 30 having the substantially lower impurity concentration and the substantially greater N+/P junction 36 depth. A coating of a highly conductive material is then deposited on the oxide coating 48 and the two exposed parts of the surface 20, and is selectively removed to yield the electrical contacts 38 and 40. Usually, the electrical contacts are made of aluminum which is vaporized onto the surface 20 and then heated to 530°C to alloy it to the silicon. Since the electrical contact 38 to the N+ region 32 is made only in the area over the P portion 28 where the N+/P junction 36 is at a significantly greater depth, the chances of the aluminum spiking through the N+/P junction 36 and shorting the zener diode 10 are greatly reduced.

The N+/P+ characteristic of zener diodes is maintained with the improved zener

diode 10 because the voltage breakdown occurs across the N+/P+ junction 34. The N+/P+ junction 34 has a voltage breakdown of 5.5 volts but the N+/P junction 36 has a higher voltage breakdown of 7.0 volts; consequently, the diode breaks down across the lower voltage N+/P+ junction 34 even though the electrical contact to the N+ region 32 is only made above the N+/P junction 36.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a body of semiconductor material having a surface, a zener diode in said body comprising a first region of one conductivity type containing two diffused portions, one of said portions having a high maximum impurity concentration and having a boundary at a predetermined depth with respect to said surface and the other portion having a significantly lower maximum impurity concentration and a boundary at a significantly lesser depth than said one portion, said first region containing a second region of opposite type conductivity connected to both portions of said first region and separated from each by a PN junction, at least a part of the PN junction between said second region and said one portion being within the zones of maximum impurity concentration of each, a part of the PN junction between said second region and said other portion of said first region being at a significantly greater depth than the PN junction between said second region and said one portion of said first region, and an electrical contact to said second region only where it overlies said other portion of said first region where the PN junction is at a significantly greater depth.

2. A semiconductor device as claimed in claim 1, wherein the maximum impurity concentration in said one portion of said first region is about 8×10^{19} atoms/cm³, the maximum impurity concentration in said other portion of said first region is about 5×10^{18} atoms/cm³, and the maximum impurity concentration in said second region is about 1.2×10^{21} atoms/cm³.

3. A semiconductor device as claimed in claim 2, wherein the PN junction between said second region and said other portion of said first region is at a depth of about 1.4 micrometers with respect to said surface.

4. A semiconductor device as claimed in claim 3, wherein said zener diode is an element of a microcircuit of the monolithic integrated type, said first region being disposed within an isolated region in said body of the same conductivity type as said second region.

5. A process of making a semiconductor device including a zener diode as claimed in claim 1 in a body of semiconductive

tions of the first region 26 and the second region 32. As shown by curve 50, the P+ portion 28 has a high surface impurity concentration of about 8×10^{19} atoms/cm³ and diffuses deeply into the N region 24. As shown by the curve 52, the P portion 30 has a significantly lower surface impurity concentration of about 5×10^{18} atoms/cm³ and does not diffuse as deeply into the N region 24. The N+ region 32, which is diffused into both portions of the first region 26, forms a rectifying junction at a different depth in each portion depending upon the depth at which their respective impurity concentrations equalize. As shown by the curve 54, the N+ region 32 has the highest surface impurity concentration of about 1.2×10^{21} atoms/cm³ but does not diffuse very deeply. The N+ impurity concentration 54 quickly falls below that of the P+ concentration 50, forming the N+/P+ junction 34 at their intersection. The junction 34 is similar to that formed in prior-art zener diodes; and is shown by dotted line 56, it is formed at the intersection of the curves 50 and 54 at a shallow depth of about 0.7 micrometers. However, the P impurity concentration 52 is substantially lower than that of the P+ concentration 50; and consequently, the N+ impurity concentration 54 remains above that of the P concentration 52 for a greater depth, forming the N+/P junction 36 at the greater depth of about 1.4 micrometers, as shown by the dotted line 58.

Electrical connection is then made to the improved zener diode 10 by the electrical contacts 38 and 40. As shown in Figure 6, a new oxide coating 48 is laid down and opened up to expose a part of the surface 20 adjacent the N+ region 32 and another part of the surface 20 adjacent the P+ portion 28. The surface 20 adjacent the N+ region 32 is exposed only in the area where the N+ region 32 is disposed within the P portion 30 having the substantially lower impurity concentration and the substantially greater N+/P junction 36 depth. A coating of a highly conductive material is then deposited on the oxide coating 48 and the two exposed parts of the surface 20, and is selectively removed to yield the electrical contacts 38 and 40. Usually, the electrical contacts are made of aluminum which is vaporized onto the surface 20 and then heated to 530°C to alloy it to the silicon. Since the electrical contact 38 to the N+ region 32 is made only in the area over the P portion 28 where the N+/P junction 36 is at a significantly greater depth, the chances of the aluminum spiking through the N+/P junction 36 and shorting the zener diode 10 are greatly reduced.

The N+/P+ characteristic of zener diodes is maintained with the improved zener

diode 10 because the voltage breakdown occurs across the N+/P+ junction 34. The N+/P+ junction 34 has a voltage breakdown of 5.5 volts but the N+/P junction 36 has a higher voltage breakdown of 7.0 volts; consequently, the diode breaks down across the lower voltage N+/P+ junction 34 even though the electrical contact to the N+ region 32 is only made above the N+/P junction 36.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a body of semiconductor material having a surface, a zener diode in said body comprising a first region of one conductivity type containing two diffused portions, one of said portions having a high maximum impurity concentration and having a boundary at a predetermined depth with respect to said surface and the other portion having a significantly lower maximum impurity concentration and a boundary at a significantly lesser depth than said one portion, said first region containing a second region of opposite type conductivity connected to both portions of said first region and separated from each by a PN junction, at least a part of the PN junction between said second region and said one portion being within the zones of maximum impurity concentration of each, a part of the PN junction between said second region and said other portion of said first region being at a significantly greater depth than the PN junction between said second region and said one portion of said first region, and an electrical contact to said second region only where it overlies said other portion of said first region where the PN junction is at a significantly greater depth.

2. A semiconductor device as claimed in claim 1, wherein the maximum impurity concentration in said one portion of said first region is about 8×10^{19} atoms/cm³, the maximum impurity concentration in said other portion of said first region is about 5×10^{18} atoms/cm³, and the maximum impurity concentration in said second region is about 1.2×10^{21} atoms/cm³.

3. A semiconductor device as claimed in claim 2, wherein the PN junction between said second region and said other portion of said first region is at a depth of about 1.4 micrometers with respect to said surface.

4. A semiconductor device as claimed in claim 3, wherein said zener diode is an element of a microcircuit of the monolithic integrated type, said first region being disposed within an isolated region in said body of the same conductivity type as said second region.

5. A process of making a semiconductor device including a zener diode as claimed in claim 1 in a body of semiconductive



material having a surface, comprising forming a first diffusion masking coating on said surface with an opening having a given shape and area exposing a first part of said surface, diffusing conductivity modifiers of one type through said opening into said body to form said one portion of said first region, forming a second diffusion masking coating on said surface with an opening having a shape and area such that it exposes both a portion of said surface which was exposed and a portion which was not exposed by said first diffusion masking coating, diffusing conductivity modifiers of said one type through said opening in said second diffusion masking coating into said body to form said other portion of said first region, forming a third diffusion masking coating on said surface with an opening having a shape and area such that it exposes a portion of said surface which was exposed by both said first and said second diffusion masking coatings, and diffusing conductivity modifiers of opposite type through said opening in said third diffusion masking coating to form said second region.

6. A process as claimed in claim 5 wherein said conductivity modifiers of said one type are boron atoms, and said conductivity modifiers of opposite type are phosphorus atoms.

7. A process as claimed in claim 6, wherein said body has an N type region

containing conductivity modifiers in a concentration of about 5×10^{18} atoms/cm³ into which said diffusions are carried out, the first mentioned diffusion step being performed by heating said body in the presence of a boron source to a temperature of 1150°C for a period of 45 minutes and then heating said body in steam to a temperature of 1165°C for a period of 45 minutes, the second mentioned diffusion step being performed by heating said body in the presence of a boron source to a temperature of 950°C for a period of 40 minutes, then heating said body in a dry atmosphere to a temperature of 1100°C for 50 minutes, and then heating said body in a wet atmosphere to a temperature of 1100°C for 50 minutes, the third mentioned diffusion step being performed by heating said body in the presence of a phosphorus source to a temperature of 1050°C for 18 minutes, and then heating said body in steam to a temperature of 945°C for 45 minutes.

8. A semiconductor device substantially as hereinbefore described with reference to Figures 1—6 of the accompanying drawing.

For the Applicants:
MATTHEWS, HADDAN & CO.,
Chartered Patent Agents,
Haddan House,
33 Elmfield Road,
Bromley, BR1 1SU.

